CONFIDENTIAL

Date	Phenomenon	Description	Solution
10/12/2001	UART-DMA	Miss characters when in the active combination, UART-DMA and long instruction cycle (MUL, IMUL, DIV, IDIV).	
11/30/2001	INT3 with 10K pull-up resistor	Interrupt will abnormal occur when external pull-low resistor with 10K or more large value.	The external pull-low resistor should be with 2.2K ohm.
12/19/2001	9 bit UART serial DMA	The receiver & transmitter will re-start from the initial state if the mode is changed from mode 2 to mode 3 during frame transfer, and data in receive & transmit temp buffer will be cleared.	
2/2/2002	INT5/DMA0, INT6/DMA1	AMD: default normal function pin as INT5/INT6. Enable DMA Control register, DMA0/DMA1 is existing. INT5/DMA0 can share common interrupt vector that dependent on DMA transfer counter register. RDC: default normal function pin as DMA0/DMA1 Enable the EXT-INT bit of DMA Control register, INT5/INT6 is existing. INT5/DMA0 can't share common interrupt vector. (INT5 and DMA0 can't exist at the same time.)	
2/2/2002	Non-specific EOI, Priority	The interrupt with same priority. The ISR will have some problems when with non-specific EOI.	In same priority, suggest to use specific EOI
2/2/2002	PWD, pulse width demodulation	AMD: Timer 1 for the INT2, Timer 0 for INT4 RDC: Timer 1 for INT4, Timer 0 for INT2	Software modify
8/2/2002	INT5/INT6, IR is active twice	The IR bit for INT5/INT6 is active twice during one external INT5/INT6 trigger.	Software solved. In the service routine, execute first time ISR and give up the second time ISR.

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11/12/2002	EDRAM (offset E4h) bit 15 (EN)	After write bit 15 (EN) to 1, even though clear this bit to 0. But this bit is always read “1”. Actually, write this bit “0” the action is successful; The read data path is errant. So this bit is always read “1”.	
3/31/2003	DAA/DAS Instructions.	When AF = 1, CF = 0 and AL = 90h~99h, program execute DAA or DAS instructions. CF will be set to 1. But it is wrong. It should be CF=0.	If use this instruction and check CF result, the program must check the final AL value whether located between 90h and 99h is to avoid this behavior.
4/11/2003	SAL/SAR/SHL/ROL/RCL/ RCR Instructions	When the rotate/shift value is 2 that need memr / memw with word cross (Odd address), i.e. word access is not alignment. The value will be wrong (only do shift / rotate 1 time).	When use these instructions, avoid the rotate / shift value is 2 that need memr / memw with word cross (Odd address)
6/03/2003	Combine Trace Flag (TF) with CMP Instruction (***Only happen in R88xx. Already fix it in R11xx.***)	When TF=1 and CMP instruction compare with mem word cross (Odd address), i.e. word access is not alignment. The flags (SF, ZF, ...) value will not be updated.	Set break point behind CMP instruction. Don’t let the situation combine TF=1 with CMP instruction. The flags will be updated correctly.