SDP3B FlashDisk
Product Manual

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Revision History

- *Revisions before Rev. 4.0—initial release and general changes.*
- *Revision 4.0—general editorial changes, new higher capacities products added, some lower capacities removed, new card reader/writer vendor added.*
- *Revision 5.0—identified part number (SDP3BX-YY-390) for 110, 150, 175, 220, 280, 350 and 440 MB capacities.*
- *Revision 6.0—added 256 Mbit technology products, general and editorial changes.*
- *Revision 7.0—added 512 Mbit products, updated product capacities, and modified read & write timing specifications.*

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1. Introduction to the SDP3B FlashDisk

The SanDisk SDP3B FlashDisk products provide high capacity solid state flash me mory that electrically complies with the Personal Computer Memory Card International Association ATA (PC Card ATA) standard. (In Japan, the applicable standards group is JEIDA.) The SDP3B FlashDisk also supports a True IDE Mode that is electrically compatible with an IDE disk drive. SDP3B FlashDisks provide up to 2.0 gigabytes (GB) of formatted storage capacity in a Type II form factor. The host system can support as many cards as there are Type II or III PCMCIA slots.

The SDP3B FlashDisk uses SanDisk Flash memory, which was designed by SanDisk specifically for use in mass storage applications. In addition to the mass storage specific Flash memory chips, the SDP3B FlashDisks include an on-card intelligent controller that provides a high level interface to t he host computer. This interface allows a host computer to issue commands to the memory card to read or write blocks of memory. The host addresses the card in 512 byte sectors. Each sector is protected by a powerful Error Correcting Code (ECC).

The SDP3B FlashDisk on-card intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control. Once the SDP3B FlashDisk has been configured by the host, it appears to the host as a standard ATA (IDE) disk drive. Additional ATA commands have been provided to enhance system performance.

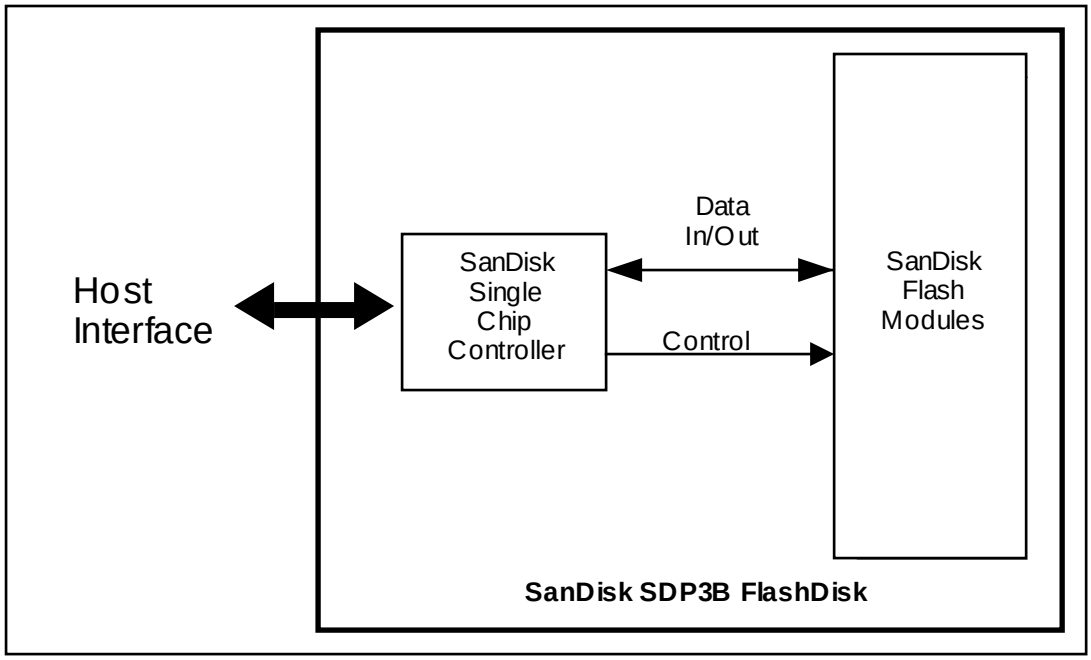

Figure 1-1 SDP3B FlashDisk Block Diagram

1.1. Scope

This document describes the key features and specifications of the SDP3B FlashDisk, as well as the information required to interface this product to a host system.

1.2. Product Models

The SDP3B FlashDisk is available in 32 megabyte to 2.0 gigabyte capacities. All SDP3B FlashDisks are shipped formatted with a DOS file structure.

1.3. System Features

- Up to 2.0 gigabytes of data storage available in a Type II form factor
- PC Card ATA protocol compatible
- True IDE Mode compatible
- Very low CMOS power
- Very high performance
- Very rugged
- Low weight
- Noiseless
- Low Profile
- +5 Volts or +3.3 Volts operation
- Automatic error correction and retry capabilities
- Supports power down commands and sleep modes
- Non-volatile storage (no battery required)
- MTBF of 1,000,000 hours
- Minimum 10,000 insertions
- Standard (SDP3B) and industrial (SDP3BI) versions available

1.4. PCMCIA Standard

SDP3B FlashDisks are fully compatible with the PCMCIA specifications listed below. These specifications may be obtained from:

PCMCIA
2635 N. First St. Suite 209
San Jose, CA 95134
USA
Phone: 408-433-2273
Fax: 408-433-9558

- *PCMCIA PC Card Standard*, January 1995
- *PCMCIA PC Card ATA Specification*, January 1995

1.5. Related Documentation

- *American National Standard X3.221*
  AT Attachment for Interface for Disk Drives Document
  This document can be obtained by calling Global Engineering at 1-800-854-7179.

1.6. Functional Description

SDP3B FlashDisks contain a high level, intelligent subsystem as shown in the block diagram, Figure 1-1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of memory cards. These capabilities include:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Host independence from details of erasing and programming flash memory.
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives).
- Sophisticated system for error recovery including a powerful error correction code (ECC).
- Power management for low power operation.

1.6.1. Flash Technology Independence

The 512 byte sector size of SDP3B FlashDisk is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the SDP3B FlashDisk. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Since the SDP3B FlashDisk uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support the SDP3B FlashDisk today will be able to access future SanDisk cards built with new flash technology without having to update or change host software.

1.6.2. Defect and Error Management

SDP3B FlashDisks contain a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary, SDP3B FlashDisks will replace the entire sector with a spare sector. This is completely transparent to the host and does not consume any user data space.

These defect and error management systems coupled with the solid state construction give SDP3B FlashDisks unparalleled reliability.

1.6.3. Wear Leveling

Wear Leveling is an intrinsic part of the erase pooling functionality of NAND memory. The command is supported as an NOP operation to maintain backward compatibility with existing software utilities.

1.6.4. Using the Erase Sector and Write without Erase Commands

As a result of the SDP3B FlashDisk's high write performance, the Erase Sector and Write Without Erase Commands are no longer supported. There will be no net gain in the use of these commands. Since the write performance of SanDisk products typically improves with the introduction of next generation flash technologies, this feature is no longer required. Any platforms employing these commands in previous SanDisk products will not be affected as a result of the elimination of this function. The Erase Sector Command will still erase the sectors but the Write Without Erase Command will perform a normal Write Command resulting in no net gain in write performance.

1.6.5. Automatic Sleep Mode

A unique feature of the SanDisk SDP3B FlashDisk (and other SanDisk products) is automatic entrance and exit from sleep mode. Upon completion of a command, the SDP3B FlashDisk will enter sleep mode to conserve power if no further commands are received within 5 msec. The host does not have to take any action for this to occur. In most systems, the SDP3B FlashDisk is in sleep mode except when the host is accessing it, thus conserving power. Note that the delay from command completion to entering sleep mode can be adjusted.

When the host is ready to access the SDP3B FlashDisk and it is in sleep mode, any command issued to the SDP3B FlashDisk will cause it to exit sleep and respond. The host does not have to follow the ATA protocol of issuing a reset first. It may do this if desired, but it is not needed. By not issuing the reset, performance is improved through the reduction of overhead but this must be done only for the SanDisk products as other ATA products may not support this feature.

1.6.6. Dynamic Adjustment of Performance versus Power Consumption

This feature is no longer supported. This command will be treated as a NOP (No Operation) to guarantee backward compatibility.

1.6.7. Power Supply Requirements

This is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ± 5% or 5.00 volts ± 10% (± 5% for industrial versions). Per the PCMCIA specification section 2.1.1, the host system must apply 0 volts in order to change a voltage range. This same procedure of providing 0 volts to the card is required if the host system applies an input voltage outside the desired voltage by more than 20%. This means less than 4.0 volts for the 5.00 volt range and less than 2.70 volts for the 3.30 volt range.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. SDP3B FlashDisk System Environmental Specifications

		SDP3B (Standard Version)	SDP3BI (Industrial Version)
Temperature	Operating: Non-Operating:	0° C to 60° C -25° C to 85° C	-40° to 85° C -50° to 100° C
Humidity	Operating: Non-Operating:	8% to 95%, non-condensing 8% to 95%, non-condensing	8% to 95%, non-condensing 8% to 95%, non-condensing
Acoustic Noise:		0 dB	0 dB
Vibration	Operating: Non-Operating:	15 G peak to peak max. 15 G peak to peak max.	15 G peak to peak max. 15 G peak to peak max.
Shock	Operating: Non-Operating:	1,000 G max. 1,000 G max.	1,000 G max. 1,000 G max.
Altitude (relative to sea level)	Operating: Non-Operating:	80,000 feet max. 80,000 feet max.	80,000 feet max. 80,000 feet max.

2.2. SDP3B FlashDisk System Power Requirements

		SDP3B (Standard Version)		SDP3BI (Industrial Version)	
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		3.3V ±5%	5V ± 10%	3.3V ±5%	5V ±5% Only
(maximum Average value) See Notes 1 to 3.	Sleep: Reading: Writing: Read/Write Peak	200 µA 21 mA 21 mA 150 mA/50µs	500 µA 34 mA 34 mA 150 mA/50µs	200 µA 21 mA 21 mA 150 mA/50µs	500 µA 34 mA 34 mA 150 mA/50µs

Note 1. All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.
Note 2. Sleep mode currently is specified under the condition that all card inputs are static CMOS levels and in a "Not Busy" operating state.
Note 3. The currents specified show the bounds of programmability of the product.

2.3. System Performance

All performance timings assume the SDP3B FlashDisk controller is in the default (i.e., fastest) mode.

Start Up Times	Sleep to write: Sleep to read: Reset to ready:	2.5 msec maximum 50 msec maximum 50 msec typical 400 msec maximum
Active to Sleep Delay		Programmable
Data Transfer Rate To/From Flash		20.0 MBytes/sec burst
Data Transfer Rate To/From Host		16.0 MBytes/sec burst
Controller Overhead	Command to DRQ	50 msec maximum

Note: The Sleep to Write and Sleep to Read times are the times it takes the SDP3B FlashDisk to exit sleep mode when any command is issued by the host to when the card is reading or writing. SDP3B FlashDisks do not require a reset to exit sleep mode. See section 1.6.5.

2.4. System Reliability and Maintenance

MTBF (@ 25°C)	1,000,000 hours
Preventive Maintenance	None
Data Reliability	<1 non-recoverable error in 10^{14} bits read
Endurance SDP3B-XX (Commercial Product)	•300,000 erase/program cycles per block typical
Endurance SDP3BI-XX (Industrial Product)	•100,000 erase/program cycles per block typical

2.5. Physical Specifications

Refer to the following table and to Figure 2-1 for additional information.

	SDP3B FlashDisks
Weight:	43 g. (1.52 oz.) maximum
Length:	85.6 ± 0.20 mm (3.370 ± .008 in.)
Width:	54.0 ± 0.10 mm (2.126 ± .004 in.)
Thickness:	5.0 mm max. (.1968 in.)

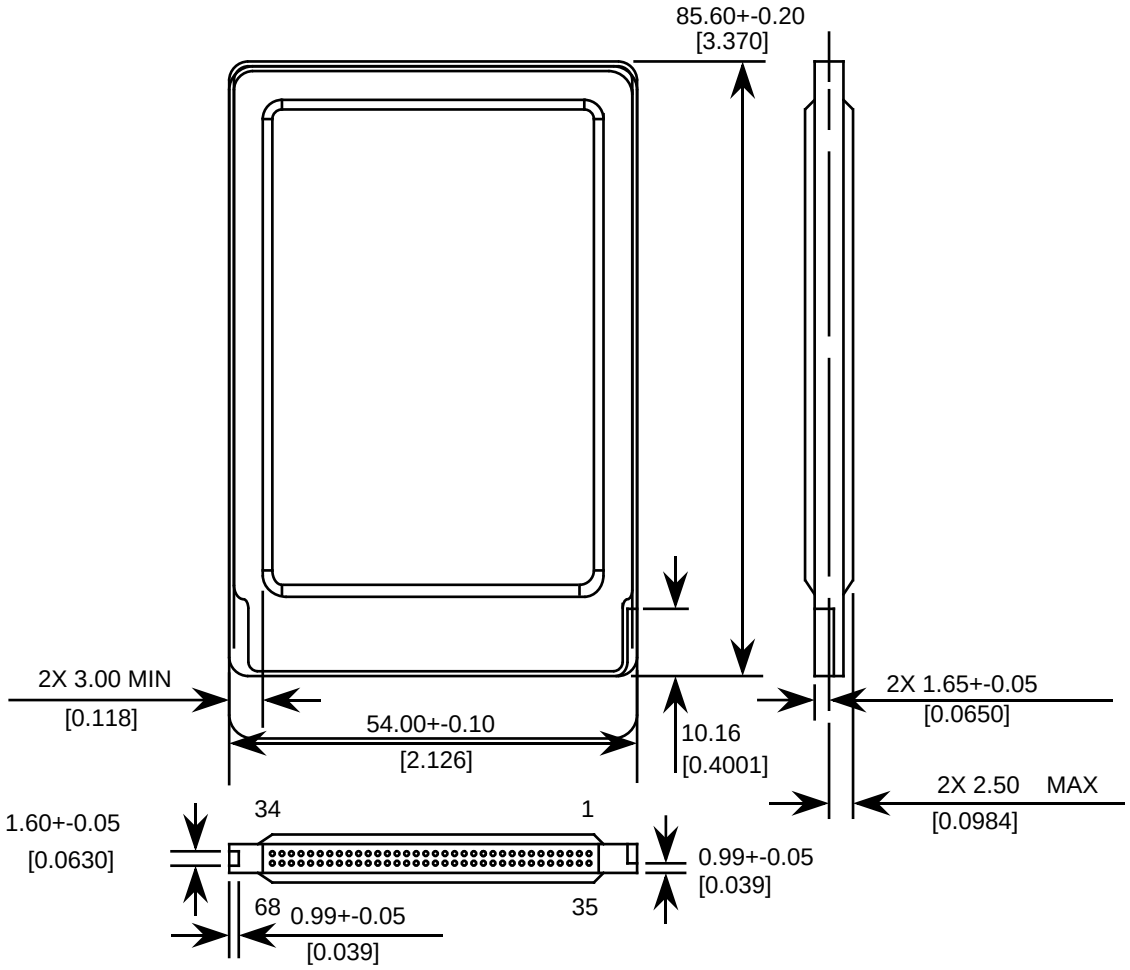

Figure 2-1 SDP3B Type II FlashDisk Dimensions

2.6. Capacity Specifications

The table below shows the specific capacity for the various models and the default number of heads, sectors / track and cylinders.

Model Number	Capacity (formatted)	Sectors/Card (Max LBA+1)	No. of Heads	No. of Sectors/Track	No. of Cylinders
SDP3B(I)-16	16,056,320 bytes	31,360	2	32	490
SDP3B(I)-32	32,112,640 bytes	62,720	4	32	490
SDP3B(I)-64	64,225,280 bytes	125,440	8	32	490
SDP3B(I)-128	128,450,560 bytes	250,880	8	32	980
SDP3B(I)-192	192,413,696 bytes	375,808	16	32	734
SDP3B(I)-256	256,901,120 bytes	501,760	16	32	980
SDP3B(I)-384	384,491,520 bytes	750,960	16	63	745
SDP3B-512	512,483,328 bytes	1,000,944	16	63	993
SDP3B(I)-640	640,475,136 bytes	1,250,928	16	63	1,241
SDP3B-896	896,458,752 bytes	1,750,896	16	63	1,737
SDP3B(I)-1024	1,024,966,656 bytes	2,001,888	16	63	1,986
SDP3B-1280	1,280,434,176 bytes	2,500,848	16	63	2,481
SDP3B-1536	1,536,417,792 bytes	3,000,816	16	63	2,977
SDP3B(I)-2048	2,048,901,120 bytes	4,001,760	16	63	3,970

Note: (I) refers to industrial temperature

3. Installation

3.1. Mounting

The Type II SDP3B FlashDisks fit into any standard PCMCIA Type II (5 mm) or Type III (10.5 mm) socket.

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4. SDP3B FlashDisk Interface Description

4.1. Physical Description

The host is connected to the SDP3B FlashDisk using a standard 68 pin PCMCIA connector consisting of two rows of 34 female contacts each on 50 mil (1.27 mm) centers.

4.1.1. Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4-1. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 4.3.1 to 4.3.4 define the DC characteristics for all input and output type structures.

4.2. Electrical Description

The SDP3B FlashDisk is optimized for operation with hosts, which support the PCMCIA I/O interface standard conforming to the PC Card ATA specification. However, the SDP3B FlashDisk may also be configured to operate in systems that support only the memory interface standard. The configuration of the SDP3B FlashDisk will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the SDP3B FlashDisk.

Table 4-2 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the SDP3B FlashDisk sources are outputs. The SDP3B FlashDisk logic levels conform to those specified in the PCMCIA Release 2.1 specification. Refer to section 4.3 for definitions of Input and Output type.

Table 4-1 Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num	Signal Name	Pin Type	In, Out[4] Type	Pin Num	Signal Name	Pin Type	In, Out[4] Type	Pin Num	Signal Name	Pin Type	In, Out[4] Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10				10				10			
11	A09	I	I1Z	11	A09	I	I1Z	11	A09[2]	I	I1Z

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
12	A08	I	I1Z	12	A08	I	I1Z	12	A08[2]	I	I1Z
13				13				13			
14				14				14			
15	-WE	I	I3U	15	-WE	I	I3U	15	-WE[3]	I	I3U
16	RDY/BSY	O	OT1	16	IREQ	O	OT1	16	INTRQ	O	OZ1
17	VCC		Power	17	VCC		Power	17	VCC		Power
18	VPP		(Not Used)	18	VPP		(Not Used)	18	VPP		(Not Used)
19				19				19			
20				20				20			
21				21				21			
22	A07	I	I1Z	22	A07	I	I1Z	22	A07[2]	I	I1Z
23	A06	I	I1Z	23	A06	I	I1Z	23	A06[2]	I	I1Z
24	A05	I	I1Z	24	A05	I	I1Z	24	A05[2]	I	I1Z
25	A04	I	I1Z	25	A04	I	I1Z	25	A04[2]	I	I1Z
26	A03	I	I1Z	26	A03	I	I1Z	26	A03[2]	I	I1Z
27	A02	I	I1Z	27	A02	I	I1Z	27	A02	I	I1Z
28	A01	I	I1Z	28	A01	I	I1Z	28	A01	I	I1Z
29	A00	I	I1Z	29	A00	I	I1Z	29	A00	I	I1Z
30	D00	I/O	I1Z,OZ3	30	D00	I/O	I1Z,OZ3	30	D00	I/O	I1Z,OZ3
31	D01	I/O	I1Z,OZ3	31	D01	I/O	I1Z,OZ3	31	D01	I/O	I1Z,OZ3
32	D02	I/O	I1Z,OZ3	32	D02	I/O	I1Z,OZ3	32	D02	I/O	I1Z,OZ3
33	WP	O	OT3	33	-IOIS16	O	OT3	33	-IOCS16	O	ON3
34	GND		Ground	34	GND		Ground	34	GND		Ground
35	GND		Ground	35	GND		Ground	35	GND		Ground
36	-CD1	O	Ground	36	-CD1	O	Ground	36	-CD1	O	Ground
37	D11[1]	I/O	I1Z,OZ3	37	D11[1]	I/O	I1Z,OZ3	37	D11[1]	I/O	I1Z,OZ3
38	D12[1]	I/O	I1Z,OZ3	38	D12[1]	I/O	I1Z,OZ3	38	D12[1]	I/O	I1Z,OZ3
Pin Num	Signal Name	Pin Type	In, Out[4] Type	Pin Num	Signal Name	Pin Type	In, Out[4] Type	Pin Num	Signal Name	Pin Type	In, Out[4] Type
39	D13[1]	I/O	I1Z,OZ3	39	D13[1]	I/O	I1Z,OZ3	39	D13[1]	I/O	I1Z,OZ3
40	D14[1]	I/O	I1Z,OZ3	40	D14[1]	I/O	I1Z,OZ3	40	D14[1]	I/O	I1Z,OZ3
41	D15[1]	I/O	I1Z,OZ3	41	D15[1]	I/O	I1Z,OZ3	41	D15[1]	I/O	I1Z,OZ3
42	-CE2[1]	I	I3U	42	-CE2[1]	I	I3U	42	-CS1[1]	I	I3Z
43	-VS1	O	Ground	43	-VS1	O	Ground	43	-VS1	O	Ground
44	-IORD	I	I3U	44	-IORD	I	I3U	44	-IORD	I	I3Z
45	-IOWR	I	I3U	45	-IOWR	I	I3U	45	-IOWR	I	I3Z
46				46				46			
47				47				47			
48				48				48			
49				49				49			

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
50				50				50			
51	VCC		Power	51	VCC		Power	51	VCC		Power
52	VPP		(Not Used)	52	VPP		(Not Used)	52	VPP		(Not Used)
53				53				53			
54				54				54			
55				55				55			
56	-CSEL	I	I2Z	56	-CSEL	I	I2Z	56	-CSEL	I	I2U
57	-VS2	O	OPEN	57	-VS2	O	OPEN	57	-VS2	O	OPEN
58	RESET	I	I2Z	58	RESET	I	I2Z	58	-RESET	I	I2Z
59	-WAIT	O	OT1	59	-WAIT	O	OT1	59	IORDY	O	ON1
60	-INPACK	O	OT1	60	-INPACK	O	OT1	60	-INPACK	O	OZ1
61	-REG	I	I3U	61	-REG	I	I3U	61	-REG[3]	I	I3U
62	BVD2	I/O	I1U,OT1	62	-SPKR	I/O	I1U,OT1	62	-DASP	I/O	I1U,ON1
63	BVD1	I/O	I1U,OT1	63	-STSCHG	I/O	I1U,OT1	63	-PDIAG	I/O	I1U,ON1
64	D08[1]	I/O	I1Z,OZ3	64	D08[1]	I/O	I1Z,OZ3	64	D08[1]	I/O	I1Z,OZ3
65	D09[1]	I/O	I1Z,OZ3	65	D09[1]	I/O	I1Z,OZ3	65	D09[1]	I/O	I1Z,OZ3
66	D10[1]	I/O	I1Z,OZ3	66	D10[1]	I/O	I1Z,OZ3	66	D10[1]	I/O	I1Z,OZ3
67	-CD2	O	Ground	67	-CD2	O	Ground	67	-CD2	O	Ground
68	GND		Ground	68	GND		Ground	68	GND		Ground

Note: 1. These signals are required only for 16 bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. Please refer to section 4.3 for definitions of In, Out type.

Table 4-2 Signal Description

Signal Name	Dir.	Pin	Description
A10—A0 (PC Card Memory Mode)	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the SDP3B FlashDisk, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10—A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2—A0 (True IDE Mode)	I	27, 28, 29	In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File.
A10—A3 (True IDE Mode)			In True IDE Mode, these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	62	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	36, 67	These Card Detect pins are connected to ground on the SDP3B FlashDisk. They are used by the host to determine if the product is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 42	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 4-11, 4-12, 4-15, and 4-16.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15—D00 (PC Card Memory Mode)	I/O	41, 40, 39, 38, 37, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15—D00 (PC Card I/O Mode)			These signals are the same as the PC Card Memory Mode signal.
D15—D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND (PC Card Memory Mode)	--	1, 34, 35, 68	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	60	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the SDP3B FlashDisk when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the SDP3B FlashDisk when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the SDP3B FlashDisk controller registers when the product is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the SDP3B FlashDisk in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	16	In Memory Mode this signal is set high when the SDP3B FlashDisk is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the SDP3B FlashDisk has completed its power up or reset function. No access of any type should be made to the SDP3B FlashDisk during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The SDP3B FlashDisk has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			I/O Operation—After the SDP3B FlashDisk Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	61	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	58	When the pin is high, this signal resets the SDP3B FlashDisk. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	17, 51	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
VPP (PC Card Memory Mode)		18, 52	Programming Voltage power supply is not connected on the SDP3B FlashDisk products.
VPP (PC Card I/O Mode)			This signal is the same for all modes.
VPP (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	43 57	Voltage Sense Signals. -VS1 is grounded so that the SDP3B FlashDisk CIS can be read at 3.3 volts and -VS2 is open and reserved by PCMCIA for a secondary voltage.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	59	SanDisk SDP3B FlashDisks do not assert a -**WAIT** signal.
-WAIT (PC Card I/O Mode)			SanDisk SDP3B FlashDisks do not assert a -**WAIT** signal.
-IORDY (True IDE Mode)			SanDisk SDP3B FlashDisks do not assert an—**IORDY** signal.
-WE (PC Card Memory Mode)	I	15	This is a signal driven by the host and used for strobing memory write data to the registers of the SDP3B FlashDisk when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
WP (PC Card Memory Mode) Write Protect	O	33	Memory Mode—The SDP3B FlashDisk does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation—When the SDP3B FlashDisk is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4.3. Electrical Specification

The following table defines all D.C. Characteristics for the SDP3B FlashDisk. Unless otherwise stated, conditions are:

Vcc = 5V ±10% Vcc = 5V ± 5%
Vcc = 3.3V ± 5%Vcc = 3.3V ± 5%
Ta = 0°C to 60°C Ta = -40°C to 85°C
Absolute Maximum conditions are:
Vcc = -0.3V min. to 7.0V max.
V* = -0.5V min. to Vcc + 0.5V max.
* Voltage on any pin except Vcc with respect to GND.

4.3.1. Input Leakage Current

Note: In the table below, x refers to the characteristics described in section 4.3.2. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc/Vil = Gnd	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note: The minimum pullup resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the SDP3B FlashDisk to reduce power use.

4.3.2. Input Characteristics

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		 0.6	2.4		 0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		 0.6	2.0		 0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

4.3.3. Output Drive Type

Note: In the table below, x refers to the characteristics described in section 4.3.4. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

4.3.4. Output Drive Characteristics

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

4.3.5. Common Memory Read Timing

Table 4-3 Common Memory Read Timing Specification for all Types of Memory

Speed Version Item	Symbol	IEEE Symbol	150 ns	
			Min	Max
Read Cycle Time	t_c(R)	tAVAV	150	
Address Access Time[1]	t_a(A)	tAVQV		150
Card Enable Access Time	t_a(CE)	tELQV		150
Output Enable Access Time	t_a(OE)	tGLQV		75
Output Disable Time from -**OE**	t_{dis}(OE)	tGHQZ		75
Output Disable Time from -**CE**	t_{dis}(CE)	tEHQZ		75
Output Enable Time from -**CE**	t_{en}(CE)	tELQNZ	5	
Output Enable Time from -**OE**	t_{en}(OE)	tGLQNZ	5	
Data Valid from Add Change[1]	t_v(A)	tAXQX	0	
Address Setup Time	t_{su} (A)	tAVGL	20	
Address Hold Time	t_h (A)	tGHAX	20	
Card Enable Setup Time	t_{su} (CE)	tELGL	0	
Card Enable Hold Time	t_h (CE)	tGHEH	20	

1. The -**REG** signal timing is identical to address signal timing.
2. SanDisk SDP3B FlashDisks do not assert a **–WAIT** Signal

NOTE: All timings measured at the SDP3B FlashDisk. Skews and delays from the system driver/receiver to the SDP3B FlashDisk must be accounted for by the system.

4.3.6. Common and Attribute Memory Write Timing

The write timing specifications for Common and Attribute memory are the same.

Table 4-4 Common and Attribute Memory Write Timing Specifications

Speed Item	Symbol	IEEE Symbol	150 ns	
			Min	Max
Write Cycle Time	t_c(W)	tAVAV	150	
Write Pulse Width	t_w(WE)	tWLWH	80	
Address Setup Time[1]	t_{su}(A)	tAVWL	20	
Address Setup Time for -**WE**[1]	t_{su}(A-WEH)	tAVWH	100	
Card Enable Setup Time for -**WE**	t_{su}(CE-WEH)	tELWH	100	
Data Setup Time from -**WE**	t_{su}(D-WEH)	tDVWH	50	
Data Hold Time	t_h(D)	tWMDX	20	
Write Recover Time	t_{rec}(WE)	tWMAX	20	
Output Disable Time from -**WE**	t_{dis}(WE)	tWLQZ		75
Output Disable Time from -**OE**	t_{dis}(OE)	tGHQZ		75
Output Enable Time from -**WE**	t_{en}(WE)	tWHQNZ	5	
Output Enable Time from -**OE**	t_{en}(OE)	tGLQNZ	5	
Output Enable Setup from -**WE**	t_{su}(OE-WE)	tGHWL	10	
Output Enable Hold from -**WE**	t_h(OE-WE)	tWHGL	10	
Card Enable Setup Time	t_{su} (CE)	tELWL	0	
Card Enable Hold Time	t_h (CE)	tGHEH	20	

1. The -**REG** signal timing is identical to address signal timing.
2 SanDisk SDP3B FlashDisks do not assert a **–WAIT** Signal

NOTE: All timings measured at the SDP3B FlashDisk . Skews and delays from the system driver / receiver to the SDP3B FlashDisk must be accounted for by the system.

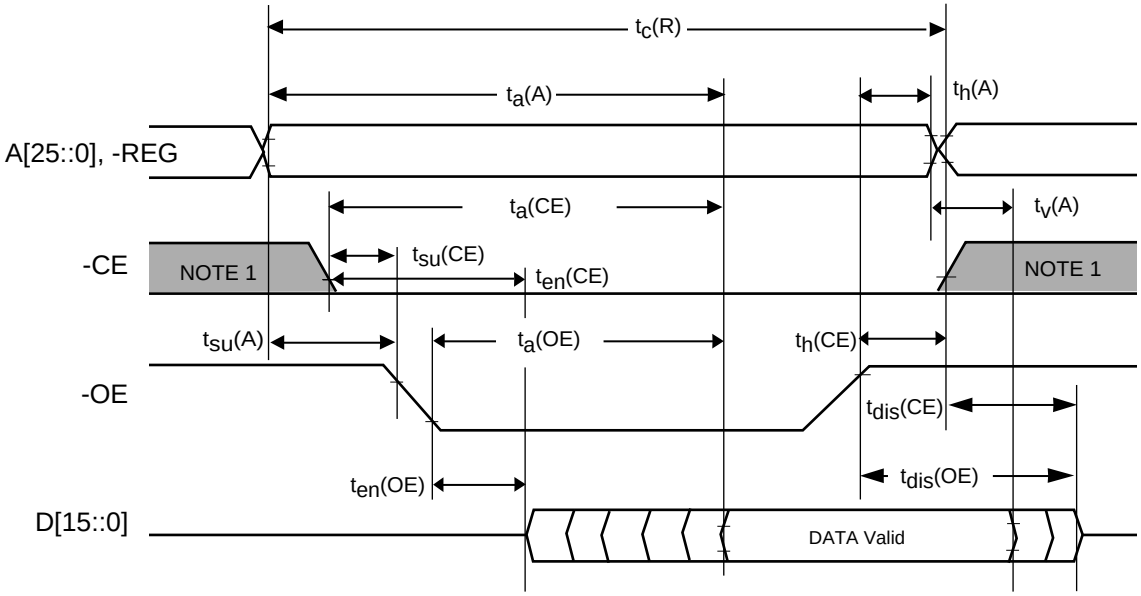
4.3.7. Attribute Memory Read Timing Specification

Table 4-5 Attribute Memory Read Timing Specification for all Types of Memory

Speed Version Item	Symbol	IEEE Symbol	300 ns		600 ns	
			Min	Min	Max	Max
Read Cycle Time	t_c(R)	tAVAV	300		600	
Address Access Time	t_a(A)	tAVQV		300		600
Card Enable Access Time	t_a(CE)	tELQV		300		600
Output Enable Access Time	t_a(OE)	tGLQV		150		300
Output Disable Time from -**OE**	t_{dis}(OE)	tGHQZ		100		150
Output Enable Time from -**OE**	t_{en}(OE)	tGLQNZ	5		5	
Data Valid from Add Change	t_v(A)	tAXQX	0		0	
Address Setup Time	t_{su} (A)	tAVGL	30		100	
Address Hold Time	t_h (A)	tGHAX	20		35	
Card Enable Setup Time	t_{su} (CE)	tELGL	0		0	
Card Enable Hold Time	t_h (CE)	tGHEH	20		35	

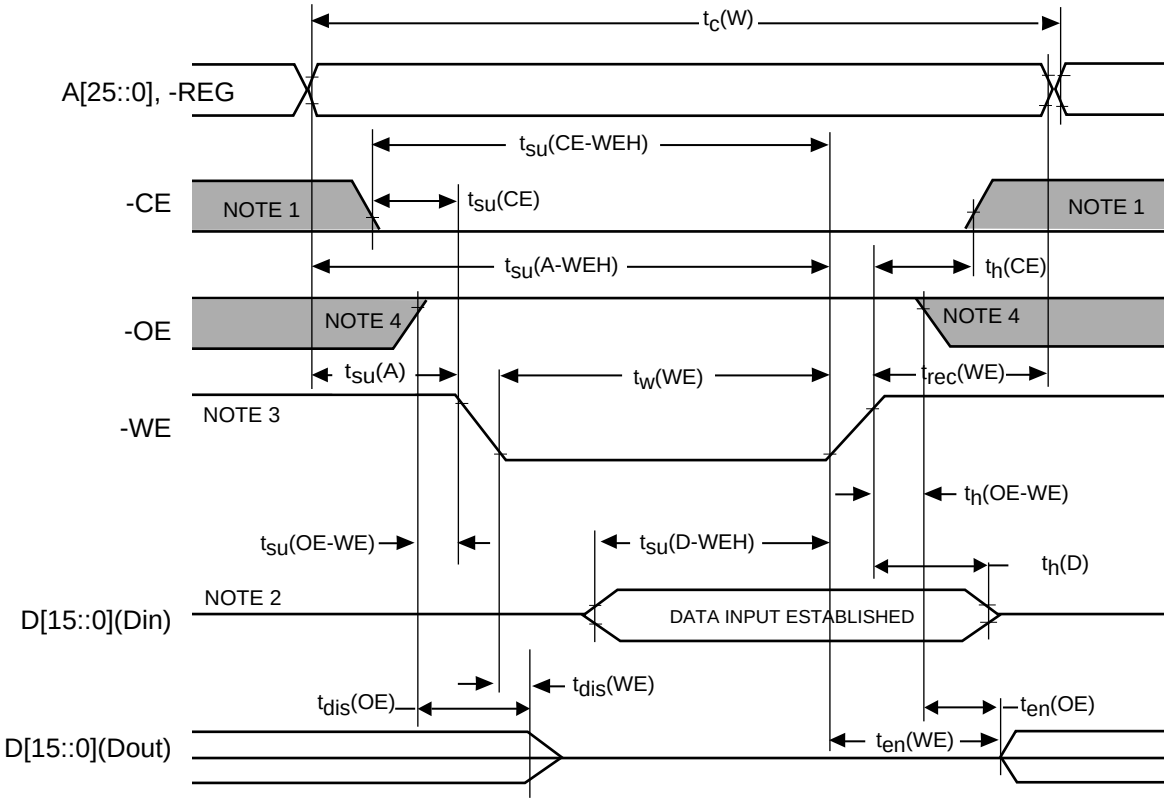
1. SanDisk SDP3B FlashDisks do not assert a **–WAIT** Signal

4.3.8. Memory Timing Diagrams



1. Shaded areas may be high or low.
2. SanDisk SDP3B FlashDisks do not assert a -**WAIT** signal.

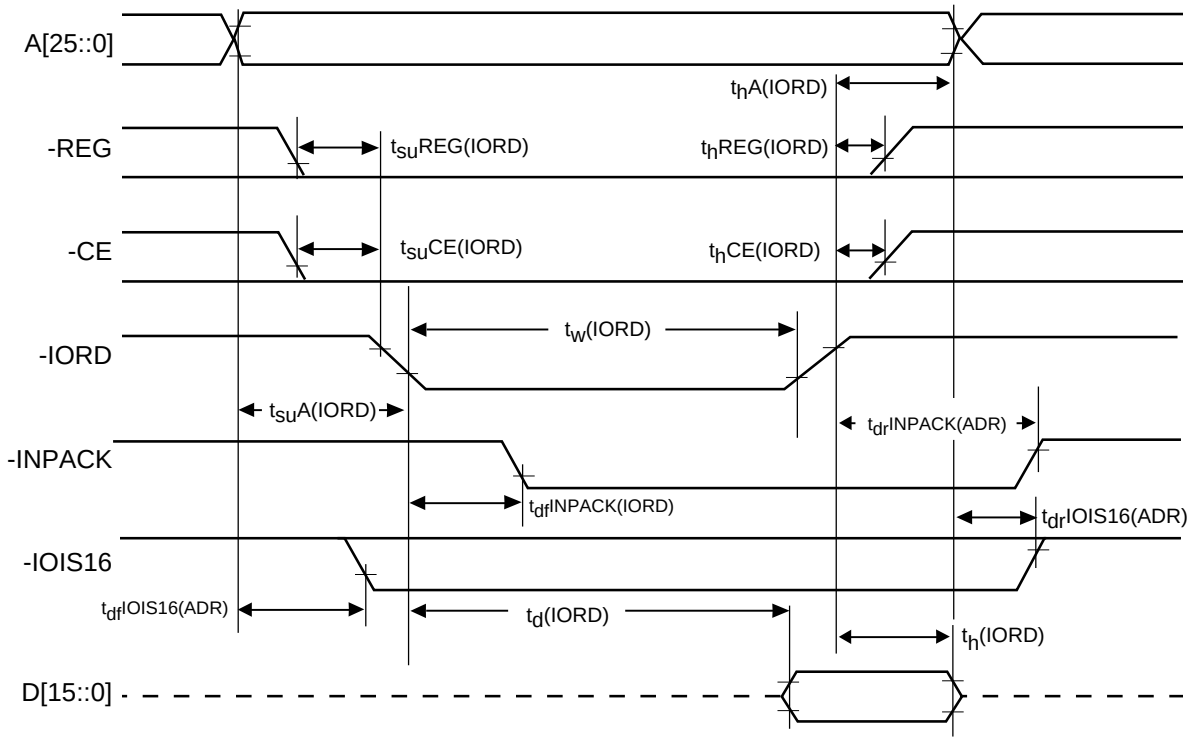
Figure 4-1 Common and Attribute Memory Read Timing Diagram



1. Shaded areas may be high or low.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (**D[15::0]**) by the host system
3. Minimum write pulse width must be met whether or not **-WAIT** is asserted by card.
4. May be high or low for write timing, but restrictions on **-OE** from previous figures apply.
5. SanDisk SDP3B FlashDisks do not assert a **-WAIT** signal.

Figure 4-2 Common and Attribute Memory Write Timing Diagram

4.3.9. I/O Read (Input) Timing Specification



1. All timings are measured at the SDP3B FlashDisk.
2. Skews and delays from the host system driver/receiver to the SDP3B FlashDisk must be accounted for by the system design.
3. **D[15::0]** signifies data provided by the SDP3B FlashDisk to the host system.

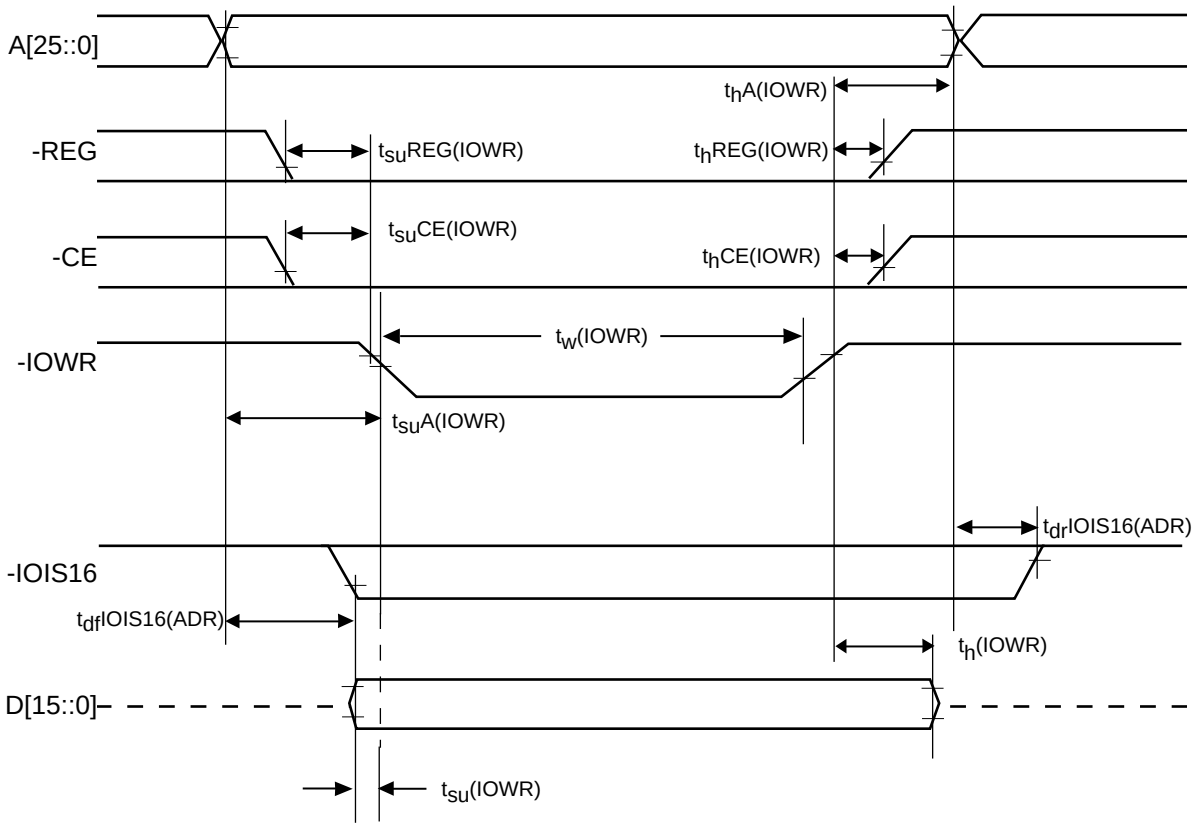
Figure 4-3 I/O Read Timing Diagram

Table 4-6 I/O Read (Input) Timing Specification

Item	Symbol	IEEE Symbol	Min	Max
Data Delay after **-IORD**	t_d(IORD)	tIGLQV		100
Data Hold following **-IORD**	t_h(IORD)	tIGHQX	0	
-IORD Width Time	t_w(IORD)	tIGLIGH	165	
Address Setup before **-IORD**	t_{su}A(IORD)	tAVIGL	70	
Address Hold following **-IORD**	t_hA(IORD)	tIGHAX	20	
-CE Setup before **-IORD**	t_{su}CE(IORD)	tELIGL	5	
-CE Hold following **-IORD**	t_hCE(IORD)	tIGHEH	20	
-REG Setup before **-IORD**	t_{su}REG(IORD)	tRGLIGL	5	
-REG Hold following **-IORD**	t_hREG(IORD)	tIGHRGH	0	
-INPACK Delay Falling from **-IORD**	t_{df}INPACK(IORD)	tIGLIAL	0	45
-INPACK Delay Rising from **-IORD**	t_{dr}INPACK(IORD)	tIGHIAH		45
-IOIS16 Delay Falling from Address	t_{df}IOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	t_{dr}IOIS16(ADR)	tAVISH		35

1. All timings in ns.
2. The maximum load on **-INPACK** and **-IOIS16** is 1 LSTTL with 50 pF total load.
3. SanDisk SDP3B FlashDisks do not assert a **–WAIT** Signal

4.3.10. I/O Write (Output) Timing Specification



1. All timings are measured at the SDP3B FlashDisk.
2. Skews and delays from the host system driver/receiver to the SDP3B FlashDisk must be accounted for by the system design.
3. **D[15::0]** signifies data provided by the host system to the SDP3B FlashDisk.

Figure 4-4 I/O Write Timing Diagram

Table 4-7 I/O Write Timing Specification

Item	Symbol	IEEE Symbol	Min	Max
Data Setup before **-IOWR**	t_{su}(IOWR)	tDVIWL	60	
Data Hold following **-IOWR**	t_h(IOWR)	tIWHDX	30	
-IOWR Width Time	t_wIOWR	tIWLIWH	165	
Address Setup before **-IOWR**	t_{su}A(IOWR)	tAVIWL	70	
Address Hold following **-IOWR**	t_hA(IOWR)	tIWHAX	20	
-CE Setup before **-IOWR**	t_{su}CE(IOWR)	tELIWL	5	
-CE Hold following **-IOWR**	t_hCE(IOWR)	tIWHEH	20	
-REG Setup before **-IOWR**	t_{su}REG(IOWR)	tRGLIWL	5	
-REG Hold following **-IOWR**	t_hREG(IOWR)	tIWHRGH	0	
-IOIS16 Delay Falling from Address	t_{df}IOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	t_{dr}IOIS16(ADR)	tAVISH		35

1. All timing in ns.
2. The maximum load on **-IOIS16** is 1 LSTTL with 50 pF total load.

True IDE Mode

4.3.10.1. Deskewing

The host shall provide cable deskewing for all signals originating from the device. The device shall provide cable deskewing for all signals originating at the host.

All timing values and diagrams are shown and measured at the connector of the selected device.

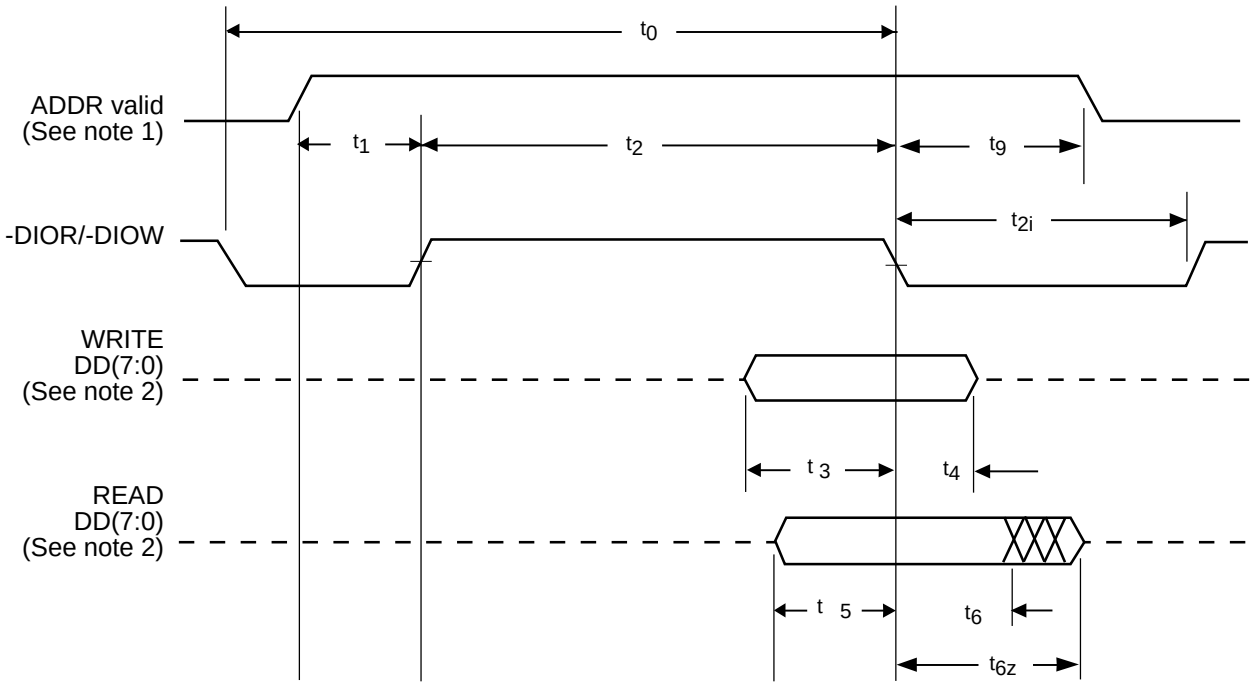
4.3.10.2. Transfer Timing

The minimum cycle time supported by the device in PIO mode 3, 4 and Multiword DMA mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated mode, e.g., a device supporting PIO mode 4 timing shall not report a value less than 120 ns., the minimum cycle time defined for PIO mode 4 timings.

Register transfers

Figure 4-5 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 4-8 defines the minimum value that shall be placed in word 68.



1. Device address consists of signals **-CS0**, **-CS1** and **-DA(2:0)**
2. Data consists of DD(7:0)
3. SanDisk SDP3B FlashDisks do not assert an **-IORDY** signal.

Figure 4-5 Register Transfer To/From Device

Table 4-8 Register Transfer To/From Device

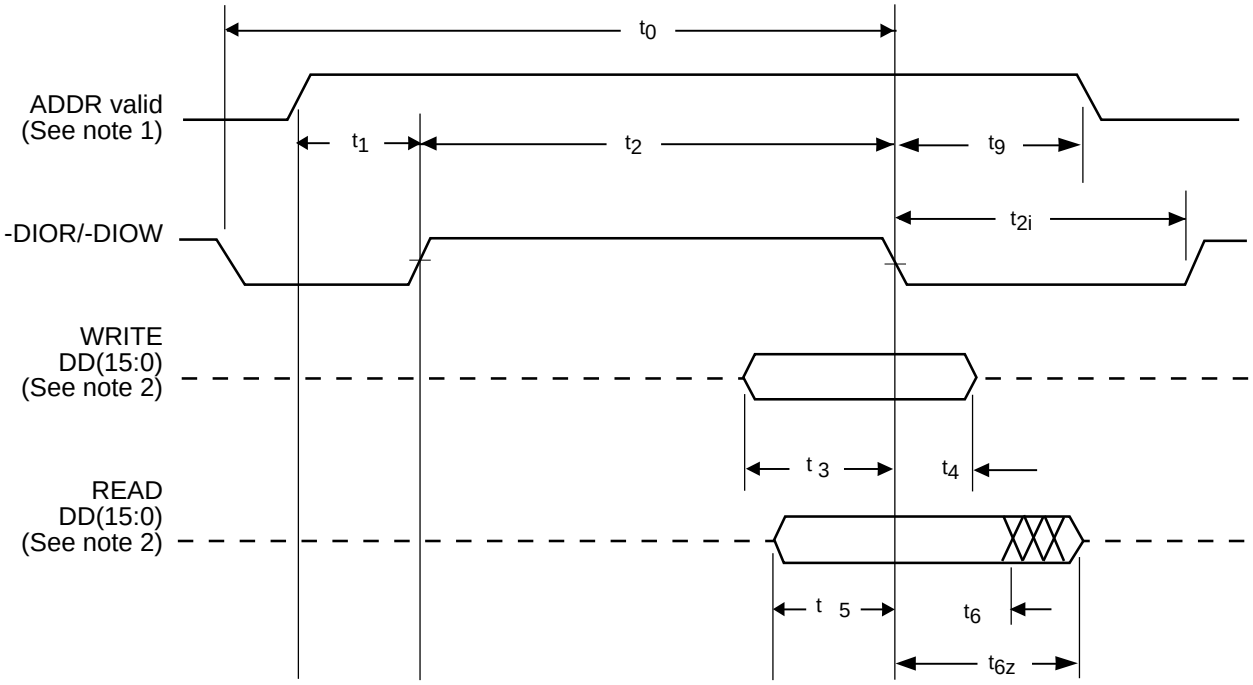
PIO Timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1
t_1	Address valid to -DIOR/-DIOW (min) setup	70	50	30	30	25	
t_2	-DIOR/-DIOW pulse width 8-bit (min)	290	290	290	80	70	1
t_{2i}	-DIOR/-DIOW recovery time (min)	-	-	-	70	25	1
t_3	-DIOW data setup (min)	60	45	30	30	20	
t_4	-DIOW data hold (min)	30	20	15	10	10	
t_5	-DIOR data setup (min)	50	35	20	20	20	
t_6	-DIOR data hold (min)	5	5	5	5	5	
t_{6z}	-DIOR data tri-state (min)	30	30	30	30	30	2
t_9	-DIOR/-DIOW to address valid (min) hold	20	15	10	10	10	

1. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements are greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of-DIOR to the time that the data bus is no longer driven by the device (tri-state).
3. SanDisk SDP3B FlashDisks do not assert an -IORDY signal.

PIO data transfers

Figure 4-6 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 4-9 defines the minimum value that shall be placed in word 68.



1. Device address consists of signals **-CS0**, **-CS1** and **-DA(2:0)**
2. Data consists of DD(15:0)
3. SanDisk SDP3B FlashDisks do not assert an -**IORDY** signal.

Figure 4-6 PIO Data Transfer To/From Device

Table 4-9 PIO Data Transfer To/From Device

PIO Timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1
t_1	Address valid to -DIOR/-DIOW (min) setup	70	50	30	30	25	
t_2	-DIOR/-DIOW pulse width 16-bit (min)	165	125	100	80	70	1
t_{2i}	-DIOR/-DIOW recovery time (min)	-	-	-	70	25	1
t_3	-DIOW data setup (min)	60	45	30	30	20	
t_4	-DIOW data hold (min)	30	20	15	10	10	
t_5	-DIOR data setup (min)	50	35	20	20	20	
t_6	-DIOR data hold (min)	5	5	5	5	5	
t_{6z}	-DIOR data tri-state (min)	30	30	30	30	30	2
t_9	-DIOR/-DIOW to address valid (min) hold	20	15	10	10	10	

1. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements are greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of -**DIOR** to the time that the data bus is no longer driven by the device (tri-state).

3. SanDisk SDP3B FlashDisks do not assert an -**IORDY** signal.

4.4. Card Configuration

The SDP3B FlashDisks are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the SDP3B FlashDisk that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 4-10 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the SDP3B FlashDisk attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.4.1. Attribute Memory Function

Attribute memory is a space where SDP3B FlashDisk identification and configuration information is stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals **-REG** and **-OE** must be active and **-WE** inactive during the cycle. As in the Main Memory Read functions, the signals **-CE1** and **-CE2** control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 4-11 below for signal states and bus validity for the Attribute Memory function.

Table 4-11 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Don't Care	Even Byte

Note: The -**CE** signal or both the -**OE** signal and the -**WE** signal must be de-asserted between consecutive cycle operations.

4.4.2. Configuration Option Register (Address 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the SDP3B FlashDisk.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset—Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the SDP3B FlashDisk in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the SDP3B FlashDisk in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5—Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the SDP3B FlashDisk as shown below.

Note: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 4-12 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

4.4.3. Card Configuration and Status Register (Address 202h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's condition.

Card Configuration and Status Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the SDP3B FlashDisk is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the SDP3B FlashDisk is configured for I/O.

IOis8 The host sets this bit to a one (1) if the SDP3B FlashDisk is to be configured in an 8 bit I/O mode. The SDP3B FlashDisk is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the SDP3B FlashDisk to be in the power saving or active mode. When the bit is one (1), the SDP3B FlashDisk enters a power down mode. When zero (0), the host is requesting the SDP3B FlashDisk to enter the active mode. The PCMCIA Rdy/ -Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The SDP3B FlashDisk automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4.4. Pin Replacement Register (Address 204h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/ -Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit m ay also be written by the host.

RRdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

RWProt This bit is always zero (0) since the SDP3B FlashDisk does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/ -Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 4-13 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final	Comments
	"C" Bit	"M" Bit	"C" Bit	
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.4.5. Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the SDP3B FlashDisk.

4.5. I/O Transfer Function

4.5.1. I/O Function

The I/O transfer to or from the SDP3B FlashDisk can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal **-IOIS16** is asserted by the SDP3B FlashDisk. Otherwise, the **-IOIS16** signal is de-asserted. When a 16-bit transfer is attempted, and the **-IOIS16** signal is not asserted by the SDP3B FlashDisk, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The SDP3B FlashDisk permits both 8- and 16-bit accesses to all of its I/O addresses, so **-IOIS16** is asserted for all addresses to which the SDP3B FlashDisk responds.

Table 4-14 I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

4.6. Common Memory Transfer Function

4.6.1. Common Memory Function

The Common Memory transfer to or from the SDP3B FlashDisk can be either 8 or 16 bits. The SDP3B FlashDisk permits both 8 and 16 bit accesses to all of its Common Memory addresses.

Table 4-15 Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

4.7. True IDE Mode I/O Transfer Function

4.7.1. True IDE Mode I/O Function

The SDP3B FlashDisk can be configured in a True IDE Mode of operation. This SDP3B FlashDisk is configured in this mode only when the -OE input signal is grounded by the host when power is applied to the card. In this True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. SDP3B FlashDisks permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8-bit Mode.

Note: Removing and reinserting the SDP3B FlashDisk while the host computer's power is on will reconfigure the SDP3B FlashDisk to PC Card ATA mode from the original True IDE Mode. To configure the SDP3B FlashDisk in True IDE Mode, the 68-pin socket must be power cycled with the SDP3B FlashDisk inserted and **-OE** (output enable) grounded by the host.

The following table defines the function of the operations for the True IDE Mode.

Table 4-16 IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

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5. ATA Drive Register Set Definition and Protocol

The SDP3B FlashDisk can be configured as a high performance I/O device through:

- Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16 byte I/O block using any available IRQ.
- Memory space.

The communication to or from the SDP3B FlashDisk is done using the Task File registers, which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods:

Table 5-1 I/O Configurations

Standard Configurations				
Config Index	**IO or Memory**	**Address**	**Drive #**	**Description**
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

5.1. I/O Primary and Secondary Address Configurations

Table 5-2 Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

Notes: 1. Register 0 is accessed with **-CE1** low and -**CE2** low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -**CE1** low and -**CE2** high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -**CE1** low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte access to register 0 with -**CE1** high and -**CE2** low accesses the error (read) or feature (write) register.

5.2. Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the SDP3B FlashDisk, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 5-3 Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Notes: 1. Register 0 is accessed with -**CE1** low and -**CE2** low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -**CE1** low and -**CE2** high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -**CE1** low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
A byte access to register 0 with -**CE1** high and -**CE2** low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines that are not indicated are ignored by the SDP3B FlashDisk for accessing all the registers in this table.

5.3. Memory Mapped Addressing

When the SDP3B FlashDisk registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

Table 5-4 Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes: 1. Register 0 is accessed with -**CE1** low and -**CE2** low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -**CE1** low and -**CE2** high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -**CE1** low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
A byte access to address 0 with -**CE1** high and -**CE2** low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte the n even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.
Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the SDP3B FlashDisk.

5.4. True IDE Mode Addressing

When the SDP3B FlashDisk is configured in the True IDE Mode the I/O decoding is as follows:

Table 5-5 True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0	Note
1	0	0	0	0	Even RD Data	Even WR Data	
1	0	0	0	1	Error Register	Features	
1	0	0	1	0	Sector Count	Sector Count	
1	0	0	1	1	Sector No.	Sector No.	
1	0	1	0	0	Cylinder Low	Cylinder Low	
1	0	1	0	1	Cylinder High	Cylinder High	
1	0	1	1	0	Select Card/Head	Select Card/Head	
1	0	1	1	1	Status	Command	
0	1	1	1	0	Alt Status	Device Control	
0	1	1	1	1	Drive Address	Reserved	

5.5. ATA Registers

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address-1) using data bus lines (D15-D8) when -**CE1** is high and -**CE2** is low unless -**IOIS16** is high (not asserted) and an I/O cycle is being performed.

5.5.1. Data Register (Address—1F0[170];Offset 0,8,9)

The Data Register is a 16 bit register, and it is used to transfer data blocks between the SDP3B FlashDisk data buffer and the Host. This register overlaps the Error Register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note that because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-**CE2** = 0 and -**CE1** = 0) operations. SanDisk products treat these accesses as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error/Feature Register	1	0	1	1, Dh	D7-D0
Error/Feature Register	0	1	X	1	D15-D8
Error/Feature Register	0	0	X	Dh	D15-D8

5.5.2. Error Register (Address—1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -**CE2** low and -**CE1** high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a SDP3B FlashDisk status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

5.5.3. Feature Register (Address—1F1[171]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the SDP3B FlashDisk that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -**CE2** low and -**CE1** high.

5.5.4. Sector Count Register (Address—1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SDP3B FlashDisk. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

5.5.5. Sector Number (LBA 7-0) Register (Address—1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SDP3B FlashDisk data access for the subsequent command.

5.5.6. Cylinder Low (LBA 15-8) Register (Address—1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

5.5.7. Cylinder High (LBA 23-16) Register (Address—1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

5.5.8. Drive/Head (LBA 27-24) Register (Address 1F6[176]; Offset 6)

The Drive / Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder / head / sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected When DRV=1, drive (card) 1 is selected. The SDP3B FlashDisk is set to be Card 0 or 1 using the copy field of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3) When operating in the Cylinder , Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

5.5.9. Status & Alternate Status Registers (Address 1F7[177]&3F6[376]; Offsets 7 & Eh)

These registers return the SDP3B FlashDisk status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the SDP3B FlashDisk has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing SDP3B FlashDisk operations. This bit is cleared at power up and remains cleared until the SDP3B FlashDisk is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the SDP3B FlashDisk is ready.

Bit 3 (DRQ) The Data Request is set when the SDP3B FlashDisk requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

5.5.10. Device Control Register (Address—3F6[376]; Offset Eh)

This register is used to control the SDP3B FlashDisk interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (don't care).

Bit 6 This bit is an X (don't care).

Bit 5 This bit is an X (don't care).

Bit 4 This bit is an X (don't care).

Bit 3 This bit is ignored by the SDP3B FlashDisk.

Bit 2 (SW Rst) This bit is set to 1 in order to force the SDP3B FlashDisk to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the SDP3B FlashDisk are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 1 at power on and Reset.

Bit 0 This bit is ignored by the SDP3B FlashDisk.

5.5.11. Card (Drive) Address Register (Address 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SDP3B FlashDisk. Following are some possible solutions to this problem for the PCMCIA implementation:
1. Locate the SDP3B FlashDisk at a non-conflicting address, i.e., Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.
2. Do not install a Floppy and a SDP3B FlashDisk in the system at the same time.
3. Implement a socket adapter, which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SDP3B FlashDisk is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SDP3B FlashDisk 's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SDP3B FlashDisk or b) if provided use an additional Primary/Secondary configuration in the SDP3B FlashDisk which does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

6. ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the SDP3B FlashDisks. Commands are issued to the SDP3B FlashDisk by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 6-1) of command acceptance, all dependent on the host not issuing commands unless the SDP3B FlashDisk is not busy. (The BUSY bit in the status and alternate status registers is 0.)

- Upon receipt of a Class 1 command, the SDP3B FlashDisk sets the BUSY bit within 400 nsec.
- Upon receipt of a Class 2 command, the SDP3B FlashDisk sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears the BUSY bit within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the SDP3B FlashDisk sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears the BUSY bit within 400 nsec of setting DRQ.

6.1. ATA Command Set

Table 6-1 summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1 ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s) (Note 2)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense (Note 1)	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Stand By	E2h or 96h	-	-	-	-	D	-

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Stand By Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector (Note 1)	87h	-	Y	Y	Y	Y	Y
1	Wear Level (Note 1)	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase (Note 2)	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase (Note 2)	38h	-	Y	Y	Y	Y	Y
2	Write Verify Sector(s)	3Ch	-	Y	Y	Y	Y	Y

Note 1: These commands are not standard PC Card ATA commands but provide additional functionality.

Note 2: These commands are not standard PC Card ATA commands and these features are no longer supported with the introduction of 256 Mbit Flash Technology. If one of these commands is issued, the sectors will be erased but there will be no net gain in write performance when using the Write Without Erase command.

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the SDP3B FlashDisk and head parameters are used; D—only the SDP3B FlashDisk parameter is valid and not the head parameter.

6.1.1. Check Power Mode—98H, E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E5H or 98H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

If the SDP3B FlashDisk is in, going to, or recovering from the sleep mode, the SDP3B FlashDisk sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the SDP3B FlashDisk is in Idle mode, the SDP3B FlashDisk sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.1.2. Execute Drive Diagnostic—90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the SDP3B FlashDisk.

The Diagnostic codes shown in Table 6-2 are returned in the Error Register at the end of the command.

Table 6-2 Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Failed (True IDE Mode)

6.1.3. Erase Sector(s)—C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is no longer recommended. There is essentially no net gain in the use of the Erase Sec tors Command and/or the Write Without Erase Commands. This command is supported to guarantee backward compatibility.

6.1.4. Format Track—50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with an FFh pattern. To remain host backward compatible, the SDP3B FlashDisk expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the SDP3B FlashDisk. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256).

6.1.5. Identify Drive—ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Drive command enables the host to receive parameter information from the SDP3B FlashDisk. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 6-3. All reserved bits or words are zero. Table 6-3 is the definition for each field in the Identify Drive Information.

Table 6-3 Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	XXXX	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0240H	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7-8	XXXX	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000H	2	Reserved
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002H	2	Buffer type (dual ported)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	W revision in ASCII (Rev M.ms) set by code Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit 8), LBA supported (bit 9)
50	0000H	2	Reserved
51	0400H	2	PIO data transfer cycle timing mode 4
52	0000H	2	DMA data transfer cycle timing mode Not Supported
53	0003	2	Field validity
54	XXXX	2	Current numbers of cylinders
55	XXXX	2	Current numbers of heads
56	XXXX	2	Current sectors per track
57-58	XXXX	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010XH	2	Multiple sector setting is valid
60-61	XXXX	4	Total number of sectors addressable in LBA Mode
62-63	0000H	4	Reserved
64	0000H	2	Advanced PIO modes supported
65-66	0000H	4	Reserved
67	0000H	2	Minimum PIO transfer without flow control

Word Address	Default Value	Total Bytes	Data Field Type Information
68	0000H	2	Minimum PIO transfer with IORDY flow control
69-127	0000H	130	Reserved
128-159	0000H	64	Reserved vendor unique bytes
160-255	0000H	192	Reserved

6.1.5.1. Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 mb/sec and is not MFM encoded.

6.1.5.2. Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.1.5.3. Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.1.5.4. Word 4: Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

6.1.5.5. Word 5: Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

6.1.5.6. Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.1.5.7. Words 7-8: Number of Sectors per Card

This field contains the number of sectors per SDP3B FlashDisk. This double word value is also the first invalid address in LBA translation mode.

6.1.5.8. Words 10-19: Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20h).

6.1.5.9. Word 20: Buffer Type

This field defines the buffer capability with the 0002h meaning a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the SDP3B FlashDisk.

6.1.5.10. Word 21: Buffer Size

This field defines the buffer capacity of 2 sectors or 1 kilobyte of SRAM.

6.1.5.11. Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

6.1.5.12. Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.1.5.13. Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.1.5.14. Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.1.5.15. Word 48: Double Word Support

This field indicates this product will not support double word transfers.

6.1.5.16. Word 49: Capabilities

This field indicates this product will not support DMA Data transfers but does support LBA mode.

6.1.5.17. Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer.

6.1.5.18. Word 52: DMA Data Transfer Cycle Timing Mode

This field states this product doesn't support any DMA data transfer mode.

6.1.5.19. Word 53: Translation Parameters Valid

Bit 0 of this field is set, indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. Bit 1 is also set, indicating values in words 64 through 70 are valid.

6.1.5.20. Words 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.1.5.21. Words 57- 58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

6.1.5.22. Word 59: Multiple Sector Setting

This field contains a validity flag in the odd byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01H, which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00H, which indicates that R/W Multiple commands are not valid. The only other value returned by the SDP3B FlashDisk in the even byte is a 01H value, which indicates that 1 sector per interrupt can be transferred in R/W Multiple mode.

6.1.5.23. Words 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the SDP3B FlashDisk in LBA mode only.

6.1.5.24. Word 64: Advanced PIO Transfer Modes Supported

Bits 0 and 1 of this field are set to indicate support for PIO transfer modes 3 and 4, respectively.

6.1.5.25. Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

This field indicates in nanoseconds, the minimum cycle time that, if used by the host, the SDP3B FlashDisk guarantees data integrity during the cycle without utilization of flow control.

6.1.5.26. Word 68: Minimum PIO Transfer Cycle Time With Flow Control

This field indicates in nanoseconds, the minimum cycle time the SDP3B FlashDisk supports while performing data transfers using flow control.

6.1.6. Idle—97H,E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3H or 97H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the SDP3B FlashDisk to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

6.1.7. Idle Immediate—95H,E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1H or 95H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the SDP3B FlashDisk to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

6.1.8. Initialize Drive Parameters—91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

Note: SanDisk recommends NOT using this command in any system because DOS determines the offset to the Boot Record based on the number of heads and sectors per track. If a SDP3B FlashDisk is “Formatted” with one head and sector per track value, the same SDP3B FlashDisk will not operate correctly with DOS configured with another heads and sectors per track value.

6.1.9. Read Buffer—E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the SDP3B FlashDisk's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.1.10. Read Multiple—C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SDP3B FlashDisk only supports a block count of 1 as indicated in the Identify Drive Information command. This command is provided for compatibility with future products that may support a larger block count.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count)—modulo (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

6.1.11. Read Long Sector—22H & 23H

Bit ->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command (7)	22H + 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the SDP3B FlashDisk does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of random data transferred in byte mode. Random data is returned instead of ECC bytes because of the nature of the ECC system used. This command has the same protocol as the Read Sector(s) command.

6.1.12. Read Sector(s)—20H & 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H + 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the SDP3B FlashDisk sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.1.13. Read Verify Sector(s)—40H & 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H + 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the SDP3B FlashDisk sets BSY.

When the requested sectors have been verified, the SDP3B FlashDisk clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.1.14. Recalibrate—1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the SDP3B FlashDisk and is provided for compatibility purposes. After this command is executed the Cyl High and Cyl Low as well as the Head number will be 0 and Sec Num will be 1 if LBA=0 and 0 if LBA=1 (i.e., the first block in LBA is 0 while CHS mode the sector number starts at 1).

6.1.15. Request Sense—03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests an extended error code after a command ends with an error. Table 6-4 defines the valid extended error codes for the SDP3B FlashDisk. The extended error code is returned to the host in the Error Register. This command must be the next command issued to the SDP3B FlashDisk following the command that returned an error.

Table 6-4 Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/Aborted Command
0Ch, 38H, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write/Erase Failed

6.1.16. Seek—7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the SDP3B FlashDisk although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.1.17. Set Features—EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 6-5 defines all features that are supported. Please note that the 9AH feature is unique to the SDP3B FlashDisk and are not part of the ATA Specification.

Table 6-5 Features Supported

Feature	Operation
01H	Enable 8-bit data transfer.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69H	Accepted for backward compatibility with the SDP Series but has no impact on the SDP3B FlashDis k.
81H	Disable 8-bit data transfer.
96H	Accepted for backward compatibility with the SDP Series but has no impact on the SDP3B FlashDisk.
9AH	Accepted for backward compatibility with the SDP Series but has no impact on the SDP3B FlashDisk.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01H and 81H are used to enable and clear 8 bit data transfer mode. If the 01H feature command is issued, all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 55H and BBH are the default features for the SDP3B FlashDisk; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

The 9AH Feature is accepted for backward compatibility with the SDP Series but has no impact on the SDP3B FlashDisk. SanDisk does not recommend the use of this command in new designs.

Features 66H and CCH can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs. POR defaults the number of heads and sectors along with 16 bit data transfers and the read / write multiple block count.

6.1.18. Set Multiple Mode—C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the SDP3B FlashDisk to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. The current version of the SDP3B FlashDisk supports only a block size of 1 sector per block. Future versions may support larger block sizes. Upon receipt of the command, the SDP3B FlashDisk sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

6.1.19. Set Sleep Mode- 99H,E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6H or 99H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the SDP3B FlashDisk to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the read to sleep timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

6.1.20. Standby—96H,E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2H or 96H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the SDP3B FlashDisk to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.1.21. Standby Immediate—94H,E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H or 94H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the SDP3B FlashDisk to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.1.22. Translate Sector—87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

When this command is issued, the controller responds with a 512-byte buffer of information on the desired cylinder, head and sector with the actual Logical Address. Table 6-6 represents the information in the buffer. Please note that this command is unique to the SanDisk SDP3B FlashDisk.

Table 6-6 Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04)—LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased 00h = Not Erased
14h—17h	Reserved
18h-1Ah	Reserved
1Bh-1FFh	Reserved

6.1.23. Wear Level—F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

This command is effectively a NOP command and only implemented for backward compatibility with earlier SanDisk SDP series products. The Sector Count Register will always be returned with an 00H indicating Wear Level is not needed.

6.1.24. Write Buffer—E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write Buffer command enables the host to overwrite contents of the SDP3B FlashDisk's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

6.1.25. Write Long Sector—32H & 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state SDP3B FlashDisk, the four bytes of ECC transferred by the host cannot be used by the SDP3B FlashDisk. The SDP3B FlashDisk discards these four bytes and writes the sector with valid ECC fields. This command has the same protocol as the Write Sector(s) command.

6.1.26. Write Multiple Command—C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SDP3B FlashDisk only supports a block count of 1 as indicated in the Identify Drive Command information. This command is provided for compatibility with future products that may support a larger block count.

This command is similar to the Write Sectors command. The SDP3B FlashDisk sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transfe rred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sect ors is not evenly divisible by the sector / block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = sector count (modulo sector / block).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated wh en DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need t o be transferred for successful completion of the command e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

6.1.27. Write Multiple without Erase—CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

SanDisk does not recommend the use of this command in new designs but it is supported as a normal Write Sectors command for backward compatibility reasons.

6.1.28. Write Sector(s)—30H & 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the SDP3B FlashDisk sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.1.29. Write Sector(s) without Erase—38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

SanDisk does not recommend the use of this command in new designs but it is supported as a normal Write Sectors command for backward compatibility reasons.

6.1.30. Write Verify Sector(s)—3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the SDP3B FlashDisk sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.2. Error Posting

The following table summarizes the valid status and error value for all the ATA Command set.

Table 6-7 Error and Status Register

	Error Register							Status Register		
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic*						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify Sector(s)	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

V = valid on this command * See Table 6-2.

7. CIS Description

This section describes the Card Information Structure (CIS) for the SDP3B FlashDisk.

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	04h									Link is 4 bytes	Link to next tuple
004h	DFh	Dev ID Type Dh = I/O				W 1	Speed 7h = ext			I/O Device, No WPS, ext speed	Device ID, WPS, Speed
006h	72h	X	Spd Mantis Eh == 7.0				Spd Expo 2h=100 nsec			700 nsec if no wait	Extended Speed
008h	01h	1x					2K units			2 Kilobytes of Address Space	Device Size
00Ah	FFh	List End Marker								End of Devices	End Marker
00Ch	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Eh	04h									Link is 4 bytes	Link to next tuple
010h	03h	Reserved 0						3 0	W 1	Conditions: 3V operation is allowed, and WAIT is used	3 Volts Operation, Wait Function
012h	D9h	Dev ID Type Dh = I/O				W 1	Speed 01h=250nsec			I/O Device, No WPS, Speed is 250 nsec with Wait	Device ID, WPS, Speed
014h	01h	1x					2K units			2Kilobytes of Address Space	Device Size
016h	FFh	List End Marker								End of Devices	End Marker
018h	18h	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
01Ah	02h									Link is 2 bytes	Link Length
01Ch	DFh	PCMCIA JEDEC Manufacturer's ID								First Byte of JEDEC ID for SanDisk PC Card-ATA 12V	Byte 1, JEDEC ID of Device 1 (0-2K)
01Eh	01h	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2, JEDEC ID
020h	20h	CISTPL_MANFID								Manufacturer's ID Tuple	Tuple Code
022h	04h									Link is 4 bytes	Link Length
024h	45h	Low Byte of PCMCIA Manufacturer's Code								SanDisk JEDEC Manufacturer's ID	Low Byte of PCMCIA Mfg ID
026h	00h	High Byte of PCMCIA Manufacturer's Code								Code of 0 because other byte is JEDEC 1 byte Manufacturer's ID	High Byte of PCMCIA Mfg ID
028h	01h	Low Byte of Product Code								SanDisk Code for SDP Series	Low Byte Product Code
02Ah	04h	High Byte of Product Code								SanDisk Code for PC CARD ATA	High Byte Product Code
02Ch	15h	CISTPL_VER_1								Level 1 version/product info	Tuple Code

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
02Eh	17h									Link to next tuple is 23 bytes	Link Length
030h	04h					TPPLV1_MAJOR				PCMCIA 2.0/JEIDA 4.1	Major Version
032h	01h					TPPLV1_MINOR				PCMCIA 2.0/JEIDA 4.1	Minor Version
034h	53h					ASCII Manufacturer String				'S'	String 1
036h	75h									'u'	
038h	6Eh									'n'	
03Ah	44h									'D'	
03Ch	69h									'i'	
03Eh	73h									's'	
040h	6Bh									'k'	
042h	00h					End of Manufacturer String				Null terminator	
044h	53h					ASCII Product Name String				'S'	Info String 2
046h	44h									'D'	
048h	50h									'P'	
04Ah	00h					End of Product Name String				Null terminator	
04Ch	35h									'5'	Info String 3
04Eh	2Fh									'/'	
050h	33h									'3'	
052h	20h									' '	
054h	30h					SanDisk Card CIS Revision Number				'0'	
056h	2Eh									'.'	
058h	36h									'6'	
05Ah	00h					End of CIS Revision Number				Null terminator	
05Ch	FFh					End of List Marker				FFh List terminator	No Info String 4
05Eh	80h					CISTPL_VEND_SPECIF_80				SanDisk Parameters Tuple	Tuple Code
060h	03h					(Field Bytes 3-4 taken as 0)				Link length is 3 byte	Link to next tuple and length of info in this tuple

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
062h	14h	W 0	12 0	NI 0	PP 1	PDNA 0	RIA 1	RIR 0	SP 0	No Wear Level & NO Vpp W:No Wear Level 12:Vpp Not used on Write NI:-INPACK connected PP:Programmable Power PDNA:Pwr Down Not Abort--Cmd RIA:RBsy, ATBsy connected RIR:RBsy Inhibited at Reset SP:No Security Present This definition applies only to cards with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 bytes limited by link length.
064h	08h	R 0	R 0	R 0	R 0	E 1	TPR 0	TAR 0	R8 0	R8:8 bit ROM present TAR:Temp Bsy on AT Reset TPR:Temp Bsy on PCMCIA --Reset E:Erase Ahead Available R:Reserved, 0 for now This definition applies only to card with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 bytes limited by link length.
066h	00h										For Specific platform use Only
068h	21h	CISTPL_FUNCID								Function ID Tuple	Tuple Code
06Ah	02h									Link length is 2 bytes	Link to next tuple
06Ch	04h	Function Type Code								Disk Function	Function Code
06Eh	01h	R 0	R 0	R 0	R 0	R 0	R 0	R 0	P 1	Attempt installation at Post P:Install at POST R:Reserved(0)	
070h	22h	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
072h	02h									Link length is 2 bytes	Link to next tuple
074h	01h	Disk Function Extension Tuple Type								Extension tuple describes the Interface Protocol	Extension Tuple Type for Disk
076h	01h	Interface Type Code								PC Card-ATA Interface	Extension Info
078h	22h	CISTPL_FUNCE								Function Extension tuple	Tuple Code
07Ah	03h									This tuple has 3 info bytes	Link Length
07Ch	02h	Disk Function Extension Tuple Type								Basic PCMCIA-ATA Extension tuple	Extension Tuple Type for Disk

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
07Eh	0Ch	R 0	R 0	R 0	R 0	U 1	S 1	V 0		No Vpp, Silicon Drive with Unique Manufacturer/Serial Number combined string V=0:No Vpp Required V=1:Vpp on Modify Media V=2:Vpp on any operation V=3:Vpp continuous S:Silicon, else Rotating U:ID Drive Mfg/SN Unique	Basic ATA Option Parameters
080h	0Fh	R 0	I 0	E 0	N 0	P3 1	P2 1	P1 1	P0 1	All power down modes and power commands are not needed to minimize power. P0:Sleep Mode Supported P1:Standby Mode Supported P2:Idle Mode Supported P3:Drive Auto Power Control N:Some Config Excludes 3X7 E:Index Bit is Emulated I:Twin -IOis16 Data Reg Only	Extended ATA Option Parameters
082h	1Ah	CISTPL_CONF								Configuration Tuple	Tuple Code
084h	05h									Link Length is 5 bytes	Link to next tuple
086h	01h	RFS 00			RMS 00		RAS 01			Size of Reserved Field is 0 bytes, Size of Register Mask is 1 Byte, Size of Config Base Address is 2 bytes RFS:Bytes in Reserved Field RMS:Bytes in Reg Mask-1 RAS:Bytes in Base Addr-1	Size of fields byte (TPCC_SZ)
088h	07h	TPCC_LAST								Entry with Config Index of 07h is final entry in table	Last entry of configuration table
08Ah	00h	TPCC_RADR (lsb)								Configuration Registers are located at 200h in Reg Space.	Location of Config Registers
08Ch	02h	TPCC_RADR (msb)									
08Eh	0Fh	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	First 4 Configuration Registers are present I:Configuration Index C:Configuration and Status P:Pin Replacement S:Socket and Copy R:Reserved for future use	TPCC_RMSK
090h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
092h	0Bh									Link to next tuple is 11 bytes. Also limits size of this tuple to 13 bytes.	Link to next tuple

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
094h	C0h	I 1	D 1	Configuration Index 0						**Memory Mapped I/O Configuration** Configuration Index for this entry is 0. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
096h	C0h	W 1	R 1	P 0	B 0	Interface Type 0				Memory Only Interface(0), Bvd's and wProt not used, Ready/-Busy and Wait for memory cycles active. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
098h	A1h	M 1	MS 1		IR 0	IO 0	T 0	P 1		Vcc only Power; No Timing, I/O, or IRQ; 2 Byte Mem Space Length; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
09Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Minimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
09Ch	55h	X 0	Mantissa Ah = 5.0			Exponent 5h = 1V				Vcc Nominal is 5 Volts	Vcc Nominal Value
09Eh	4Dh	X 0	Mantissa 9h = 4.5			Exponent 5h = 1V				Vcc Nominal is 4.5 Volts	Vcc Minimum Value
0A0h	5Dh	X 0	Mantissa Bh = 5.5			Exponent 5h = 1V				Vcc Nominal is 5.5 Volts	Vcc Maximum Value
0A2h	75h	X 0	Mantissa Eh = 8.0			Exponent 5h = 10				Max Average Current over 10 msec is 80 mA	Max Average Current
0A4h	08h	Length in 256 bytes pages (lsb)								Length of Mem Space is 2 KB	TPCE_MS Length LSB
0A6h	00h	Length in 256 bytes pages (msb)								Start at 0 on card	TPCE_MS Length MSB

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0A8h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
0AAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0ACh	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
0AEh	00h	I 0	D 0	Configuration Index 0						Memory mapped I/O 3.3V configuration.	TPCE_INDX
0B0h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
0B2h	21h	R 0	DI 0	PI 1	AI 0	SI 0	H 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	TPCE_PD
0B4h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0B6h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0B8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
0BAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0BCh	0Dh									Link to next tuple is 13 bytes. Also limits size of this tuple to 15 bytes.	Link to next tuple
0BEh	C1h	I 1	D 1	Configuration Index 1						**I/O Mapped Contiguous 16 registers configuration** Configuration Index for this entry is 1. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
0C0h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0C2h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
0C4h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Minimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
0C6h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
0C8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5 Volts	Vcc Minimum Value
0CAh	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value
0CCh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0CEh	64h	R 0	S 1	E 1	IO AddeLines 4					Supports both 8 and 16 bit I/O hosts. 4 Address lines and no range so 16 registers and host must do all selection decoding. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0D0h	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present V:Vendor Unique IRQ B:Bus Error IRQ I:IO Check IRQ N:Non-Maskable IRQ	TPCE_IR
0D2h	FFh	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0—15 recommended.	TPCE_IR Mask Extension Byte 1

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0D4h	FFh	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	Recommended routing to any "normal, maskable" IRQ.	TPCE_IR Mask Extension Byte 2
0D6h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
0D8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0DAh	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
0DCh	01h	I 0	D 0	Configuration Index 1						I/O mapped contiguous 16 3.3V configuration	TPCE_INDX
0DEh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
0E0h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
0E2h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0E4h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0E6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45 mA	Max Average Current
0E8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0EAh	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple
0ECh	C2h	I 1	D 1	Configuration Index 2						**AT Fixed Disk Primary I/O Address Configuration** Configuration Index for this entry is 2. Interface Byte follows this byte. Default Configuration	TPCE_INDX
0EEh	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0F0h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Description; No Timing; I/O and IRQ present; No Mem Space; Misc Entry present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
0F2h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Minimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
0F4h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
0F6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5Volts	Vcc Minimum Value
0F8h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value
0FAh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0FCh	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (1F0-1F7, 3F6-3F7) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0FEh	61h	LS 1		AS 2	N Ranges—1 1					Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
100h	F0h	1st I/O Base Address (lsb)								First I/O Range base is	
102h	01h	1st I/O Base Address (msb)								1F0h	

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
104h	07h	1st I/O Range Length—1								8 bytes total ==> 1F0-1F7h	I/O Length—1
106h	F6h	2nd I/O Base Address (lsb)								2nd I/O Range base is	
108h	03h	2nd I/O Base Address (msb)								3F6h	
10Ah	01h	2nd I/O Range Length—1								2 bytes total ==> 3F6-3F7h	I/O Length—1
10Ch	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
10Eh	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
110h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
112h	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
114h	02h	I 0	D 0	Configuration Index 2						AT Fixed Disk Primary I/O 3.3V configuration	TPCE_INDX
116h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
118h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
11Ah	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
11Ch	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
11Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
120h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
122h	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
124h	C3h	I 1	D 1	Configuration Index 3						**AT Fixed Disk Secondary I/O Address Configuration** Configuration Index for this entry is 3. Interface Byte follows this byte. Default Configuration	TPCE_INDX
126h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Used P:Write Protect Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
128h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present. P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
12Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Minimum Voltage HB:Maximum Voltage SI:Static Current AI:Average Current PI:Peak Current DI:Power Down Current	Power Parameters for Vcc
12Ch	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
12Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Nominal is 4.5Volts	Vcc Minimum Value
130h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Nominal is 5.5Volts	Vcc Maximum Value
132h	75h	X 0	Mantissa Eh = 1.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
134h	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (170-177, 376-377) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
136h	61h	LS 1		AS 2		N Ranges—1 1				Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
138h	70h	1st I/O Base Address (lsb)								First I/O Range base is 170h	
13Ah	01h	1st I/O Base Address (msb)									
13Ch	07h	1st I/O Range Length—1								8 bytes total ==> 170-177h	I/O Length—1
13Eh	76h	2nd I/O Base Address (lsb)								2nd I/O Range base is 376h	
140h	03h	2nd I/O Base Address (msb)									
142h	01h	2nd I/O Range Length—1								2 bytes total ==> 376-377h	I/O Length—1
144h	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
146h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed A:Audio Supported RO:Read Only Mode P:Power Down Supported R:Reserved X:More Misc Fields Bytes	TPCE_MI
148h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
14Ah	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
14Ch	03h	I 0	D 0	Configuration Index 3						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
14Eh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
150h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
152h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
154h	1Eh	X 0	1Eh				+.30			Nominal Operation Supply Voltage Extension Byte	
156h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
158h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
15Ah	04h									Link to next tuple is 4 bytes.	Link to next tuple
15Ch	07h	I 0	D 0	Configuration Index 7						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
15Eh	00h	M 0	MS 0		IR 0	IO 0	T 0	P 0		P:Power info type	TPCE_FS
160h	028h									SanDisk Code	Reserved
162h	0D3h									SanDisk Code	Reserved
164h	014h	CISTPL_NO_LINK								Prevent Scan of Common Memory	Tuple Code
166h	000h	No Bytes Following								Link Length is 0 Bytes	Link to next tuple
168h	0FFh	End of Tuple Chain								End of CIS	Tuple Code

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Appendix A. Ordering Information

To order SanDisk products directly from SanDisk, call **408-542-0595**.

SDP3B SanDisk FlashDisk Series

Model SDP3BX-YY-101

Where:	X:	I	Industrial temperature grade
			Standard
	YY:	16	16.06 MB
		32	32.11 MB
		64	64.22 MB
		128	128.45 MB
		192	192.41 MB
		256	256.90 MB
		384	384.49 MB
		512	512.48 MB
		640	640.48 MB
		896	896.46 MB
		1024	1.02 GB
		1280	1.28 GB
		1536	1.54 GB
		2048	2.05 GB

SanDisk FlashDisk Evaluation Kit

The SanDisk SDP3B FlashDisk Series is a solid-state mass storage system that is fully compatible with the PCMCIA ATA protocol for mass storage on a memory card. SanDisk SDP3B FlashDisks support both PCMCIA Rev. 2.1 and PCMCIA Rev. 1.0 standards.

The FlashDisk Evaluation Kit (Model SDPEV-1) permits designers to quickly and easily evaluate the SanDisk SDP3B FlashDisk solid-state mass storage card using a desktop PC.

The SDP3B FlashDisk Evaluation Kit (Model SDPEV-1) includes the following items:

Hardware

- Evaluation adapter board
- FlashDisk, one unit
- Card extender
- IDE-AB7 adapter board

Software

- FlashDisk Driver and Utilities diskette

Documentation

- *Read Me First flyer*
- *FlashDisk Evaluation Kit User's Guide*
- *Pre-Erase Command Application Note*

Model SDPEV-1

To order, or for more information call: 408-542-0595.

SanDisk FlashDisk Adapter Board

The SanDisk IDE-AB-6 FlashDisk Adapter Board enables a CompactFlash (with adapter), Type II or Type III FlashDisk to be installed in a portable computer's 2.5-inch drive bay, allowing users to replace a 2.5-inch rotating IDE disk drive with the SanDisk FlashDisk. To order this adapter board, use the following model number.

Model IDE-AB-6

Appendix B. Technical Support Services

Direct SanDisk Technical Support

Call SanDisk Applications Engineering at 408-542-0405 for technical support.

SanDisk Worldwide Web Site

Internet users can obtain technical support and product information along with SanDisk news and much more from the SanDisk Worldwide Web Site, 24 hours a day, seven days a week. The SanDisk Worldwide Web Site is frequently updated. Visit this site often to obtain the most up-to-date information on SanDisk products and applications. The SanDisk Web Site URL is http://www.sandisk.com.

System Software and Card Reader/Writers Compatible with the SanDisk SDP3B FlashDisk

Table 1 System Software with SanDisk SDP3B FlashDisk Support

Vendor	Product Name	Telephone Number
AMI	AMICARDZ	770-263-8181
Award/VMI	Cardware	415-968-4433
Databook	Card Talk for Databook Chip	508-762-9779
Phoenix	Phoenix Card Manager Plus	714-440-8000
SystemSoft	Card Soft	508-651-0088
Vadem	Socket Services for VG365, VG465, VG468	408-467-2100

Below is a list of PC card reader/writers that are compatible with the SanDisk FlashDisk. These reader/writers can be installed in desktop PCs to enable the SDP3B FlashDisk to be used in those systems. The SDP3B FlashDisk will operate in any of these reader/writers.

Table 2 Card Readers/Writers Compatible with SanDisk SDP3B FlashDisks

Vendor	Country	Telephone/FAX Number	Product Model	Product Type
Adtron	United States	602-926-9324 FAX 602-926-9359 http://www.adtron.com	SDDA	Adapter for direct IDE-mode operation; 16-bit data interface, BIOS compatible (no drivers); 3.5- or 2.5-inch mount; can replace laptop hard drives.
			SDDB	IDE or ISA connected 8-bit drive; front access.
			SDDC	Industry standard ISA dual-slot adapter, rear entry, cabled to front entry or 100% internal access.
			SDDL	External LPT port drive.
			SDDM	8-bit PC/104 drive.
			SDDP	16-bit PC/104 industry standard adapter.
			SDDR	External RS-232 drive.
			SDDS	Dual-slot SCSI bus drive; ATA card appears as removable disk device; compatible with PC, Macintosh and most workstations.
Altec	Germany	Country Code 49 (0) 511 98381-0 FAX (0) 511 98381-49	EasyDrive	Triple slot (two Type II or one Type II and one Type III) in 3.5-inch frame; IDE interface.
			PCBoardCard	Dual slot (two Type II or one Type III) on ISA slot card.
			i-Drive	Dual slot (two Type II or one Type III) in a 3.5-inch frame; SCSI-2 interface.
			PC/104 Drive	Dual slot (two Type II or one Type III) for PC/104 system bus.

Table 2 Card Readers/Writers Compatible with SanDisk FlashDisks (continued)

Vendor	Country	Telephone/FAX Number	Product Model	Product Type
CardWize Data Solutions	United Kingdom	Country Code 44 118-947-9475 FAX 118-947-4676 Email pcmcia@cardwize.co.uk	MiniWizard 1R WIZ/001	ISA adapter with one rear access slot.
			MiniWizard 2R WIZ/006	ISA adapter with two rear mounted slots.
			CardWizard 1F1R WIZ/101	ISA adapter with one FDD bay mounted slot and one rear access slot.
			CardWizard 2F WIZ/106	ISA adapter with two FDD bay mounted slots.
			CardWizard EXT WIZ/107	ISA adapter with external slot housed in a robust metal case.
			CardWizard IP54 WIZ/108	ISA adapter with one slot IP54 sealed and one rear access slot.
			CardWizard Bezel WIZ/109	ISA adapter with one slot via the standard CardWize bezel and one rear access slot.
			PC104 Wizard 1 WIZ/201	PC104 bus adapter with one slot on board.
			PC104 Wizard 1+H WIZ/202	PC104 bus adapter with one slot on board and headers for remote access slot two.
			PC104 Wizard Stack WIZ/211	PC104 bus adapter with two stacking slots.
			PC104 Wizard Bezel WIZ/221	PC104 bus adapter with one PC104 slot and one bezel mounted slot.
			PC104Wizard FDD WIZ/231	PC104 bus adapter with one PC104 slot and one FDD bay mounted slot.
			PC104 Wizard IP54 WIZ/241	PC104 bus adapter with one PC104 slot and I slot IP54 sealed.
			CardMaestro 3.5” MAE/000	IDE adapter for direct IDE mode 3.5” & 5.25” FDD bay mounted.
			CardMaestro 3.5” PCB MAE/050	IDE adapter PCB on a 3.5”HDD foot print.
			CardMaestro EXT MAE/300	IDE adapter with an external slot.
			CardMaestro 2.5” MAE/400	IDE adapter on a 2.5” HDD footprint.

Table 2 Card Readers/Writers Compatible with SanDisk FlashDisks (continued)

Vendor	Country	Telephone/FAX Number	Product Model	Product Type
Chase/CNF	United States United Kingdom	408-778-1160 FAX 408-779-6558 Country Code 44 (0) 1274 841358 FAX (0) 1274 841316	CARDport isa	ISA adapter with one slot on card and cable to single slot drive bay mounted unit.
CSM	Germany	Country Code 49 (0) 711 7796420 FAX (0) 711 7796440	OmniDrive Professional Drive Dual Front Board Dual Slot Board CIS-I/O Board	Single slot (Type III) external unit that connects to Centronics (EPP) port (supports Windows NT, Windows 95, Windows 3.11 and MS-DOS). Single slot (Type III) external unit that connects to Centronics (EPP) port with professional software for binary data access. ISA adapter with cable to dual slot (one Type III and one Type II) in a 3.5-inch frame. ISA adapter with one slot (Type III) on card and cable to single slot (Type III) in a 3.5-inch frame. ISA adapter with one slot (Type III) on card.
Greystone	United States	408-866-4739 FAX 408-866-8328	CardDock	ISA adapter with cable to dual slot drive bay mounted unit.
Intermart	United States Japan	408-379-0770 FAX 408-379-3666 Country Code 81 3-5489-8301 FAX 3-5489-8310	PCD-15 PCD-10 PCD-15B	Dual slot external unit that connects to SCSI-2 port. (Supports Apple Macintosh, UNIX, Risc, Vme and PowerPC platforms.) Single slot external unit that connects to SCSI-2 port. Same platform support as PCD-15. Internal configuration of PCD-15 for use as built-in for desktop systems.
Karby Corp.	United States	716-889-4204 FAX 716-889-2593	TDM 650 ThinCard Drive TMB 240 ThinCard Drive	Single slot external unit connected to Parallel Port. ISA adapter with cable to single slot internal unit.
Protege	United States	714-450-8950 FAX 714-450-8959	ATA/X	ISA adapter with single cable to either an internal or external unit.

Appendix C. SanDisk Worldwide Sales Offices

SanDisk Corporate Headquarters

140 Caspian Court
Sunnyvale, CA 94089
Tel: 408-542-0500
Fax: 408-542-0503
http://www.sandisk.com

U.S. Industrial/OEM Sales Offices

Northwest
8 Corporate Park, Suite 300
Irvine, CA 92606
Tel: 949-442-8370
Fax: 949-442-8371

Southwest & Mexico
140 Caspian Court
Sunnyvale, CA 94089
Tel: 408-542-0730
Fax: 408-542-0403

North Central & South America
101 Southhall Lane Suite 400
Maitland, FL 32751
Tel: 407-667-4880
Fax: 407-667-4834

North East & South East USA
620 Herndon Pkwy. Suite 200
Herndon, VA 22070
Tel: 703-481-9828
Fax: 703-437-9215

U.S. Retail Sales Offices

Americas
10 Flagstone
Trabuco Canyon, CA 92679
Tel: 949-589-8351
Fax: 949-589-8364

Retail Account Sales
32500 Mills Rd.
Avon, OH 44011
Tel: 440-327-0490
Fax: 440-327-0295

International Retail Sales Offices

European Retail Sales
Wilhelminastraat 10
2011 VM Haarlem
The Netherlands
Tel: 31-23-5514226
Fax: 31-23-5348625

Southern European Retail Sales
Centre Hoche Condorcet
3 Rue Condorcet—B.P. 9
91263 Juvisy Sur Orge Cedex
France
Tel: 33-169-12-16-04
Fax: 33-169-12-16-24

Japan Retail Sales
Umeda-Shinmichi Bldg. 10F
1-1-5 Dojima, Kita-ku
Osaka 530-0003
Tel: 81-6-6343-6480
Fax: 81-6-6343-6481

International Industrial/OEM Sales Offices

Europe
SanDisk GmbH
Karlsruher Str. 2C
D-30519 Hannover, Germany
Tel: 49-511-875-9131
Fax: 49-511-875-9187

Northern Europe
Videroegatan 3 B
S-16440 Kista, Sweden
Tel: 46-08-75084-63
Fax: 46-08-75084-26

Central and Southern Europe
Rudolf-Diesel-Str. 3
40822 Mettmann, Germany
Tel: 49-210-495-3433
Fax: 49-210-495-3434

Japan
8F Nisso Bldg. 15
2-17-19 Shin-Yokohama,
Kohoku-ku
Yokohama 222-0033,
Japan
Tel: 81-45-474-0181
Fax: 81-45-474-0371

Asia/Pacific Rim
89 Queensway, Lippo Center
Tower II, Suite 4104
Admiralty, Hong Kong
Tel: 852-2712-0501
Fax: 852-2712-9385

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Appendix D. Limited Warranty

I. WARRANTY STATEMENT

SanDisk warrants its products to be free of any defects in materials or workmanship that would prevent them from functioning properly for one year from the date of purchase. This express warranty is extended by SanDisk Corporation.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of SanDisk's responsibilities regarding the SanDisk FlashDisk. In satisfaction of its obligations hereunder, SanDisk, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

SanDisk's products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within one year of purchase, SanDisk will have the option of repairing or replacing the defective product, if the following conditions are met:

A. A warranty registration card for each defective product was submitted and is on file at SanDisk. If not, a warranty registration card must accompany each returned defective product. This card is included in each product's original retail package.

B. The defective product is returned to SanDisk for failure analysis as soon as possible after the failure occurs.

C. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

D. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to SanDisk under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

SanDisk reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

SanDisk may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, SanDisk also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

IV. RECEIVING WARRANTY SERVICE

According to SanDisk's warranty procedure, defective product should be returned only with prior authorization from SanDisk Corporation. Please contact SanDisk's Customer Service department at 408-542-0595 with the following information: product model number and description, serial numbers, nature of defect, conditions of use, proof of purchase and purchase date. If approved, SanDisk will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

SanDisk Corporation
Attn: RMA Returns
(Reference RMA or PRA #)
140 Caspian Court
Sunnyvale, CA 94089

V. STATE LAW RIGHTS

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES, OR LIMITATION ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU. This warranty gives you specific rights and you may also have other rights that vary from state to state.

VI. OUT OF WARRANTY REPAIRS

Please contact SanDisk Customer Service at 408-542-0595 for the current out of warranty and repair price list.