PRELIMINARY USER'S MANUAL

PCL6045A

Nippon Pulse Motor Co., Ltd.

Attention:

- The PCL6045A is the improved base function of the PCL6045.
- This manual is only to illustrate the differences between the PCL6045A and PCL6045. Please also refer to the "PCL6045 Users Manual".

September 3, 2002

1. Outline

The PCL6045A is based upon the PCL6045 motion control chip. Because of this, the PCL6045A can be substituted for the PCL6045 without altering the layout of the circuit board and without rewriting the software. The PCL6045A and PCL6045 use the same package.

2. Additional Function Contents

2.1. The noise filter is added to EA/EB/EZ and PA/PB input.

The noise filter can be inserted into EA/EB/EZ and PA/PB input. PCL6045A disregards a signal of less than CLK 3 cycles when the noise filter is inserted. The setting of the filter insertion makes EINF (bit18) and PINF (bit19) of the RENV2 register.

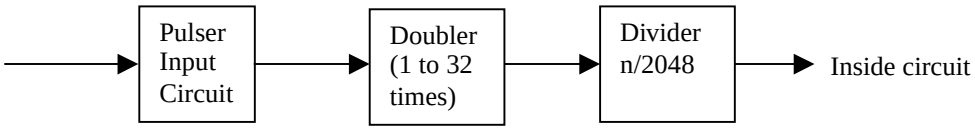
Set the noise filter for EA, EB, and EZ <Set to EINF (bit18) of RENV2> 1: The noise filter is set to EA, EB and also EZ. A signal of less than 3 cycles of the reference clocks is disregarded when the filter is inserted.	<RENV2> (WRITE) 23 16 - - - - - n - -
Set the noise filter for PA and PB <Set to PINF (bit19) of RENV2> 1: The noise filter is set to PA and PB. A signal of less than 3 cycles of the reference clocks is disregarded when the filter is inserted.	<RENV2> (WRITE) 23 16 - - - - n - - -

2.2. The doubler and the divider are added to input the circuit of the pulser (PA and PB)

(Pulser input: From the external pulse generator or the outside manual pulse generator)

The pulser input of the PCL6045 functions at 2 times and 4 times the phase difference at 90 degrees. The divider of n/2048 and the doubler of 1 to 32 times were added in the PCL6045A.

PA and PB



Set the doubler of PA and PB <Set to PMG4 to 0 (bit31 to 27) of RENV6> The magnification is set up to the doubler. When n (1 to 31) is set up, it becomes (n+1).	<RENV6> (WRITE) 31 24 n n n n n - - -
Set the divider of PA and PB <Set to PD10 to 0 (bit26 to 10) of RENV6> The ratio of the divider is set up. When n (1 to 2047) is set up it is done. The divider is n/2048. In the case of n=0, the rate of the divider becomes disenable ((2048/2048)=1).	<RENV6> (WRITE) 31 24 - - - - - n n n 23 16 n n n n n n n n

2.3. Memory condition of pre-register was added to the flag.

The PCL6045 was able to confirm only that the pre-register had become full. The PCL6045A understands the present condition better. It is able to confirm use condition with the numerical value from 0 to 3.

Read out the condition of the pre-register for the comparator 5 <Read from PFC1 to 0 (bit 19 to 18) of RSTS> The condition of the pre-register to compare 5 is possible with a confirmation value of 0 to 3.	<RSTS (READ) 23 16 0 0 - - n n 0 -
Read out the condition of the pre-register for the next operation. <Read from PFM1 to 0 (bit 21 to 20) of RSTS> The condition of the pre-register for the next operation is possible with a confirmation with value of 0 to3.	<RENV2> (WRITE) 23 16 0 0 n n - - 0 -

The detailed use condition of pre-register can be confirmed. (The "✓" shows the condition of memory completion.)

PFM, PFC	2nd pre-register	1st pre-register	register
0 0			
0 1			✓
1 0		✓	✓
1 1	✓	✓	✓

2.4. The status for confirmation was added to determine whether or not the rewrite of the position was done.

In the case when a RMV registration is changed (command: 90h) in the vicinity of the target position in PCL6045 (whether it is disregarded or the rewriting is implemented) it needs to confirm the position at present after it stops because it is indistinct. The PCL6045A added and increased confirmation bit to main status (MSTS), to do conformation work easily.

Read out the reception condition of the rewriting position. <Read from SEOR (bit 13) of MSTS> 1: The rewriting was disregarded. MSTS be return to 0 by reading.	<MSTS> (READ) 15 8 - - n - - - - -

2.5. The circular step binary counter is added (RCIC), for acceleration/deceleration control at circular interpolation.

The PCL6045 did acceleration/deceleration of circular interpolation by utilizing the u-axis. The PCL6045A does acceleration/deceleration by using the step binary counter while circular interpolation added it. The circular step binary counter loads the value of the circular step binary register at the start of circular interpolation.

Register	Contents	Read		Write		2nd pre-register	Read		Write	
		COMBO	Sign	COMBO	Sign		COMBO	Sign	COMBO	Sign
RCI	Step binary number of circular interpolation	FCh	RRCI	BCh	WIRCI	PRCI	CCh	RPRCI	8Ch	WPRCI
RCIC	Step binary counter of circular interpolation	FDh	RRCIC							

2.6. Circular interpolation midway stoppage during the action

Circular interpolation midway stoppage during the action of the PCL6045 was not possible during circular interpolation.

The PCL6045A can continue circular interpolation during midway stoppage.
The output remaining command (54 to 57 hex) is used to do the continuation start.

2.7. Interruption function of action stoppage added

When the PCL6045A does the detection of stoppage timing during the interrupt, it is processed easily by the CPU.

There are normal and abnormal reasons that cause stoppage.
The interrupt error occurs automatically at abnormal stoppage. Makes bit1=1 in the RIRQ register and produce the event interruption that was being used to produce the interruption at normal stoppage. However, the event interruption had to judge and had to read RIST register, because other factors occur.

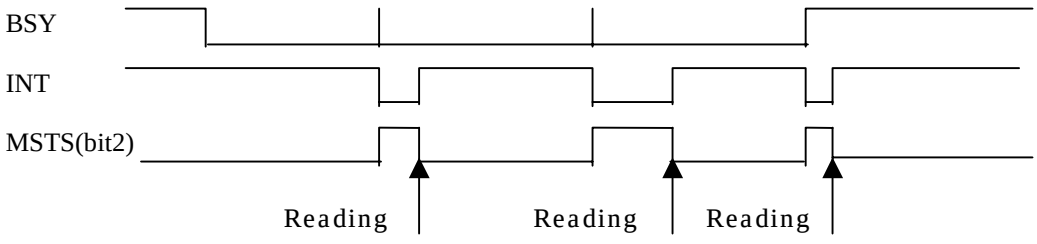
The setting and status for the exclusive use are available when the PCL6045 is to do the stoppage confirmation by interruption processing quickly.

This interrupt output is possible even to mask the continuation operation by the pre-registration.

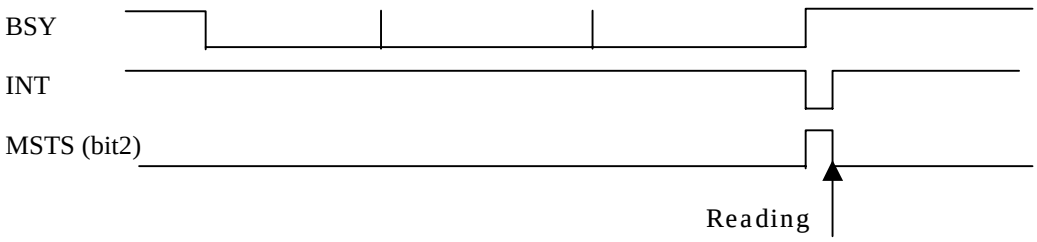
Setting for the interruption of action stoppage. <Set to IEND (bit27) of RENV2> 1:Output the INT signal at action stoppage. However, it does not take part in the cause of stoppage.	<RENV2> (WRITE) 31 24 - - - - n - - -
Setting for mask at the continuation action by pre-register. <Set to PD10 to 0 (bit26 to 10) of RENV6> 1: Pre-register considers as the continuation operation in the setting completion, and does not output. Even if it is in “END=1”, it does not output INT signal.	<RMD> (WRITE) 7 0 n - - - - - - -
Status of the operation completion interruption <Read from SENI (bit2) of MSTS> 1: During the output of an INT signal by operation completion, it returns a "0" automatically by the reading of MSTS.	<RMD> (READE) 7 0 - - - - - n - -

<Movement model by MENI setting>
It is the operation of the setting of the next operation and the 3rd operation written at the start.

• At IEND=1 and MENI=0



• At IEND=1 and MENI=1



If "IEND" and "MENI" have "1" or not, pre-register is output at INT signal at the pre-register wasn't set.

2.8. Mask of the output pulse

PCL6045 could mask the output pulse only at the timer mode.
PCL6045A is able to mask the output pulse during other modes and confirm the program without the operation of the machine.

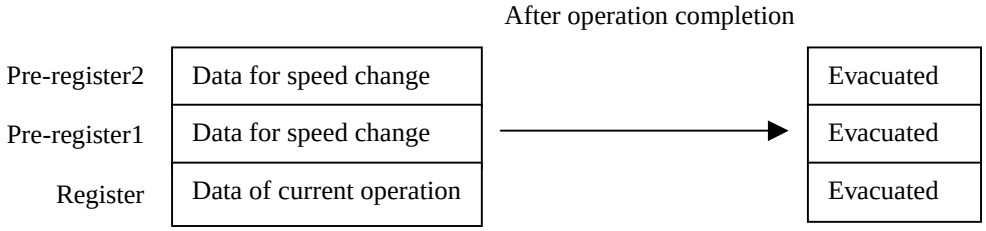
Setting for Mask of the output pulse <Set to PMSK (bit28) of RENV2> 1: Mask the output pulse	<RENV2> (WRITE) 31 24 0 0 - n - - - -

2.9. Added command of the fixed pre-register

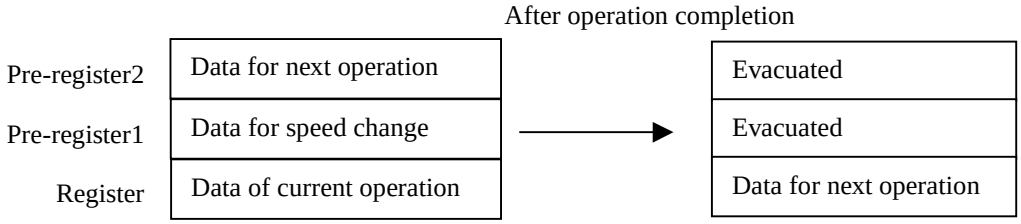
The PCL6045A has a speed change function in the function of the comparator. There is a pre-register function in the comparator 5, and it is able to set up speed change positions several times.
With the PCL6045, speed change was not possible more than twice, because the pre-register for speed setting is fixed at a start command.
The PCL6045A adds the pre-register command and makes it able to use for the settlement of pre-register.

The next motion is done without regard to speed change data, when the speed change data remains in pre-register 1 and the next motion data remains in pre-register 2 after current motion.

ex. 1>

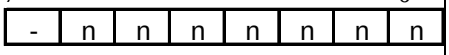


ex. 2>



Fix the pre-register <PRSET: the operation command> 1: The data of pre-register is used as the data of speed change.	<Operation command> 4Fh

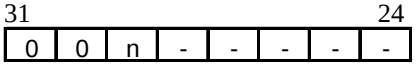
2.10. Addition of the operation mode

Addition contents <Setting to MOD(bit6 to 0) of RMD> 1000010 (42h): Positioning (Absolute position designated on COUNTER1) 1000011 (43h): Positioning (Absolute position designated on COUNTER2) 1010010 (52h): Positioning synchronized to PA/PB (Absolute position designated on COUNTER1) 1010011 (53h): Positioning synchronized to PA/PB (Absolute position designated on COUNTER2) 1100110 (66h): Circular interpolation to CW direction with synchronized u-axis (Linear/Circular interpolation) 1100111 (67h): Circular interpolation to CCW direction with synchronized u-axis (Linear/Circular interpolation) 1101000 (68h): Continues linear interpolarion1 with synchronized PA/PB 1101001 (69h): Linear interpolation1 with synchronized PA/PB 1101010 (6Ah): Continues linear interpolation2 with synchronized PA/PB 1101011 (6Bh): Linear interpolation2 with synchronized PA/PB 1101100 (6Ch): Circular interpolation to CW direction with PA/PB 1101101 (6Dh): Circular interpolation to CCW direction with PA/PB	<RMD> (WRITE) 7 0 

2.11. Automatic start by designated axis stoppage

Any axis can start automatically by setting designated axis stoppage at “MSY1=1” and “MSY0=1” of the operation register. The specified axis sets it up with MAX3 to 0.

In the case of the PCL6045, it was not possible to include a designated axis.
With the PCL6045A, it is possible to include a designated axis. However, the PCL6045A established the switch (SMAX) for the change of the function because the continuation operation may differ from the PCL6045.

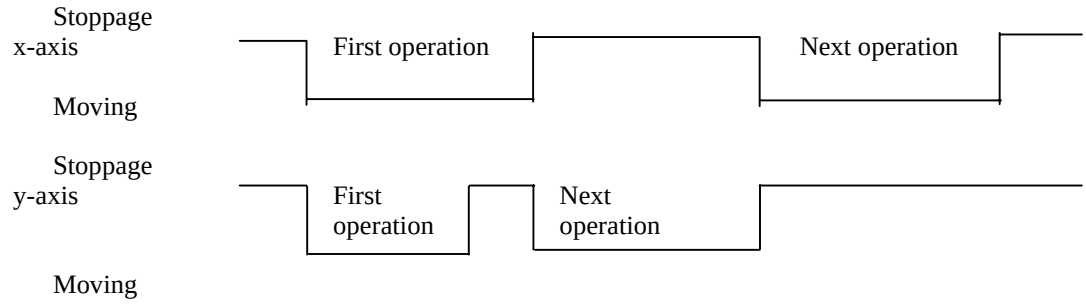
Automatic start by designated axis stoppage <Set to SMAX (bit29) of RENV2> 0: When PCL6045 designated the axis of the self it does not start. 1: possible to start own axis	<RENV2> (WRITE) 31 24 

e.x.>
Setting value

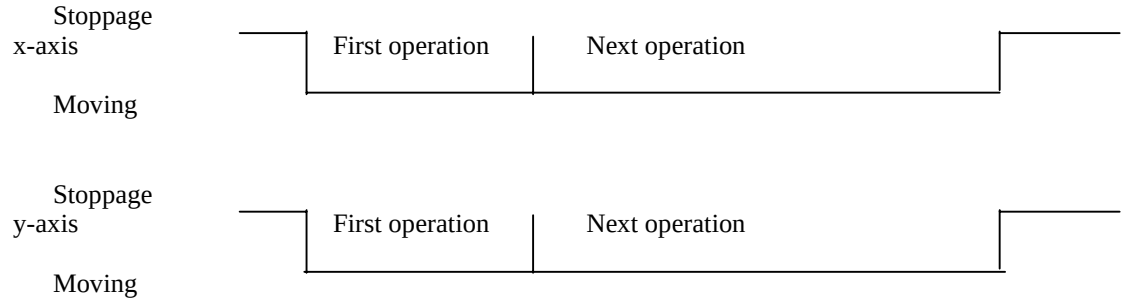
- Operation mode in the first time move of x-axis:
  MSY1 to 0 = 00, MAX3 to 0 = 0000
- Operation mode in the next time move of x-axis:
  MSY1 to 0 = 11, MAX3 to 0 = 0011
- Operation mode in the first time move of y-axis:
  MSY1 to 0 = 00, MAX3 to 0 = 0000
- Operation mode in the next time move of y-axis:
  MSY1 to 0 = 11, MAX3 to 0 = 0011

(Operation time for x-axis of positioning) > (Operation for y-axis of positioning)

1. Case in PCL6045 and PCL6045A (SMAX=0)



2. Case in PCL6045A (SMAX=1)



3. Table of the addition part

3.1. Main status

Bit 13 (SEDR) and bit 2 (SENI) were added.

7	6	5	4	3	2	1	0
SSC1	SSC0	SINT	SERR	SEND	SENI	SRUN	SSCM

15	14	13	12	11	10	9	8
SPDF	SPRF	SEOR	SCP5	SCP4	SCP3	SCP2	SCP1

Bit	Bit name	Description
2	SENI	Flag of Interrupt stoppage This bit change to “1” by moving to stoppage at “IEDN=1” of RENV2 (It returns to “0” by reading main status.)
13	SEOR	This bit became “1” when the position cannot be overwritten. (It returns to “0” by reading main status "0".)

3.2. Operation command

Added a following command.

COMBO	Sign	Description
4Fh	PRESET	Settlement command of pre-register

3.3. Register control command

Added the following commands.

Register	Contents	Read		Write		2nd pre-register	Read		Write	
		COMBO	Sign	COMBO	Sign		COMBO	Sign	COMBO	Sign
RCI	Step binary number of circular interpolation	FCh	RRCI	BCh	WIRCI	PRCI	CCh	RPRCI	8Ch	WPRCI
RCIC	Step binary counter of circular interpolation	FDh	RRCIC							

3.4. RMD (PRMD) register

Bit 7 (MENI) and operation mode (MOD) were added.

7	6	5	4	3	2	1	0
MENI	MOD						

15	14	13	12	11	10	9	8
MIPF	MPCS	MSDP	METM	MCCE	MSMD	MINP	MSDE

23	22	21	20	19	18	17	16
MAX3	MAX2	MAX1	MAX0	MSY1	MSY0	MSN1	MSN0

31	30	29	28	27	26	25	24
0	0	0	0	MIPM	MADJ	MSPO	MSPE

Bit	Bit name	Description
6 to 0	MOD	Add the following operation mode 1000010 (42h): Positioning (Absolute position designated on COUNTER1) 1000011 (43h): Positioning (Absolute position designated on COUNTER2) 1010010 (52h): Positioning synchronized to PA/PB (Absolute position designated on COUNTER1) 1010011 (53h): Positioning synchronized to PA/PB (Absolute position designated on COUNTER2) 1100110 (66h): Circular interpolation to CW direction with synchronized u-axis (Linear/Circular interpolation) 1100111 (67h): Circular interpolation to CCW direction with synchronized u-axis (Linear/Circular interpolation) 1101000 (68h): Continues linear interpolarion1 with synchronized PA/PB 1101001 (69h): Linear interpolation1 with synchronized PA/PB 1101010 (6Ah): Continues linear interpolation2 with synchronized PA/PB 1101011 (6Bh): Linear interpolation2 with synchronized PA/PB 1101100 (6Ch): Circular interpolation to CW direction with PA/PB 1101101 (6Dh): Circular interpolation to CCW direction with PA/PB
7	MENI	1: Even if it is “IEND=1”, INT does not output when pre-register completed setting.

3.5. RENV2 register

Bit 29 (SMAX), bit 28 (PMSK), bit 27 (ISTP), bit19 (PINF) and bit 18 (EINF) were added.

7	6	5	4	3	2	1	0
P3M1	P3M0	P2M1	P2M0	P1M1	P1M0	P0M1	P0M0

15	14	13	12	11	10	9	8
P7M1	P7M0	P6M1	P6M0	P5M1	P5M0	P4M1	P4M0

23	22	21	20	19	18	17	16
EZL	EDIR	EIM1	EIM0	PINF	EINF	P1L	P0L

31	30	29	28	27	26	25	24
0	0	0	PMSK	IEND	PDIR	PIM1	PIM0

Bit	Bit name	Description
18	EINF	1: Attached the noise filter to EA, EB and EZ
19	PINF	1: Attached the noise filter to PA and PB
27	IEND	It outputs INT-signal irrespective of normal stoppage and abnormal stoppage.
28	PMSK	Mask the output pulse
29	AMAX	1: It does effectively even as it is possible be designated own axis by “automatic start by designated axis stoppage”

3.6. RENV6 register

Bit 31 to 27 (RMG4 to 0) and bit 26 to 16 (BD10 to 0) were added.

7	6	5	4	3	2	1	0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

15	14	13	12	11	10	9	8
0	0	ADJ1	ADJ0	BR11	BR10	BR9	BR8

23	22	21	20	19	18	17	16
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

31	30	29	28	27	26	25	24
PMG4	PMG3	PMG2	PMG1	PMG0	PD10	PD9	PD8

Bit	Bit name	Description
26 to 16	PD10 to 0	Setting PA and PB of the dividing (Setting value / 2048)
31 to 27	PMG4 to 0	Setting PA and PB of the multiplication (Value of multiplication – 1)

3.7. RSTS register

Bit 21 to 20 (PFM1 to 0) and bit 19 to 18 (PFC1 to 0) were added.

7	6	5	4	3	2	1	0
SEMG	SSTP	SSTA	SDIR	CND3	CND2	CND1	CND0

15	14	13	12	11	10	9	8
SDIN	SLTC	SCLR	SDRM	SDRP	SEZ	SERC	SPCS

23	22	21	20	19	18	17	16
0	0	PFM1	PFM0	PFC1	PFC0	0	SINP

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0

Bit	Bit name	Description
19 to 18	PFC1 to 0	These bits are able to monitor the use condition of the RCMP5 pre-register.
21 to 20	PFM1 to 0	These bits are able to monitor the use condition about the operation pre-register (except for RCMP5)

3.8. RCI (PRCI) register

This register is the data register of the circular step binary counter. PRCI is 2nd pre-register of RCI. The step binary number needed while the appointing circular is set up, in the deceleration with the circular interpolation. By setting except for 0 value, it is possible that deceleration of automatic ramping down point setting.
Setting range is 0 to 2,147,438,647.

31 30 0

31	30 0
*	

*: This bit is ignored at the write in and became 0 at the read in.

3.9. RCIC register

This register read in value of the step binary counter of circular interpolation. (Only read in)

The value of the PCI registration is loaded at starting interpolation circular, and it is counting and decreasing it by every computation of interpolation. However, it does not count it when the value of the step binary counter is 0.

The value of the counter of completed circular interpolation is rememberd until the next operation of circular interpolation.

Setting range is 0 to 2,147,483,647.

This register is common register for all axes. If this register is read from any axis, it will likely be the same data.