USER'S MANUAL

PROGRAMMABLE HIGH-SPEED PULSE GENERATOR FOR MOTION CONTROL ON FOUR AXES

PCL6045

NPM NIPPON PULSE MOTOR CO., LTD.

Foreword

Thank you for your interest in the programmable high-speed pulse generator PCL6045. To make full use of its versatile performance, read this manual thoroughly. Also, be sure to follow the handling precautions in the last section.

Precautions

(1) The whole or any part of this manual may not be reproduced or transmitted in any form without prior permission of Nippon Pulse Motor Co., Ltd.

(2) This manual may be revised without prior notice for performance and quality improvement.

(3) We compiled this manual carefully. But if you find any thing uncomprehensible or unclear, please report the fact to us.

(4) We have no responsibility for any adverse effect caused by using this chip or by insufficient description of this manual.

Notes

1. Suffixed “x”, “y”, “z” and “u” to pin and bit names stand for X, Y, Z and U axes, respectively.
2. Pins having an upper line on the name (e.g. $\overline{\text{RST}}$) are fixed to negative logic and do not allow change to positive logic. Pins having no upper line on the name are positive logic pins or pins for which input/output logic may be changed.
3. In explanation of register bits, “n” and “0” indicate the bit positions. Please note that when “0” is used to indicate bit positions, it cannot be changed and the bits will always read “0.”

Contents

1. General Description

1.1 Outline of the Chip

The PCL6045, a CMOS LSI, is a high-speed pulse generator used to drive stepping motors and pulse-train input servomotors according to commands received through the CPU bus interface. By generating pulses at a constant speed or in linear or S-curve acceleration/deceleration, the chip can control these motors for continuous operation or in-positioning and origin return.

The chip can control four axes and allows linear interpolation among two to four axes and circular interpolation between the desired two axes. The chip also provides pins for checking its own operation status, outputting an interrupt signal based on conditions, and a function to control a servomotor driver.

Our intelligent design concept makes all these functions easy to access by sending simple commands from the CPU and reduces the burden on the CPU.

1.2 Features

Four CPU Interfaces

The PCL6045 provides the following four CPU interfaces:

(1) 8-bit interface to Z80
(2) 16-bit interface to 8086
(3) 16-bit interface to H8
(4) 16-bit interface to 68000

Two Types of Acceleration/Deceleration

Linear and S-curve acceleration/deceleration modes are available. Onto the mid-way of the S-curve acceleration/deceleration, linear acceleration/deceleration can be added by setting the range of acceleration/deceleration. Since acceleration and deceleration characteristics can be set independently when setting the S-curve range, it is possible to accelerate linearly and then decelerate in S curve or to accelerate in S curve and then decelerate linearly.

Interpolation

It is possible to execute linear interpolation among two to four axes or circular interpolation between any two desired axes.

Override of Pulse Output Rate

The pulse output rate can be changed during an in progress operation while in any mode.

Two Override Modes of Target Position

(1) During in-positioning in progress, the target position (moving amount) can be changed. If the PCL6045 has already generated pulses beyond the newly designated target, it decelerates the rate and stops generating pulses (immediately stops outputting pulses in constant speed operation) and then generates pulses in reverse direction.

(2) The PCL6045 starts in the case of continuous mode and stops after generating pulses in a preset number from the time it inputs an external signal.

Function to Avoid Triangular Drive

In the in-positioning mode, a maximum rate is automatically lowered when the number of output pulses is low, thereby avoiding triangular drive.

Preregisters

During operation in progress, conditions for the next operation and those thereafter can be written in preregisters. These conditions include a moving amount, initial and operating speeds, acceleration and deceleration rates, speed magnification, ramping-down point, operation mode, the center of circular interpolation, sections of S-curve acceleration and deceleration and comparator data. When the PCL6045 completes the present operation, it is set to the conditions written in preregisters.

Four Counters for Each Axis

Counter 1: The 28-bit counter counts output pulses to check the command position.

Counter 2: The 28-bit counter counts input EA/EB signals, output pulses or input PA/PB signals to check the machanical position. If desired, it can be used as a universal counter.

Counter 3: The 16-bit counter counts deviation between output pulses and input EA/EB signals, output pulses and input PA/PB signals or input EA/EB and PA/PB signals to check deviation between the command position and the mechanical position.

Counter 4: The 28-bit counter counts output pulses, input EA/EB signals, input PA/PB signals or one half the reference clock. It is used when a synchronization signal is output. If desired, it can be used as a universal counter.

All these counters can be reset by writing the command or inputting the CLR signal. Also, they can be latched by writing the command or inputting the LTC or ORG signal.

Five Comparators for Each Axis

Each comparator compares the set value with the value of an internal counter selected from counters 1 (command position), 2 (mechanical position), 3 (deviation) and 4 (universal). If desired, comparators 1 and 2 can be used to initiate soft limit signals +SL and –SL.

Soft Limit Function

Soft limits can be set using two comparators. When the operation status is in the limits, the PCL6045 stops generating pulses, immediately or after deceleration. Thereafter, it can generate pulses only in reverse direction.

Backlash Correction

Whenever the moving direction is changed, the PCL6045 corrects backlash, except for when circular interpolation is being executed.

Synchronization Signal Output

The PCL6045 can output a pulse signal at certain designated intervals.

Simultaneous Start

The command or external signal can start the PCL6045 generating pulses simultaneously for all or some selected axes.

Simultaneous Stop

The command or external signal can simultaneously stop the PCL6045 from generating pulses for all or selected axes. Also, abormal stop of an axis can simultaneously stop the PCL6045 from generating pulses for all axes.

Suppression of Vibration

By designating the control constant in advance, one each reverse and forward pulses can be added just before the stop. This reduces vibration at the stop.

Manual Pulser Input

By inputting signals from the manual pulser, the motor can be directly operated. The signals which can be input from the manual pulser are 90° phase difference signals (multiplied 1, 2 and 4 times) or UP and DOWN signals. The EL signal (soft limit) is effective to stop pulse output in the same direction as the EL signal but not in the reverse direction.

Direct Input from Drive Switch

Plus and minus DR pins are provided for each axis to input signals directly from the operation switch. The function of the switch is to drive the motor in forward and reverse directions.

Out-of-step Detection

The PCL6045 provides the deviation counter which operates based on command pulses and encoder signals EA/EB. It can be used for out-of-step detection and checking of in-positioning in combination with a comparator.

Idling Pulse Output

Use of idling pulses enables setting of an FL pulse rate at the self-starting frequency of the motor for high-speed operation. Idling pulses also make it difficult for the stepping motor to step out if a high initial speed is set for acceleration/deceleration.

Various Operation Modes

Basic operation modes are continuous operation, in-positioning, origin return, linear interpolation and circular interpolation, while various other operations are made available by setting operation mode bits:

(1) Start/stop by writing the commands
(2) Continuous operation and in-positioning by inputting PA and PB signals from the manual pulser
(3) Operation in a fixed quantity and continuous operation by inputting direction signals +DR and –DR from the drive switch
(4) Origin return
(5) In-positioning by writing the command
(6) Hard start of in-positioning by inputting the $\overline{\text{CSTA}}$ signal.
(7) Moving in a designated amount from the time the PCS signal turns on

Various Origin Return Sequences

In constant-speed operation:

(1) An ORG signal stops the chip from generating pulses.
(2) An ORG signal stops the chip from generating pulses after outputting pulses in the preset EZ counter value.
(3) An ORG signal lets the chip generate pulses in reverse direction and stop it from generating pulses after outputting pulses in the preset EZ counter value.
(4) An EL signal stops the chip from generating pulses. (Normal operation)
(5) An EL signal lets the chip generate pulses in reverse direction and stop it from gennerating pulses after outputting pulses in the preset EZ counter value.

In varied-speed operation:

(6) An SD signal lets the chip start decelerating and an ORG signal stops it from generating pulses.

(7) An ORG signal lets the chip start decelerating and stops it from generating pulses after outputting pulses in the preset EZ counter value.

(8) An ORG signal lets the chip start decelerating, output pulses in reverse direction and stop it from generating pulses after outputting pulses in the preset EZ counter value.

(9) An ORG signal lets the chip save the position of ORG signal and return to that saved position after deceleration and stop.

(10) An ORG signal lets the chip save the position of counting up EZ signals and return to that position after deceleration and stop.

(11) An EL signal lets the chip generate pulses in reverse direction after deceleration and stop and then output pulses in the preset EZ counter value before stop.

Four Input Mechanical Systems Signals for Each Axis

(1) +EL signal: When this signal turns on during operation toward plus direction, the chip stops generating pulses immediately after deceleration.

(2) –EL signal: When this signal turns on during operation toward minus direction, the chip stops generating pulses immediately after deceleration.

(3) SD signal: This signal may be made either deceleration signal or stop-after-deceleration signal by setting the bits. If this signal is made a deceleration signal, the chip decelerates the pulse output to the rate of FL register when the signal turns on during varied-speed operation. If the signal is already on at the start, the chip generates pulses in constant-speed mode at the rate of FL register.
If this signal made a stop-after-deceleration signal, the chip stops generating pulses after deceleration to the rate of FL register when the signal turns on during varied-speed operation.

(4) ORG signal: This signal is for origin return.
The input logic of +EL and –EL signals can be changed by the ELL terminal.
The input logic of SD and ORG signals can be changed by setting the bits.

Servomotor Interface

The following three pins are provided for each axis to interface with the servomotor.

(1) INP pin: This pin inputs the in-positioned signal sent from the servomotor driver.

(2) ERC pin: This pin outputs the deviation counter clear signal to the servomotor driver.

(3) ALM pin: When this signal turns on, the PCL6045 stops generating pulses immediately after deceleration whether it is operating in plus or minus direction. The chip cannot output any command pulse when this signal is on.

The input/output logic of INP, ERC and ALM can be changed by setting the bits. Also, the ERC signal is a pulse output and the pulsewidth can be selected from a range of 12μs to 104ms and the signal may be made a level output.

Two Output Pulse Modes

The common pulse mode or 2-pulse mode can be selected and the output logic can be selected.

Emergency Stop Signal ($\overline{\text{CEMG}}$) Input

When this signal turns on, the chip stops generating pulses immediately for all axes. When this signal is on, no axis can be operated.

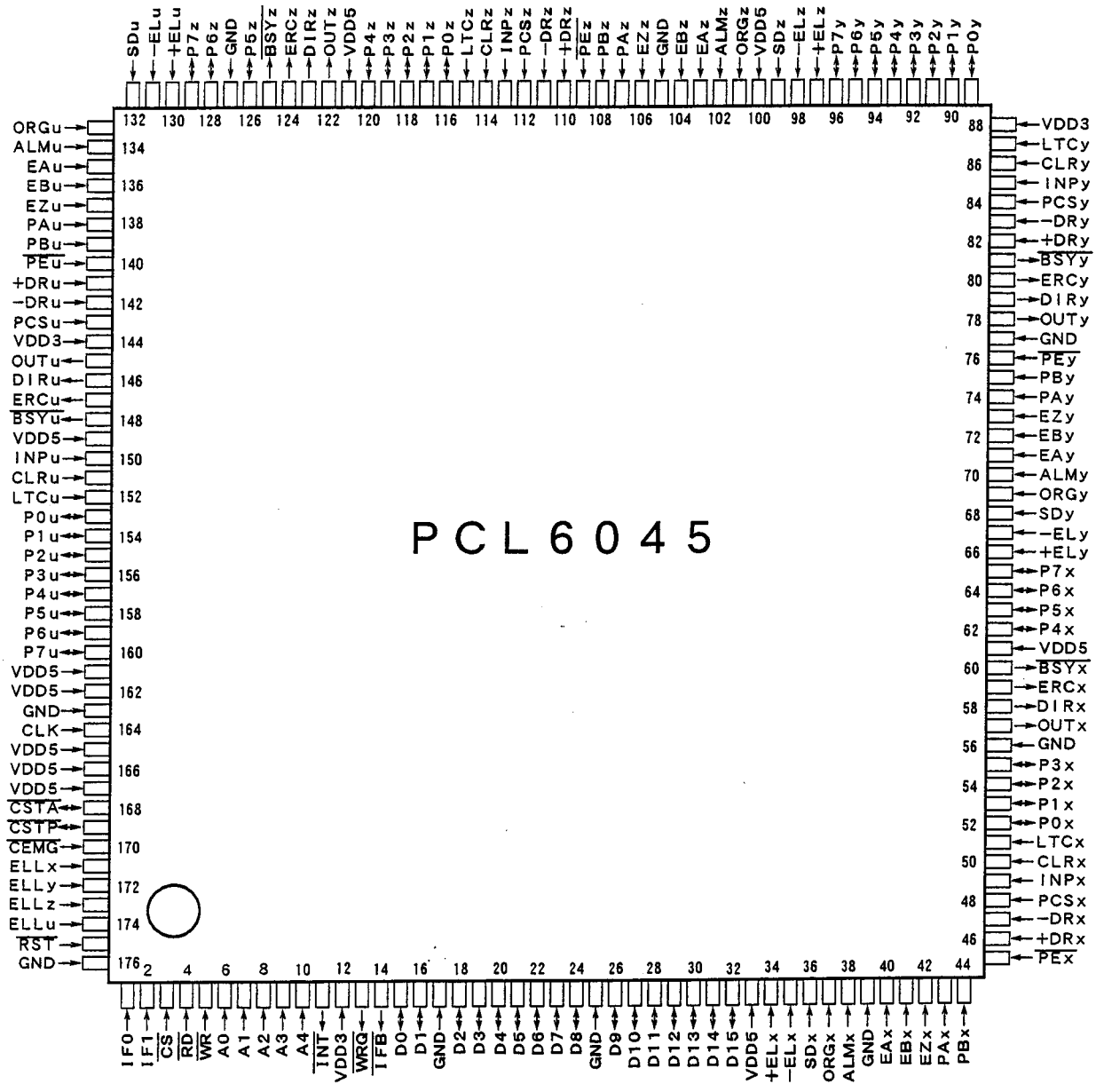
Interrupt Signal Output

The chip can output the $\overline{\text{INT}}$ (interrupt request) signal based on various factors. When each factor on each axis is in OR status, the chip outputs the signal from the $\overline{\text{INT}}$ pin. (Note, however, that wired OR connection is not possible between multiple units of PCL6045.)

2. Specifications

Number of Controllable Axes:	4 (X, Y, Z and U)
Reference Clock:	19.6608MHz standard (20MHz maximum)
In-position Control Range:	–134,217,728 to +134,217,727 (28 bits)
Ramping-down Point Setting Range:	0 to 16,777,215 (24 bits)
Pulse Rate Setting Registers:	FL (lower rate), FH (higher rate) and FA (interpolation rate) for each axis
Pulse Rate Setting Step Range:	1 to 65,535 (16 bits)
Pulse Rate Multiplication Range:	0.1 to 100 times 0.1 to 6,553.5 pps with 0.1x 1 to 65,535 pps with 1x 100 to 6,553,500 pps with 100x (with reference clock 19.6608MHz)
Acceleration/Deceleration Modes:	Linear and S-curve (parameters for acceleration and deceleration can be set independently.)
Acceleration Rate Setting Range:	1 to 65,535 (16 bits)
Deceleration Rate Setting Range:	1 to 65,535 (16 bits)
Automatic Ramping-down Point Setting:	Possible in a range of deceleration time < (acceleration time x 2)
Automatic Pulse Rate Adjustment:	Pulse rate is automatically lowered for in-positioning operation with little moving amount
Manual Operation:	Possible through manual pulser input and push button switch
Counters:	Counter 1: 28-bit command position counter Counter 2: 28-bit mechanical position counter Counter 3: 16-bit deviation counter Counter 4: 28-bit multi-purpose counter
Comparators:	Five 28-bit comparator circuits provided
Interpolation:	Linear interpolation among desired two to four axes Circular interpolation between desired two axes
Operating Temperature Range:	0 to +70°C
Supply Voltages:	+5V ±5% and 3.3V ±5%
Package:	176-pin QFP

3. Terminal Pin Layout



4. Terminal Pin Functions

4.1 GND (Power Supply Pins 17, 25, 39, 56, 77, 105, 127, 163, 176)

These pins input the minus level of power supply. Be sure to connect the power supply to all these pins.

4.2 VDD5 (Power Supply Pins 33, 61, 100, 121, 149, 161, 162, 165, 166, 167)

These pins input +5V ±5% power. Be sure to connect the power supply to all these pins.

4.3 VDD3 (Power Supply Pins 12, 88, 144)

These pins input +3.3V ±5% power. Be sure to connect the power supply to all these pins.

4.4 $\overline{\text{RST}}$ (Input Pin 175)

This pin inputs the reset signal in negative logic. After turning the chip on, be sure to set the pin at a low level to reset it once before starting an operation. Also, input more than eight reference clock signals to the CLK pin while the $\overline{\text{RST}}$ signal is at a low level. For the reset status, refer to "11.1 Resetting."

4.5 CLK (Input Pin 164)

This pin inputs the CMOS level reference clock (all input/output signals except for the reference clock are TTL level). Input the reference clock of 19.6608MHz as standard. Output pulses are produced referring to the clock input to this pin.

4.6 IF0, IF1 (Input Pins 1, 2)

These pins set the CPU interface mode as follows:

IF1	IF0	CPU	Pins and Connected CPU Signals			
			$\overline{\text{RD}}$	$\overline{\text{WR}}$	A0	$\overline{\text{WRQ}}$
L	L	68000	+5V	R/$\overline{\text{W}}$	$\overline{\text{LDS}}$	$\overline{\text{DTACK}}$
L	H	H8	$\overline{\text{RD}}$	$\overline{\text{HWR}}$	(GND)	$\overline{\text{WAIT}}$
H	L	8086	$\overline{\text{RD}}$	$\overline{\text{WR}}$	(GND)	READY
H	H	Z80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A0	$\overline{\text{WAIT}}$

4.7 $\overline{\text{CS}}$ (Input Pin 3)

Setting this pin at a low level makes $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins valid.

4.8 $\overline{\text{RD}}$, $\overline{\text{WR}}$ (Input Pins 4, 5)

Connect CPU interface signals to these pins. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins are valid when the $\overline{\text{CS}}$ pin is at a low level.

4.9 A0 to A4 (Input Pins 6 to 10)

These pins input address signals in positive logic.

4.10 $\overline{\text{INT}}$ (Output Pin 11)

This pin outputs the interrupt request signal to the CPU in negative logic. The pin recovers the OFF status upon reading the REST (error interrupt) or RIST (event interrupt) register. The output status can be checked by reading the main status (MSTSW). If desired, the $\overline{\text{INT}}$ output signal can be masked. Note, however, that wired OR connection of $\overline{\text{INT}}$ pins of multiple units of PCL6045 is not possibble.

4.11 $\overline{\text{WRQ}}$ (Output Pin 13)

This pin outputs the wait request signal to the CPU in negative logic. The PCL6045 requires four cycles of reference clock to process a command. If the $\overline{\text{WRQ}}$ signal is not used, take care not to access the chip from the CPU during these four cycles.

4.12 $\overline{\text{IFB}}$ (Output Pin 14)

This pin outputs the signal in negative logic to indicate that the chip is pocessing a command. It is used to connect the chip to the CPU which is not equipped with any input terminal for wait control.

When a command is written from the CPU, this pin becomes low level, and when the chip completes processing the command this pin becomes high level. Confirm that this pin is high level and then send the next command from the CPU.

4.12 D0 to D7 (Input/Output Pins 15, 16, 18 to 23)

These pins form the bidirectional data bus. When connecting a 16-bit data bus to the PCL6045, connect low-place 8 bits to these pins.

4.13 D8 to D15 (Input/Output Pins 24, 26 to 32)

These pins form the bidirectional data bus. When connecting a 16-bit data bus to the PCL6045, connect the high-place 8 bits to these pins.

When the PCL6045 is interfaced with Z80 by setting both IF1 and IF0 to high level, pull up these pins to VDD5 with 5kΩ to 10kΩ resistance. (Pull-up may be made with one resistor for all 8 pins.)

4.14 $\overline{\text{CSTA}}$ (Input/Output Pin 168)*2

This pin is the input/output pin of simultaneous start signal of negative logic. To simultaneously start multiple units of PCL6045, connect this pin of all the units in cascade. The pin status can be checked by reading the extension status (RSTS).

4.15 $\overline{\text{CSTP}}$ (Input/Output Pin 169)*2

This pin is the input/output pin of simultaneous stop signal of negative logic. To simultaneously stop multiple units of PCL6045, connect this pin of all the units in cascade. The pin status can be checked by reading the extension status (RSTS).

4.16 $\overline{\text{CEMG}}$ (Input Pin 170)*1

This pin inputs the emergency stop signal in negative logic. When this pin is low level, all axes stop moving immediately and the chip cannot generate any pulse.

4.17 ELLx, ELLy, ELLz, ELLu (Input pins 171, 172, 173, 174)*1

These pins set the input logic of plus and minus EL signals. Setting these pins at low level makes the input logic positive. Setting them at high level makes the input logic negative.

4.18 +ELx, +ELy, +ELz, +ELu (Input Pins 34, 66, 97, 130)*1, 4

These pins input end limit signals in plus direction. When the pin turns on during operation in plus direction, the chip stops generating pulses to that axis, immediately after deceleration. Select the input logic by setting the ELL pin. The pin status can be checked by reading the sub status (SSTSW).

4.19 –ELx, –ELy, –ELz, –ELu (Input pins 35, 67, 98, 131)*1, 4

These pins input end limit signals in minus direction. When the pin turns on during operation in minus direction, the chip stops generating pulses to that axis, immediately after deceleration. Select the input logic by setting the ELL pin. The pin status can be checked by reading the sub satus (SSTSW).

4.20 SDx, SDy, SDz, SDu (Input Pins 36, 68, 99, 132)*1, 4

These pins input stop-after-deceleration signals in negative logic. The input mode, level or latch can be selected. Also, the input logic can be changed by setting the bits and the pin status can be checked by reading the sub status (SSTSW).

4.21 ORGx, ORGy, ORGz, ORGu (Input Pins 37, 69, 101, 133)*1, 4

These pins input origin signals in negative logic. The origin return signal is detected at the edge. The input logic can be changed by setting the bit and the pin status can be checked by reading the sub status (SSTSW).

4.22 ALMx, ALMy, ALMz, ALMu (Input Pins 38, 70, 102, 134)*1, 4

These pins input alarm signals in negative logic. When the pin turns on, the chip stops generating pulses to that axis immediately after deceleration. The input logic can be changed by setting the bit and the pin status can be checked by reading the sub status (SSTSW).

4.23 OUTx, OUTy, OUTz, OUTu (Output Pins 57, 78, 122, 145)*4

These pins output motor-control command pulses in negative logic. If the chip is placed in the common pulse mode, these pins output pulses in the direction designated by the DIR signal. If the chip is placed in the 2-pulse mode, these pins output pulses in plus direction. The output logic can be changed by setting the bit.

4.24 DIRx, DIRy, DIRz, DIRu (Output Pins 58, 79, 123, 146)*4

These pins output motor-control command pulses or direction signals in negative logic. If the chip is placed in the common pulse, these pins output direction signals. If the chip is placed in the 2-pulse mode, these pins output pulses in negative direction.

4.25 EAx, EBx, EAy, EBy, EAz, EBz, EAu, EBu

(Input Pins 40, 41, 71, 72, 103, 104, 135, 136)*1

These pins input encoder signals for mechanical position control. They can input 90 degree phase difference signals (1, 2 or 4 times multiplied) or plus pulses with EA pins and minus pulses with EB pins. In the case of 90 degree phase difference signals, the counter counts up when the phase of EA signal leads the EB signal. The counting direction can be changed by setting the bit.

4.26 EZx, EZy, EZz, EZu (Input Pins 42, 73, 106, 137)*1, 4

These pins are used in the original return mode. They input marker signals which are output from the encoder at each revolution. Use of EZ signals improves the precision of origin return. The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.27 PAx, PBx, PAy, PBy, PAz, PBz, PAu, PBu

(Input Pins 43, 44, 74, 75, 107, 108, 138, 139)*1

These pins input external pulses from a manual pulser or the like. They can input 90 degree phase difference signals (1, 2 or 4 times multiplied) or plus pulses with PA pins and minus pulses with PB pins. In the case of 90 degree phase difference signals, the counter counts up when the phase of PA signal leads the PB signal. The counting direction can be changed by setting the bit.

4.28 $\overline{\text{PEx}}$, $\overline{\text{PEy}}$, $\overline{\text{PEz}}$, $\overline{\text{PEu}}$ (Input Pins 45, 76, 109, 140)*1

When these pins are low level, the input of PA/PB and +DR/–DR pins are valid. By inputting the axis changeover switch signal, a manual pulser switch can be used commonly for all four axes.

4.29 +DRx, –DRx, +DRy, –DRy, +DRz, –DRz, +DRu, –DRu

(Input Pins 46, 47, 82, 83, 110, 111, 141, 142)*1, 5

These pins enable hard start by connecting an external switch. Operation in a fixed quantity, continuous operation at a constant speed and continuous operation at a varied speed are available from the external switch. The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.30 PCSx, PCSy, PCSz, PCSu (Input Pins 48, 84, 112, 143)*1, 4

These pins input signals to start in-positioning (override of target position 2). The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.31 INPx, INPy, INPz, INPu (Input Pins 49, 85, 113, 150)*1, 4

These pins input the in-positioned signal of the servo driver. The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension (RSTS) register.

4.32 CLRx, CLRy, CLRz, CLRu (Input Pins 50, 86, 114, 151)*1, 4

These pins input the signal to reset a counter or counters selected from among 1 to 4. The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.33 LTCx, LTCy, LTCz, LTCu (Input Pins 51, 87,115, 152)*1, 4

These pins input the signal to latch the value of a counter or counters selected from among 1 to 4. The default negative input logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.34 ERCx, ERCy, ERCz, ERCu (Output Pins 59, 80, 124, 147)*4

These pins output a pulse signal to reset the deviation counter of the servo driver. The default negative output logic can be changed by setting the bit and the pin status can be checked by reading the extension status (RSTS) register.

4.35 $\overline{\text{BSYx}}$, $\overline{\text{BSYy}}$, $\overline{\text{BSYz}}$, $\overline{\text{BSYu}}$ (Output Pins 60, 81, 125, 148)

These pins output low level signals when the chip is generating pulses.

4.36 P0x/FUPx. P0y/FUPy, P0z/FUPz, P0u/FUPu (Input/Output Pins 52, 89, 116, 153)*2, 5

These pins may be used for either general-purpose I/O pins or FUP output pins. If they are set as FUP pins, they output low level signals during acceleration. As general-purpose I/O pins, they can be set as one-shot pulse output terminals besides normal input and output pins. The pin mode can be selected by setting the bits and the output logic of FUP and one-shot pulse can be changed by setting the bits.

4.37 P1x/FDWx, P1y/FDWy, P1z/FDWz, P1u/FDWu

(Input/Output Pins 53, 90, 117, 154)*2, 5

These pins may be used for either general-purpose I/O pins or FDW output pins. If they are set as FDW pins, they output low level signals during deceleration. As general-purpose I/O pins, they can be set as one-shot pulse output terminals besides normal input/output pins. The output logic of FDW and one-shot pulse can be changed by setting the bit.

4.38 P2x/MVCx, P2y/MVCy, P2z/MVCz, P2u/MVCu

(Input/Output Pins 54, 91, 118, 155)*2, 5

These pins may be used for either general-purpose I/O pins or MVC output pins. If they are set as MVC pins, they output low level signals during constant-speed operation. The pin mode can be selected by setting the bit and the MVC output logic can be changed by setting the bit.

4.39 P3x/CP1x (+SLx), P3y/CP1y (+SLy), P3z/CP1z (+SLz), P3u/CP1u (+SLu)

(Input/Output Pins 55, 92, 119, 156)*2, 5

These pins may be used for either general-purpose I/O pins or CP1 (+SL) pins. If they are set as CP1 (+SL), they output the signal when the condition of comparator 1 is being satisfied (in the + soft limit range). The output logic of CP1 (+SL) can be selected by setting the bit and the input or output can be selected by setting the bit.

4.40 P4x/CP2x (–SLx), P4y/CP2y (–SLy), P4z/CP2z (–SLz), P4u/CP2u (–SLu),

(Input/Output Pins 62, 93, 120, 157)*2, 5

These pins may be used for either general-purpose I/O pins or CP2 (–SL) pins. If they are set as CP2 (–SL), they output the signal when the condition of comparator 2 is being satisfied (in the – soft limit range). The output logic of CP2 (–SL) can be selected by setting the bit and the input or output can be selected by setting the bit.

4.41 P5x/CP3x, P5y/CP3y, P5z/CP3z, P5u/CP3u

(Input/Output Pins 63, 94, 126, 158)*2, 5

These pins may be used for either general-purpose I/O pins or CP3 pins. If they are set as CP3, they output the signal when the condition of comparator 3 is being satisfied. The output logic of CP3 can be selected by setting the bit and the input or output can be selected by setting the bit.

4.42 P6x/CP4x, P6y/CP4y, P6z/CP4z, P6u/CP4u

(Input/Output Pins 64, 95, 128, 159)*2, 5

These pins may be used for either general-purpose I/O pins or CP4 pins. If they are set as CP4, they output the signal when the condition of comparator 4 is being satisfied. The output logic of CP4 can be selected by setting the bit and the input or output can be selected by setting the bit.

4.43 P7x/CP5x, P7y/CP5y, P7z/CP5z, P7u/CP5u

(Input/Output Pins 65, 96, 129, 160)*2, 5

These pins may be used for either general-purpose I/O pins or CP5 pins. If they are set as CP5, they output the signal when the condition of comparator 5 is being satisfied. The output logic of CP5 can be selected by setting the bit and the input or output can be selected by setting the bit.

NOTES:

*1. These input pins are equipped with the pull-up resistor (50kΩ to 100kΩ) which prevents them from floating. If they are driven with an open collector, an external pull-up resistor (5kΩ to 10kΩ) is required. Also as a countermeasure against noise, it is recommended to externally pull up unused pins to VDD5 wih 5kΩ to 10kΩ or connect to VDD5 .

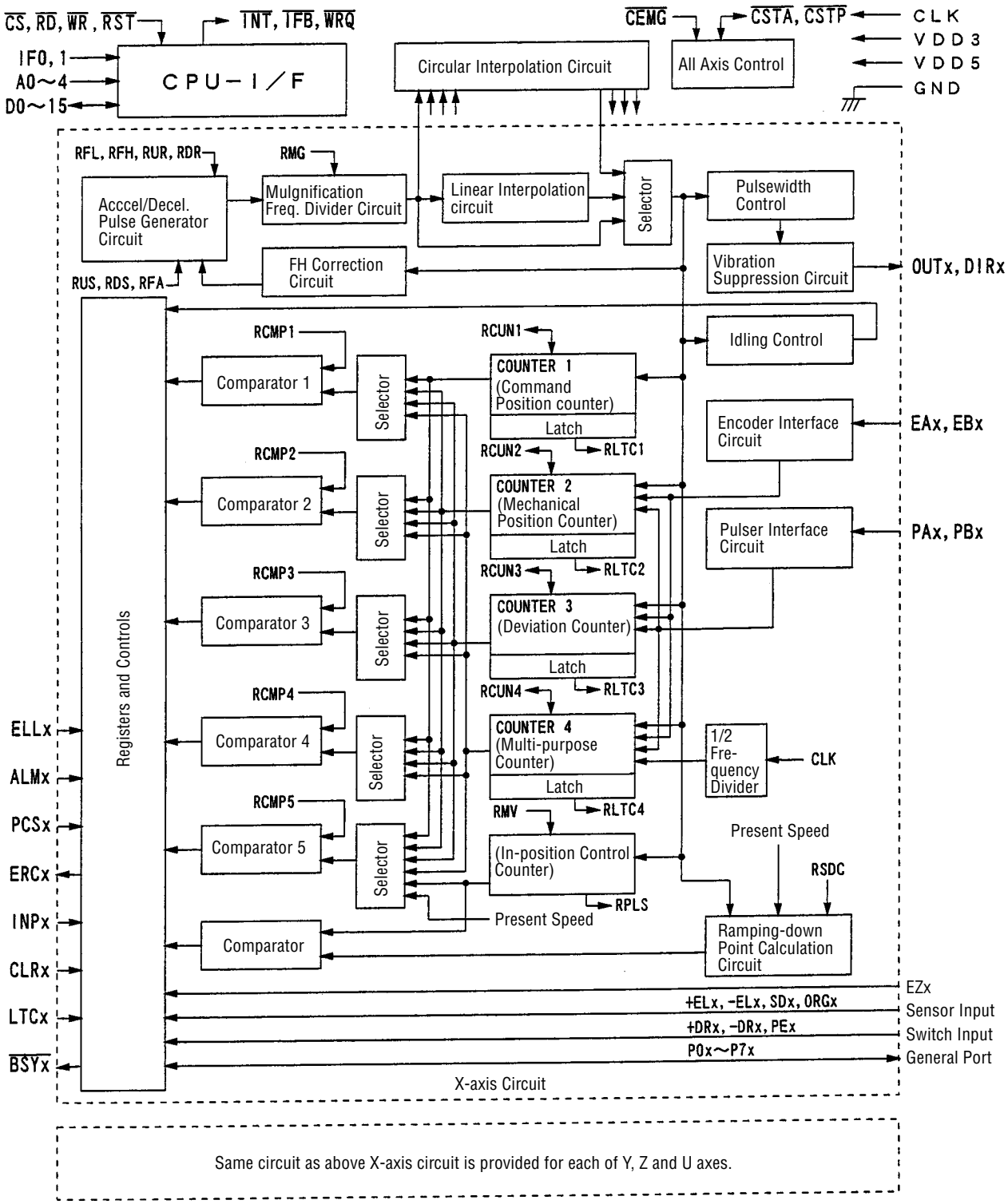
*2 These input/output pins are equipped with the pull-up resistor (50kΩ to 100kΩ) which prevents them from floating. If they are connected in WIRED OR, an external pull-up resistor (5kΩ to 10kΩ) is required. Also as a countermeasure against noise, it is recommended to externally pull up unused pins to VDD5 wih 5kΩ to 10kΩ).

*3. Place unused output pins in open condition.

*4. These pins are set to the negative logic under the default condition. But they can be set to either the negative or positive logic by setting the bits.
Also, the output logic of DIR pins is for the 2-pulse mode.

*5. If pins P0 to P7 are set as output pins, the 8 bits can be simultaneously controlled by writing to the output port (OTPB) or each bit can be individually controlled by writing the output bit control command.
If pins P0 and P1 are set as one-shot pulse output pins, one-shot pulse signal of approximately 26ms can be output by writing the output bit control command.

5. Block Diagram



6. CPU Interface

6.1 Setting to Connected CPU

By setting pins IF0 and IF1, the PCL6045 can connect to one of the following four CPUs.

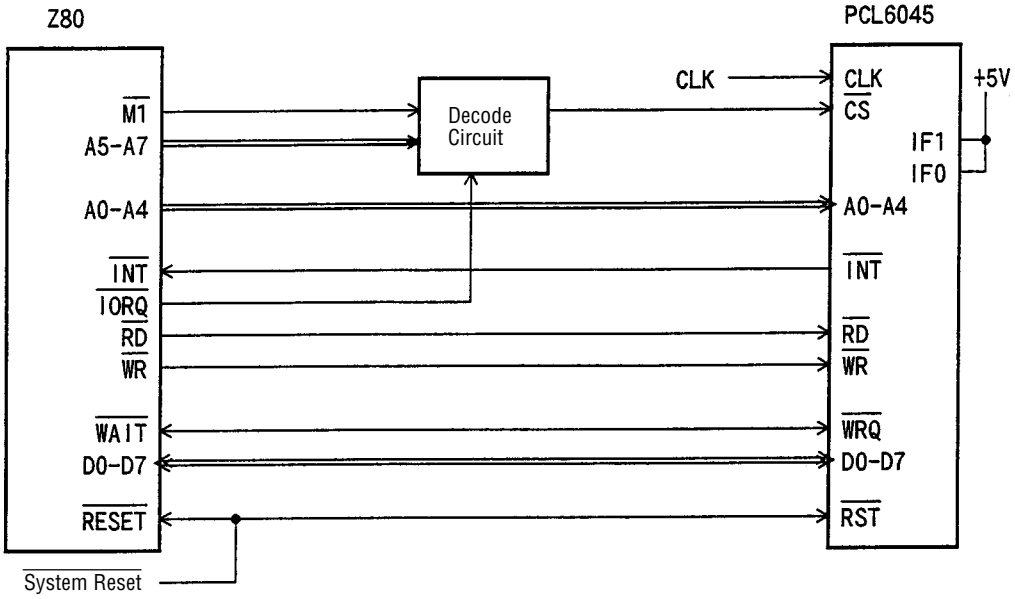
IF1	IF0	CPU	Pins and Connected CPU Signals			
			$\overline{RD}$	$\overline{WR}$	A0	$\overline{WRQ}$
L	L	68000	+5V	R/$\overline{W}$	$\overline{LDS}$	$\overline{DTACK}$
L	H	H8	$\overline{RD}$	$\overline{HWR}$	(GND)	$\overline{WAIT}$
H	L	8086	$\overline{RD}$	$\overline{WR}$	(GND)	READY
H	H	Z80	$\overline{RD}$	$\overline{WR}$	A0	$\overline{WAIT}$

6.2 Precautions in Designing Hardware

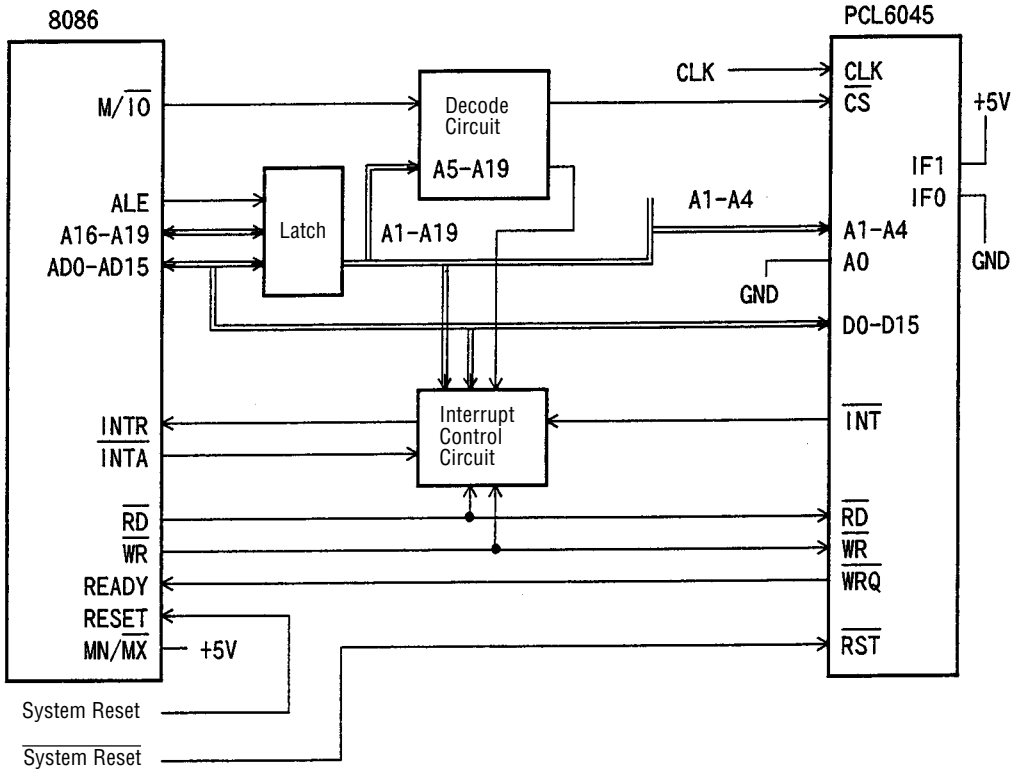
- Input to the CLK pin should be CMOS level.
- The chip should be reset by inputting 8 or more cycles of the CLK signal with the $\overline{RST}$ pin placed in low level.
- Unused pins among P0 to P7 should be externally pulled up to VDD5 with 5kΩ to 10kΩ.
- In the case of connecting the CPU with the 8-bit bus, pins D8 to D15 should be externally pulled up to VDD5 with 5kΩ to 10kΩ. These 8 pins may be pulled up with one resistor.
- The input logic of +EL and –EL signals can be changed by the ELL pin.

6.3 CPU Interface Circuit Block Diagram

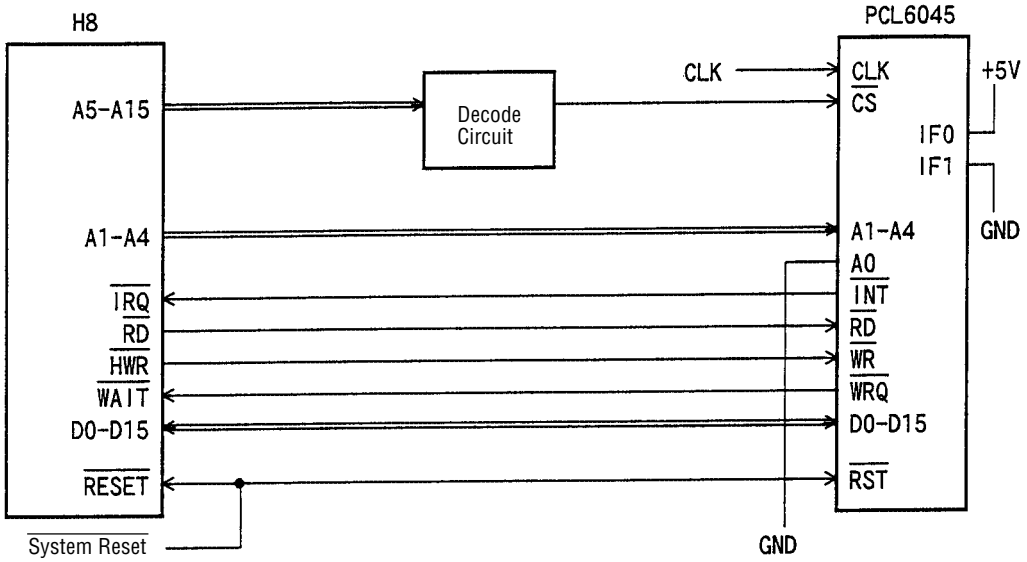
6.3.1 Z80 Interface



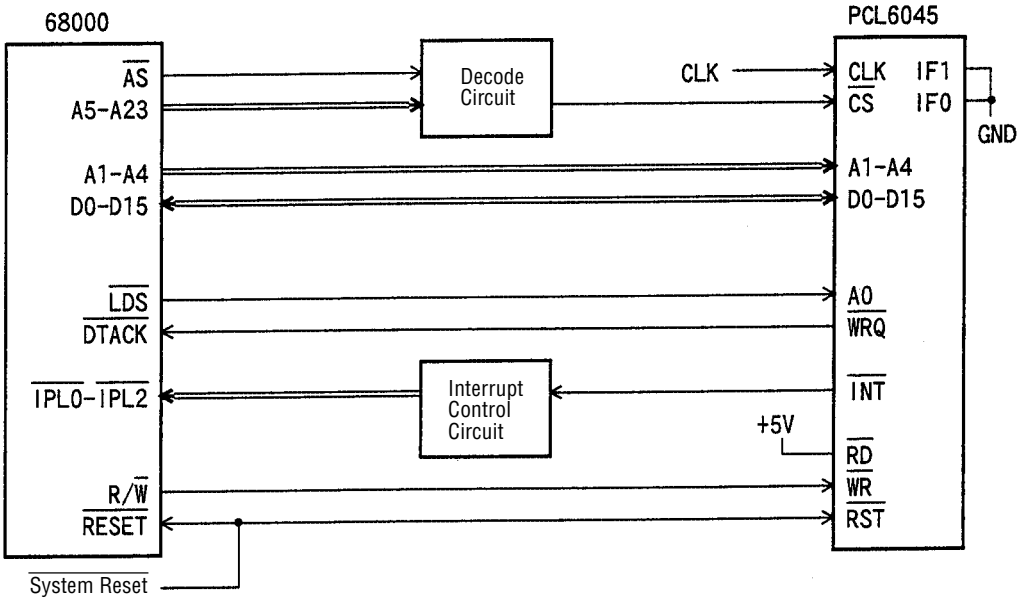
6.3.2 8086 Interface



6.3.3 H8 Interface



6.3.4 68000 Interface



6.4 Address Map

6.4.1 Axis Arrangement Map

With the PCL6045, the address of each axis is independently provided and is selected by inputting the address to pins A4 and A3.

A4	A3	Selected Axis
0	0	X axis
0	1	Y axis
1	0	Z axis
1	1	U axis

6.4.2 Address Map in Each Axis

An address in each axis is defined by writing binary digits to pins A2 and A1 (and A0) as follows:

In the case of Z80 interface

(1) Write Cycle

A2	A1	A0	Mneumonic	Description
0	0	0	COMB0	Writing a control command
0	0	1	COMB1	Designating an axis to execute the control command
0	1	0	OTPB	Changing the general-purpose output port status*
0	1	1		Invalid
1	0	0	BUFB0	Writing to input/output buffer (bits 7 to 0)
1	0	1	BUFB1	Writing to input/output buffer (bits 15 to 8)
1	1	0	BUFB2	Writing to input/output buffer (bits 23 to 16)
1	1	1	BUFB3	Writing to input/output buffer (bits 31 to 24)

*Valid only for bits designated as output

(2) Read Cycle

A2	A1	A0	Mneumonic	Description
0	0	0	MSTSB0	Reading the main status (bits 7 to 0)
0	0	1	MSTSB1	Reading the main status (bits 15 to 8)
0	1	0	IOPB	Reading general-purpose I/O ports
0	1	1	SSTSB	Reading the sub status
1	0	0	BUFB0	Reading from input/output buffer (bits 7 to 0)
1	0	1	BUFB1	Reading from input/output buffer (bits 15 to 8)
1	1	0	BUFB2	Reading from input/output buffer (bits 23 to 16)
1	1	1	BUFB3	Reading from input/output buffer (bits 31 to 24)

In the case of 8086 interface

(1) Write Cycle

A2	A1	Mneumonic	Description
0	0	COMW	Writing the command to a designated axis
0	1	OTPW	Changing the general-purpose output port status*
1	0	BUFW0	Writing to the input/output buffer (bits 15 to 0)
1	1	BUFW1	Writing to the input/output buffer (bits 31 to 16)

*Valid only for bits designated as output

(2) Read Cycle

A2	A1	Mneumonic	Description
0	0	MSTSW	Reading the main status (bits 15 to 0)
0	1	SSTSW	Reading the sub status and general-purpose I/O ports
1	0	BUFW0	Reading from the input/output buffer (bits 15 to 0)
1	1	BUFW1	Reading from the input/output buffer (bits 31 to 16)

In the case of 68000 interface

(1) Write Cycle

A2	A1	Mneumonic	Description
1	1	COMW	Writing the command to a designated axis
1	0	OTPW	Changing the general-purpose output port status*
0	1	BUFW0	Writing to the input/output buffer (bits 15 to 0)
0	0	BUFW1	Writing to the input/output buffer (bits 31 to 16)

*Valid only for bits designated as output

(2) Read Cycle

A2	A1	Mneumonic	Description
1	1	MSTSW	Reading the main status (bits 15 to 0)
1	0	SSTSW	Reading the sub status and general-purpose I/O ports
0	1	BUFW0	Reading from the input/output buffer (bits 15 to 0)
1	0	BUFW1	Reading from the input/output buffer (bits 31 to 16)

6.5 Contents of Map

6.5.1 Writing Command Code by Selecting Axis (COMB0, COMB1)

The COMW (COMB0 and COMB1) is to write a command to let the chip write/read to/from registers or start/stop pulse generation, etc.

COMB0: Set the command code. (Refer to “7. Operation and Control Commands.)

SELu to x: Select the axes for which the command is executed. If all these bits are set at 0, the axis selected by setting A3 and A4 is selected. To write the same command to two or more axes, set the bits at 1. When writing to registers, the contents of input/output buffer will be written in the selected axis. When reading from registers, the contents of registers will be read from the selected axis.

COMW

COMB1 COMB0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	SELu	SELz	SELy	SELx								

6.5.2 Writing to Output Ports (OTPW, OTPB)

The OPTW (OPTB) is to set the condition of output pins of general-purpose I/O pins P0 to P7. Pins designated as input receive no effect. High-place eight bits have no concern at the present. But set them at 0 for possible function change in the future.

OTP7 to 0: Set the condition of output pins P7n to P0n (n = x, y, z or u). If set at 1, the pin outputs high level.

OTPW

OTPB

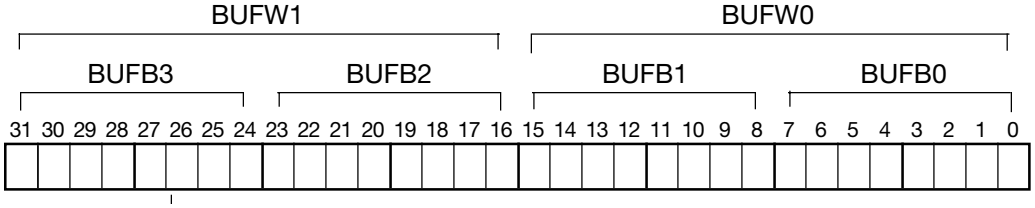
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	OTP7	OTP6	OTP5	OTP4	OTP3	OTP2	OTP1	OTP0

6.5.3 Writing/Reading to/from Input/Output Buffer

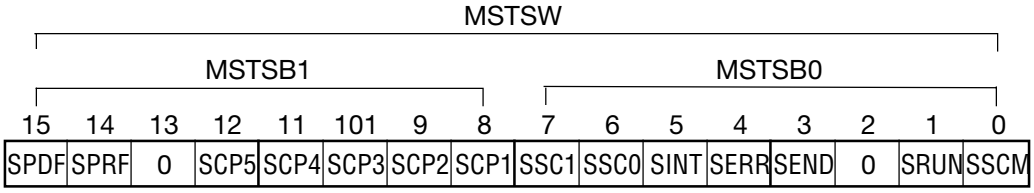
To write data in registers, first write data to the input/output buffer and then write the command to “Write to Register” in the COMB0. The contents in the input/output buffer will be copied to registers.

To read the contents of registers, firstly write the command to “Read from Register.” The contents of registers will be copied to the input/output buffer. Read the data from the input/output buffer.

You may write or read to/from BUFW0 to 1 (BUFB0 to 3) in any desired order.

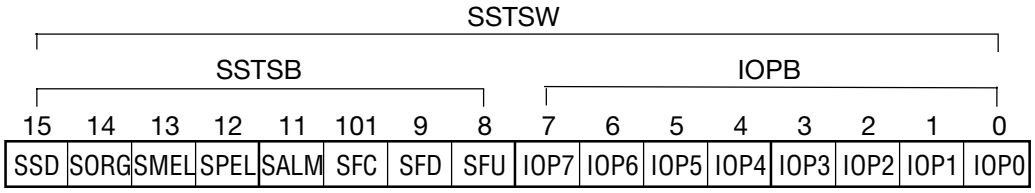


6.5.4 Reading Main Status (MSTSW, MSTSB)



Bit	Name	Description
0	SSCM	Becomes 1 when the start command is written.
1	SRUN	Becomes 1 when generating pulses.
2	Undefined	(Always 0)
3	SEND	Becomes 1 when the chip stops generating pulses.
4	SERR	Becomes 1 at error interrupt and 0 when REST is read.
5	SINT	Becomes 1 at event interrupt and 0 when RIST is read.
6	SSC1	Sequence signal during execution or stop.
7	SSC0	Sequence signal during execution or stop.
8	SCP1	Becomes 1 when the condition of comparator 1 is satisfied.
9	SCP2	Becomes 1 when the condition of comparator 2 is satisfied.
10	SCP3	Becomes 1 when the condition of comparator 3 is satisfied.
11	SCP4	Becomes 1 when the condition of comparator 4 is satisfied.
12	CSP5	Becomes 1 when the condition of comparator 5 is satisfied.
13	Undfined	(Always 0)
14	SPRF	Becomes 1 when the preregister for the next operation is full.
15	SPDF	Becomes 1 when the preregister for comparator 5 is full.

6.5.5 Reading Sub Status and I/O Ports (SSTSW, SSTSB, IOPB)



Bit	Name	Description
0	IOP0	Reads the status of I/O pin 0 (0: Low level, 1: High level).
1	IOP1	Reads the status of I/O pin 1 (0: Low level, 1: High level).
2	IOP2	Reads the status of I/O pin 2 (0: Low level, 1: High level).
3	IOP3	Reads the status of I/O pin 3 (0: Low level, 1: High level).
4	IOP4	Reads the status of I/O pin 4 (0: Low level, 1: High level).
5	IOP5	Reads the status of I/O pin 5 (0: Low level, 1: High level).
6	IOP6	Reads the status of I/O pin 6 (0: Low level, 1: High level).
7	IOP7	Reads the status of I/O pin 7 (0: Low level, 1: High level).
8	SFU	Becomes 1 during acceleration.
9	SFD	Becomes 1 during deceleration.
10	SFC	Becomes 1 during constant-speed operation.
11	SALM	Becomes 1 when ALM pin is on.
12	SPEL	Becomes 1 when +EL pin is on.
13	SMEL	Becomes 1 when –EL pin is on.
14	SORG	Becomes 1 when ORG pin is on.
15	SSD	Becomes 1 when SD pin is on. (SD input latch signal)

7. Operation and Control Commands

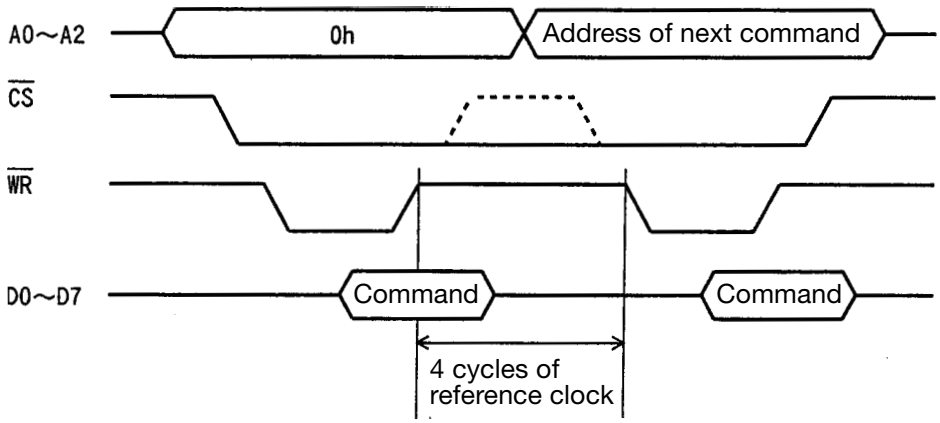
7.1 Operation Commands

You can start the chip generating pulses, stop it or change the speed by writing the command to COMB0 (address 0 in the case of Z80 interface) after writing the axis designation parameter to COMB1 (address 1 in the case of Z80 interface). In the case of 8086, H8 or 68000 interface, write the 16-bit data which include the axis designation and command.

7.1.1 Operation Command Writing Procedure

(In the following description, axis designation is omitted for simplification.)

Write the command to COMB0 (address 0 in the case of Z80 interface). To successively write the next command, you need to wait for four cycles of the reference clock (approximately 0.2µs with the reference clock 19.6608MHz). The $\overline{WRQ}$ pin outputs the wait request signal.



7.1.2 Start Commands

(1) Start Commands

Write the start command during pulse generation in cessation, and the chip will start generating pulses. Write the start command in pulse generation in progress, the command will be used for the next start.

COMB0	Mnemonic	Description
50HEX	STAFL	Starts constant-speed operation at low speed.
51HEX	STAFH	Starts constant-speed operation at high speed.
52HEX	STAD	Starts varied-speed operation 1*1.
53HEX	STAUD	Starts varied-speed operation 2*2.

*1. The chip generates pulses at high speed and stops after deceleration.
*2. The chip starts generating pulses at low speed, accelerates to high speed and stops after deceleration.

(2) Restart Commands

Write the restart command with the chip suspended on the way of in-positioning, and the chip will generate the number of remaining pulses based on the in-position counter.

COMB0	Mnemonic	Description
54_{HEX}	CNTFL	Restarts constant-speed operation at low speed.
55_{HEX}	CNTFH	Restarts constant-speed operation at high speed.
56_{HEX}	CNTD	Restarts varied-speed operation 1*1.
57_{HEX}	CNTUD	Restarts varied-speed operation 2*2.

*1. The chip restarts generating pulses at high speed and stops after deceleration.
*2. The chip restarts generating pulses at low speed, accelerates to high speed and stops after deceleration.

(3) Simultaneous Start Commands

Write the simultaneous start command, and the chip will output pulses to the chip(s) which is (are) placed in the standby status for $\overline{\text{CSTA}}$ signal by setting RMD register.

COMB0	Mnemonic	Description
06_{HEX}	CMSTA	Lets the $\overline{\text{CSTA}}$ pin output one-shot start pulse.
$2A_{HEX}$	SPSTA	Starts the chip only as when receiving $\overline{\text{CSTA}}$ signal.

7.1.3 Speed Change Commands

Write the speed change command when the chip is generating pulses, and the chip will change the pulse output speed. If written during cessation, the command is ignored.

COMB0	Mnemonic	Description
40_{HEX}	FCHGL	Immediately changes to the low speed written in FL register.
41_{HEX}	FCHGH	Immediately changes to the high speed written in FH register.
42_{HEX}	FSCHL	Decelerates to the low speed written in FL register.
43_{HEX}	FSCHH	Accelerates to the high speed written in FH register.

7.1.4 Stop Commands

(1) Stop Commands

Write the stop command when the chip is generating pulses, and the chip will stop generating pulses.

COMB0	Mnemonic	Description
49_{HEX}	STOP	Immediately stops the chip from generating pulses.
$4A_{HEX}$	SDSTP	Stops the chip from generating pulses after decelerating to low speed if written during constant-speed operation at high speed or varied-speed operation. If written during constant-speed operation at low speed, the command immediately stops the chip from generating pulses.

(2) Simultaneous Stop Command

The simultaneous stop command stops the chip(s) of which the $\overline{CSTP}$ pin is made valid by setting RMD register.

COMB0	Mnemonic	Description
07_{HEX}	CMSTP	Lets the $\overline{CSTP}$ pin output one-shot stop pulse.

(3) Emergency Stop Command

The emergency stop command stops the chip from generating pulses.

COMB0	Mnemonic	Description
05_{HEX}	CMEMG	Emergency stop (equivalent to $\overline{CEMG}$ input)

7.1.5 NOP (Invalid) Command

COMB0	Mnemonic	Description
00_{HEX}	NOP	Does not give any effect to operation.

7.2 General-purpose Output Bit Control Commands

Using these commands, you can place general-purpose I/O pins P0 to P7 in high or low level, provided that they are designated as output pins. Writing procedure is the same as for operation commands. Besides these commands, you can set all 8 bits at a time by writing to the general-purpose output port (OTPB: address 2 in the case of Z80 interface).

COMB0	Mnemonic	Description	COMB0	Mnemonic	Description
10_{HEX}	P0RST	Resets P0 to low level.	18_{HEX}	P0SET	Sets P0 at high level.
11_{HEX}	P1RST	Resets P1 to low level.	19_{HEX}	P1SET	Sets P1 at high level.
12_{HEX}	P2RST	Resets P2 to low level.	$1A_{HEX}$	P2SET	Sets P2 at high level.
13_{HEX}	P3RST	Resets P3 to low level.	$1B_{HEX}$	P3SET	Sets P3 at high level.
14_{HEX}	P4RST	Resets P4 to low level.	$1C_{HEX}$	P4SET	Sets P4 at high level.
15_{HEX}	P5RST	Resets P5 to low level.	$1D_{HEX}$	P5SET	Sets P5 at high level.
16_{HEX}	P6RST	Resets P6 to low level.	$1E_{HEX}$	P6SET	Sets P6 at high level.
17_{HEX}	P7RST	Resets P7 to low level.	$1F_{HEX}$	P7SET	Sets P7 at high level.

By setting RENV2 (environmental setting 2) register, P0 and P1 can be set for one-short output (T = approx. 26ms) and the output logic can changed. To set P0 pin for one-shot output, set P0M (bits 1 and 0) to 11 and to set P1 pin for one-shot output, set P1M (bits 3 and 2) to 11. To change the output logic of P0 pin, use P0L (bit 16) and to change that of P1 pin, use P1L (bit 17).

To let P0 and P1 pins output one-shot pulse, you need to write the bit control command which differs depending on the output logic as follows:

Pin	Logic Setting	Bit Control Command
P0	Negative logic (P0L=0)	P0RST (10_{HEX})
	Positive logic (P0L=1)	P0SET (18_{HEX})
P1	Negative logic (P1L=0)	P1RST (11_{HEX})
	Positive logic (P1L=1)	P1SET (19_{HEX})

Note that writing to the output port (OTPB: address 2 in the case of Z80 interface) does not affect P0 and P1 pins.

7.3 Control Commands

Control commands are provided for various purposes such as resetting counters. Writing procedure is the same as for operation commands.

7.3.1 Software Reset Command

This command resets the chip.

COMB0	Mnemonic	Description
04HEX	SRST	Software reset (same function as setting $\overline{\text{RST}}$ pin at low level)

7.3.2 Counter Reset Commands

These commands reset counters to 0.

COMB0	Mnemonic	Description
20HEX	CUN1R	Resets counter 1 (command position counter).
21HEX	CUN2R	Resets counter 2 (mechanical position counter).
22HEX	CUN3R	Resets counter 3 (deviation counter).
23HEX	CUN4R	Resets counter 4 (multi-purpose counter).

7.3.3 ERC Output Control Commands

ERC signal can be controlled using these commands.

COMB0	Mnemonic	Description
24HEX	ERCOUT	Outputs ERC signal.
25HEX	ERCRST	Resets ERC output when it is set for level output.

7.3.4 Preregister Control Commands

Parameters written in preregisters can be cancelled or shifted to registers using these commands.

COMB0	Mnemonic	Description
26HEX	PRICAN	Cancels parameters written in preregisters for operation.
27HEX	PCPCAN	Cancels parameters written in RCMP5 preregister.
2BHEX	PRISHF	Shifts parameters from preregisters to registers for operation.
2CHEX	PCPSHF	Shifts parameters from RCMP5 preregister to RCMP5 register.

7.3.5 PCS Input Command

This command causes the same effect as PCS input = ON.

COMB0	Mnemonic	Description
28HEX	STAON	Starts in-positioning.

7.3.6 LTC Input (Counter Latch) Command

This command causes the same effect as LTC input = ON.

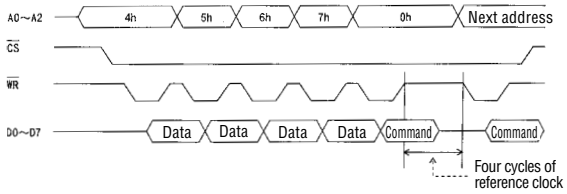
COMB0	Mnemonic	Description
29HEX	LTCH	Latches the value of counter.

7.4 Register Control Commands

By writing register control commands to COMB0 (address 0 in the case of Z80 interface), data are copied between registers and the input/output buffer. If the input/output bufffer is used for the interrupt processing program, you need to read the contents of input/output buffer in advance and to return them to the input/output buffer after using it for the interrupt processing program.

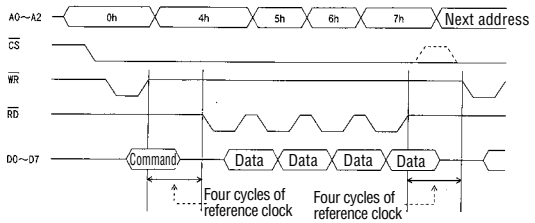
7.4.1 Writing Data to Registers

In the following description, axis designation is omitted for simplification. Firstly write data to the input/output buffer (addresses 4 to 7 in the case of Z80 interface) in any desired order. Then write the “register write command ” to COMB0 (address 0 in the case of Z80 interface). If you wish to send the next command, you need to put a waiting time of four cycles of reference clock (approx. 0.2µs with reference clock 19.6608MHz). $\overline{\text{WRQ}}$ pin outputs the wait request signal.



7.4.2 Reading Data from Register

In the following description, axis designation is omitted for simplification. Write the “register read command” to COMB0 (address 0 in the case of Z80 interface). Wait until data are copied to the input/output buffer. A waiting time of four cycles of reference clock (approx. 0.2µs with reference clock 19.6608MHz) is required. Then, read data from the input/output buffer (addresses 4 to 7 in the case of Z80 interface) in any desired order. If you wish to write the next command, you need to put a waiting time of four cycles of reference clock. $\overline{\text{WRQ}}$ pin outputs the wait request signal.



7.4.3 List of Register Control Commands

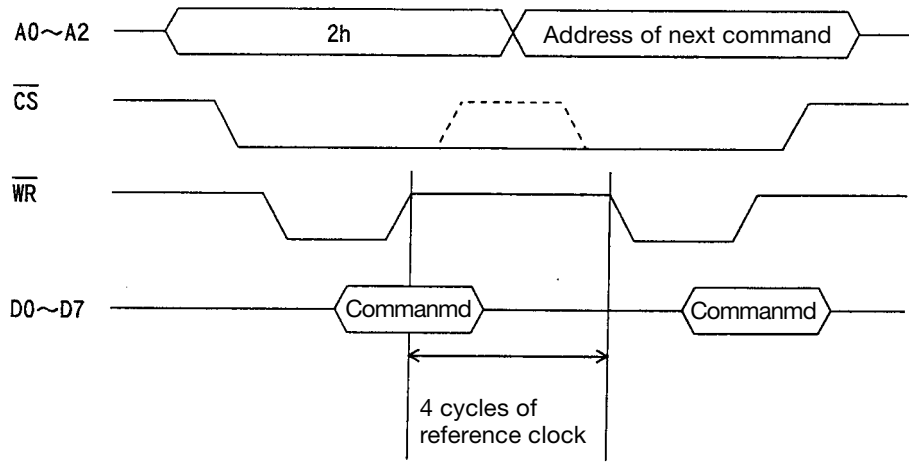
No.	Register	Content	Read Command		Write Command		2nd Preregister	Read Command		Write Command	
			COMB0	Mnemonic	COMB0	Mnemonic		COMB0	Mnemonic	COMB0	Mnemonic
1	RMV	Moving amount/target position	D0HEX	RRMV	90HEX	WRMV	PRMV	C0HEX	RPRMV	80HEX	WPRMV
2	RFL	Initial speed	D1HEX	RRFL	91HEX	WRFL	PRFL	C1HEX	RPRFL	81HEX	WPRFL
3	RFH	Operation speed	D2HEX	RRFH	92HEX	WRFH	PRFH	C2HEX	RPRFH	82HEX	WPRFH
4	RUR	Acceleration rate	D3HEX	RRUR	93HEX	WRUR	PRUR	C3HEX	RPRUR	83HEX	WPRUR
5	RDR	Deceleration rate	D4HEX	RRDR	94HEX	WRDR	PRDR	C4HEX	RPRDR	84HEX	WPRDR
6	RMG	Speed multiplication	D5HEX	RRMG	95HEX	WRMG	PRMG	C5HEX	RPRMG	85HEX	WPRMG
7	RDP	Ramping-down point	D6HEX	RRDP	96HEX	WRDP	PRDP	C6HEX	RPRDP	86HEX	WPRDP
8	RMD	Operation mode	D7HEX	RRMD	97HEX	WRMD	PRMD	C7HEX	RPRMD	87HEX	WPRMD
9	RIP	Center of circular interpolation	D8HEX	RRDP	98HEX	WRDP	PRIP	C8HEX	RPRDP	88HEX	WPRDP
10	RUS	S-curve section of acceleration	D9HEX	RRUS	99HEX	WRUS	PRUS	C9HEX	RPRUS	89HEX	WPRUS
11	RDS	S-curve section of deceleration	DAHEX	RRDS	9AHEX	WRDS	PRDS	CAHEX	RPRDS	8AHEX	WPRDS
12	RFA	Moving amount correction speed	DBHEX	RRFA	9BHEX	WRFA					
13	RENV1	Environmental setting 1	DCHEX	RRENV1	9CHEX	WRENV1					
14	RENV2	Environmental setting 2	DDHEX	RRENV2	9DHEX	WRENV2					
15	RENV3	Environmental setting 3	DEHEX	RRENV3	9EHEX	WRENV3					
16	RENV4	Environmental setting 4	DFHEX	RRENV4	9FHEX	WRENV4					
17	RENV5	Environmental setting 5	E0HEX	RRENV5	A0HEX	WRENV5					
18	RENV6	Environmental setting 6	E1HEX	RRENV6	A1HEX	WRENV6					
19	RENV7	Environmental setting 7	E2HEX	RRENV7	A2HEX	WRENV7					
20	RCUN1	Counter 1 (command position)	E3HEX	RRCUN1	A3HEX	WRCUN1					
21	RCUN2	Counter 2 (mechanical position)	E4HEX	RRCUN2	A4HEX	WRCUN2					
22	RCUN3	Counter 3 (deviation)	E5HEX	RRCUN3	A5HEX	WRCUN3					
23	RCUN4	Counter 4 (multi-purpose)	E6HEX	RRCUN4	A6HEX	WRCUN4					
24	RCMP1	Comparator 1 data	E7HEX	RRCMP1	A7HEX	WRCMP1					
25	RCMP2	Comparator 2 data	E8HEX	RRCMP2	A8HEX	WRCMP2					
26	RCMP3	Comparator 3 data	E9HEX	RRCMP3	A9HEX	WRCMP3					
27	RCMP4	Comparator 4 data	EAHEX	RRCMP4	AAHEX	WRCMP4					
28	RCMP5	Comparator 5 data	EBHEX	RRCMP5	ABHEX	WRCMP5	PRCP5	CBHEX	RPRCP5	8BHEX	WPRCP5
29	RIRQ	Event INT setting	ECHEX	RRIRQ	ACHEX	WRIRQ					
30	RLTC1	Counter 1 latch data	EDHEX	RRLTC1							
31	RLTC2	Counter 2 latch data	EEHEX	RRLTC2							
32	RLTC3	Counter 3 latch data	EFHEX	RRLTC3							
33	RLTC4	Counter 4 latch data	F0HEX	RRLTC4							
34	RSTS	Extension status	F1HEX	RRSTS							
35	REST	Error INT status	F2HEX	RREST							
36	RIST	Event INT status	F3HEX	RRIST							
37	RPLS	In-poisitioning counter	F4HEX	RRPLS							
38	RSPD	EZ counter/speed monitor	F5HEX	RRSPD							
39	RSDC	Ramping-down point	F6HEX	RRSDC							
40	RIPS	Interpolation status	FFHEX	RRIPS							

7.5 General-purpose Output Control Command

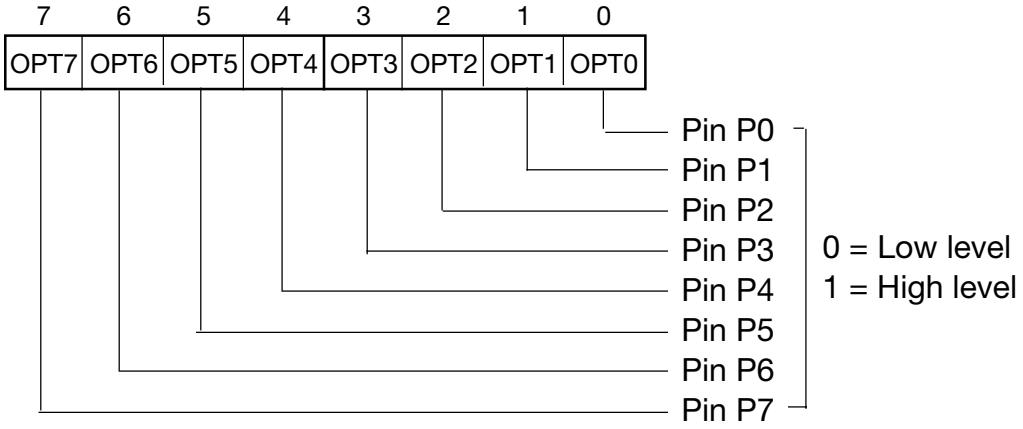
Control the output of pins P0 to P7 by writing the output control command to the output port (address 2 in the case of Z80 interface). The bits corresponding to the pins which are designated as input are ignored if the command is written. Though the high-place 8 bits are invalid, set them at 0 for function change in the future. Also, note that the setting here is kept for the pins which are designated as input.
To set each pin individually, use the bit control command.

7.5.1 Command Writing Procedure

Write the command to the output port (address 2 in the case of Z80 interface). If you wish to send the next command successively, put a waiting time of four cycles of reference clock (approx. 0.2µs with reference clock 19.6608MHz). $\overline{WRQ}$ pin outputs the wait request signal.



7.5.2 Command Bits and Output Pins



8. Registers

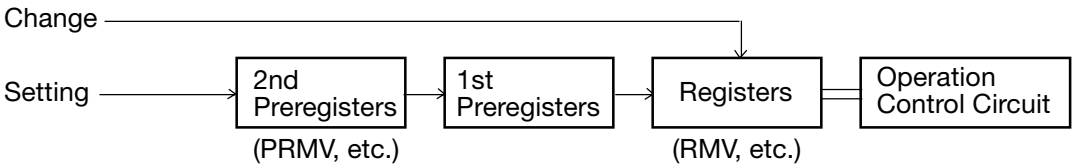
8.1 List of Registers

The following registers are provided for each individual axis.

No.	Name	Bit Length	R/W	Description	2nd Preregister
1	RMV	28	R/W	Moving amount/target position	PRMV
2	RFL	16	R/W	Initial speed	PRFL
3	RFH	16	R/W	Operation speed	PRFH
4	RUR	16	R/W	Acceleration rate	PRUR
5	RDR	16	R/W	Deceleration rate	PRDR
6	RMG	12	R/W	Speed multiplication	PRMG
7	RDP	24	R/W	Ramping-down point	PRDP
8	RMD	27	R/W	Operation mode	PRMD
9	RIP	28	R/W	Center position of circular interpolation/moving amount of main axis with linear interpolation between multiple axis	PRIP
10	RUS	15	R/W	S-curve section of acceleration	PRUS
11	RDS	15	R/W	S-curve section of deceleration	PRDS
12	RFA	16	R/W	Moving amount correction speed	
13	RENV1	32	R/W	Environmental setting register 1 (I/O pin spec)	
14	RENV2	27	R/W	Environmental setting register 2 (universal port spec)	
15	RENV3	32	R/W	Environmental setting register 3 (origin return/counter spec)	
16	RENV4	32	R/W	Environmental setting register 4 (comparators 1-4 spec)	
17	RENV5	22	R/W	Environmental setting register 5 (comparator 4 spec)	
18	RENV6	32	R/W	Environmental setting register 6 (moving amount correction)	
19	RENV7	32	R/W	Environmental setting register 7 (vibration suppress control)	
20	RCUN1	28	R/W	Counter 1 (command position counter)	
21	RCUN2	28	R/W	Counter 2 (mechanical position counter)	
22	RCUN3	16	R/W	Counter 3 (deviation counter)	
23	RCUN4	28	R/W	Counter 4 (multi-purpose counter)	
24	RCMP1	28	R/W	Comparator 1 data	
25	RCMP2	28	R/W	Comparator 2 data	
26	RCMP3	28	R/W	Comparator 3 data	
27	RCMP4	28	R/W	Comparator 4 data	
28	RCMP5	28	R/W	Comparator 5 data	PRCP5
29	RIRQ	19	R/W	Setting event interrupt factor	
30	RLTC1	28	R	Counter 1 (command position) latched data	
31	RLTC2	28	R	Counter 2 (mechanical position) latched data	
32	RLTC3	16	R	Counter 3 (deviation) latched data	
33	RLTC4	28	R	Counter 4 (multi-purpose) latched data	
34	RSTS	17	R	Extension status	
35	REST	18	R	Error INT status	
36	RIST	20	R	Event INT status	
37	RPLS	28	R	In-position counter (number of remaining pulses)	
38	RSPD	23	R	EZ counter/present speed monitor	
39	RSDC	24	R	Automatically calculated ramping-down point value	
40	RIPS	24	R	Interpolation status	

8.2 Preregisters

Preregisters are provided for registers RMV, RFL, RFH, RUR, RDR, RMG, RDP, RMD, RIP, RUS, RDS and RCMP5 and for the start command. Preregisters enable condition setting for the next operation. The preregisters of PCL6045 are configured in two stages as shown below and operate in FIFO mode.



Usually, operation data are written in 2nd preregisters. To change data such as speed for the present operation, the new data are written to registers. Data are transferred (copied) from 2nd preregisters to 1st preregisters and from 1st preregisters to registers when the start command is written or when operation is complete.

8.2.1 Operation Flow

(1) Write data to 2nd preregisters with 2nd and 1st preregisters under blank condition. Data will be written in 2nd preregisters, 1st preregisters and registers.
(2) Write the start command. The chip will operate according to parameters written in registers and 1st preregisters will be empty.
(3) Write next operation parameters to 2nd preregisters. (If the data is the same as previous step, then this step may be omitted.) The next operation data will be written in 2nd and 1st preregisters since 1st preregisters are empty.
(4) Write the start command for the next operation. The 1st preregisters will be placed in data holding condition.
(5) Write data for the operation after the next one to the 2nd preregisters. Data will be written in the 2nd preregisters only since 1st preregisters are in data holding condition.
(6) Write the start command for the operation after the next one. The 2nd preregisters will also be placed in data holding condition.
(7) When the first operation is complete, data is transferred from 2nd to 1st preregisters and from 1st preregisters to registers and the second operation will start according to the data.
(8) Since data of 2nd preregisters are transferred to 1st preregisters, 2nd preregisters are empty, thereby allowing you to write data anew to 2nd preregisters.

You can check whether all preregisters including 2nd ones are in data full condition or not by reading the main status (MSTSW). Also, you can set $\overline{\text{RIRQ}}$ (event interrupt factor) register so that $\overline{\text{INT}}$ signal is output when com-

pletion of operation makes 2nd preregisters empty.

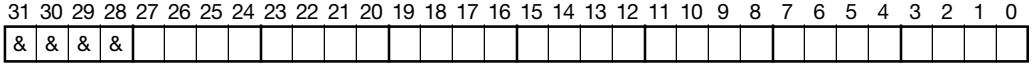
NOTE: To automatically start the next operation using preregisters, set the operation completion timing to “completion of cycle” (METM of RMD = 0). If you set it to “completion of pulse (METM of rmd = 0), the distance between the last pulse and the next operation’s start pulse is as narrow as 14 x T_{CLK} (reference clock cycle). For details, refer to “11-3-2 Output Pulsewidth Control and Operation-Comple Timing.”

8.3 Explanation of Registers

Under the default condition, all registers and preregisters are set at 0. Take care that in some case 0 is beyond the setting range for certain registers.

8.3.1 RMV (PRMV) Register

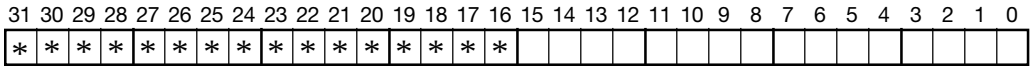
This register sets the relative target position in in-positioning operation. PRMV is the 2nd preregister for RMV register.



Setting range is –134,217,728 to +134,217,727.
A new moving amount can be overidden by changing data of RMV register during operation.

8.3.2 RFL (PRFL) Register

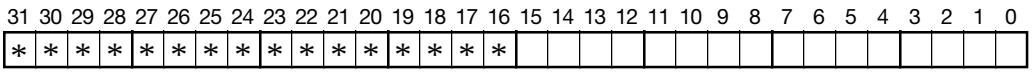
This register sets the speed at the time of the start (and stop) of varied-speed operation with acceleration and deceleration at the start and stop. PRFL is the 2nd preregister for RFL register.



Setting range is 1 to 65,535. However, the practical speed (pps) depends on the speed multiplication written in RMG register.

8.3.3 RFH (PRFH) Register

This register sets the operation speed. PRFH is the 2nd preregister for RFH register.

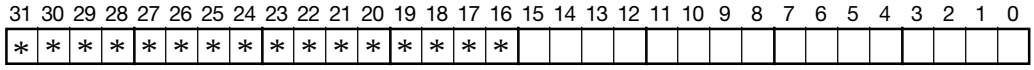


Setting range is 1 to 65,535. However, the practical speed (pps) depends on the speed multiplication written in RMG register.

NOTES: 1. Bits in which * is put are ignored in writing and become 0 when reading.
2. Bits in which & is put are ignored in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.4 RUR (PRUR) Register

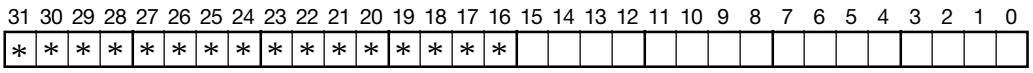
This register sets the acceleration rate. PRUR is the 2nd preregister for RUR register.



Setting range is 1 to 65,535.

8.3.5 RDR (PRDR) Register

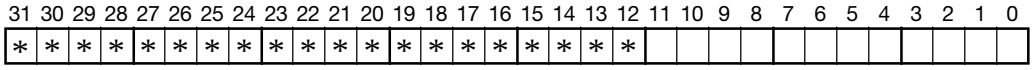
This register sets the deceleration rate. PRDR is the 2nd preregister for RDR register.



Setting range is 1 to 65,535. If this register is set at 0, the deceleration rate is as set by RUR register (acceleration rate register).

8.3.6 RMG (PRMG) Register

This register sets the speed multiplication. PRMG is the 2nd preregister for RMG register.



Setting range is 2 to 4,095. The multiplication written here is used to mutliply the values written in RFL, RFH and RFA registers for practical operation.

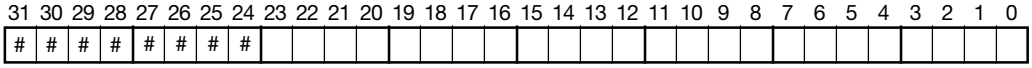
Setting samples with reference clock = 19.6608MHz

Setting Value	Multiplication	Operating Speed Setting Range
2999	0.1x	0.1 to 6,553.5
1499	0.2x	0.2 to 13,107.0
599	0.5x	0.5 to 32,767.5
299	1x	1 to 65,535
149	2x	2 to 131,070
59	5x	5 to 327,675
29	10x	10 to 655,350
14	20x	20 to 1,310,700
5	50x	50 to 3,276,750
2	100x	100 to 6,553,500

NOTES: 1. Bits in which * is put are ignored in writing and become 0 when reading.
2. Bits in which & is put are ignored in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.7 RDP (PRDP) Register

This register sets the ramping-down point (starting point of deceleration) in in-positioning. PRDP is the 2nd preregister for RDP register.



Bits in which # is put are ignored when writing and, when reading, they change depending on setting of MSDP (bit 13) of RMD register.

MSDP	Setting Content	# bits
0	Offset for automatic setting value. Early deceleration when the value is positive and late deceleration when the value is negative.	Same as bit 23
1	Deceleration starts when the remaining amount becomes lower than setting value.	0

NOTES: 1. Bits in which ∗ is put are ignored in writing and become 0 when reading.
2. Bits in which & is put are ignored in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.8 RMD (PRMD) Register

This register sets the operation mode. PRMD is the 2nd preregister for RMD register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIPF	MPCS	MSDP	METM	MCCE	MSMD	MINP	MSDE	0	MOD	MOD	MOD	MOD	MOD	MOD	MOD

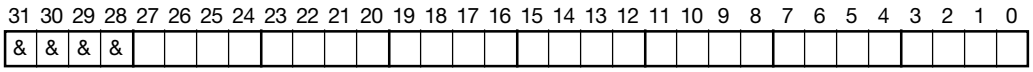
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	MADJ	MSP0	MSPE	MAX3	MAX2	MAX1	MAX0	MSY1	MSY0	MSN1	MSN0

Bit	Name	Description
Basic Operation Mode Setting		
6-0	MOD	000 0000 (00HEX): Continuous operation in plus direction under command control 000 1000 (08HEX): Continuous operation in minus direction under command control 000 0001 (01HEX): Continuous operation through pulser (PA/PB) input 000 0010 (02HEX): Continuous operation through external signal (+DR/–DR) input 001 0000 (10HEX): Origin return in plus direction 001 1000 (18HEX): Origin return in minus direction 001 0010 (12HEX): Origin escape in plus direction 001 1010 (1AHEX): Origin escape in minus direction 001 0101 (15HEX): Origin search in plus direction 001 1101 (1DHEX): Origin search in minus direction 010 0000 (20HEX): Moving to +EL or +SL position 010 1000 (28HEX): Moving to –EL or –SL position 010 0010 (22HEX): Escape from –EL or –SL 010 1010 (2AHEX): Escape from +EL or +SL 010 0100 (24HEX): Moving in plus direction by EZ count 010 1100 (2CHEX): Moving in minus direction by EZ count 100 0001 (41HEX): In-positioning (designating target relative position) 100 0100 (44HEX): Command position (counter 1) 0 return 100 0101 (45HEX): Mechanical position (counter 2) 0 return 100 0110 (46HEX): One pulse in plus direction 100 1110 (4EHEX): One pulse in minus direction 100 0111 (47HEX): Timer operation 101 0001 (51HEX): In-positioning through pulser (PA/PB) input 101 0100 (54HEX): Command position 0 return through pulser (PA/PB) input 101 0101 (55HEX): Mechanical position 0 return through pulser (PA/PB) input 101 0110 (56HEX): In-positioning through external signal (+DR/–DR) input 110 0000 (60HEX): Continuous linear interpolation 1 (continuous operation with L.I.1) 110 0001 (61HEX): Linear interpolation 1 110 0010 (62HEX): Continuous linear interpolation 2 (continuous operation with L.I.2) 110 0011 (63HEX): Linear interpolation 2 110 0100 (64HEX): Circular interpolation in CW direction 110 0101 (65HEX): Circulator interpolation in CCW direction
7	Undefined	(Always set this bit at 0.)

Bit	Name	Description
Optional Setting		
8	MSDE	1: Deceleration (deceleration-stop) with SD input ON
9	MINP	1: Completion of operation with INP input ON
10	MSMD	0: Linear accel/decel, 1: S-curve accel/decel
11	MCCE	1: Suspends counter 1 (command position). Use this when you wish to move the mechanism without changing control position.
12	METM	Operation completion timing (0: Completion of cycle, 1: Completion of pulse). Select completion of pulse when using the vibration suppression function.
13	MSDP	Ramping-down point setting method (0: Automatic, 1: Manual) Effective for in-positioning and linear interpolation
14	MPCS	1: Controls the number of pulses from PCS input = ON for in-positioning (target position override 2)
15	MIPF	1: Makes composite speed constant in interpolation.
17-16	MSN1-2	Set 2-bit sequence to control operation block. The sequence number (SSC1 to 0) can be checked by reading the main status (MSTSW). Setting the sequence number does not give any effect to operation.
19-18	MSY1-0	Starts in synchronization at the following timing after writing the start command. 00: Immediately starts. 01: Starts upon $\overline{\text{CSTA}}$ input (or command 08 or $2A_{HEX}$). 10: Starts with internal synchronization signal. 11: Starts upon stop of a designated axis.
23-20	MAX3-0	Selects the axis to check the stop when MSY1-0 = 11. e.g. 0001: Starts upon stop of X axis 0010: Starts upon stop of Y axis 0100: Starts upon stop of Z axis 1000: Starts upon stop of U axis 0101: Starts when both X and Z axes stop. 1111: Starts when all axes stop.
24	MSPE	1: Deceleration-stop or immediate stop by $\overline{\text{CSTP}}$ input. Use this to stop in the occasion of abnormal stop of other axis.
25	MSPO	1: Outputs $\overline{\text{CSTP}}$ (simultaneous stop) at abnormal stop of any axis.
26	MADJ	FH correction function (0: ON, 1: OFF). Set FH correction function to ON when interpolation control is done.
31-27	Undefined	(Always set these bits at 0.)

8.3.9 RIP (PRIP) Register

This register sets the the center position of circular interpolation or the moving amount of main axis with linear interpolation 2. PRIP is the 2nd preregister for RIP register.



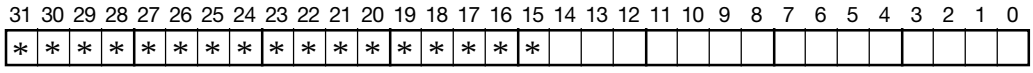
The setting is valid when MOD (bits 6 to 0) of RMD register is set to any of the following:

110 0010 (62_{HEX}): Continuous linear interpolation 2 (continuous operation with linear interpolation 2)
110 0011 (63_{HEX}): Linear interpolation 2
110 0100 (64_{HEX}): Circular interpolation in CW direction
110 0101 (65_{HEX}): Circular interpolation in CCW direction

Set the moving amount of main axis with a relative value when continuous linear interpolation 2 or linear interpolation 2 is selected.
Set the circular center position with a relative value when the circular interpolation is selected.
Setting range is –134,217,727 to +134,217,727.

8.3.10 RUS (PRUS) Register

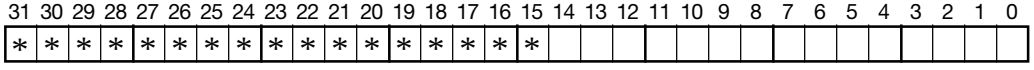
This register sets the S-curve section of S-curve acceleration. PRUS is the 2nd preregister for RUS register.



Setting range is 1 to 32,767. If it is set at 0, the S-curve section is internally calculated using an equation of (RFH – RFL)/2.

8.3.11 RDS (PRDS) Register

This register sets the S-curve section of S-curve deceleration. PRDS is the 2nd preregister for RDS register.



Setting range is 1 to 32,767. If it is set at 0, the S-curve section is internally calculated using an equation of (RFH – RFL)/2.

NOTES: 1. Bits in which * is put are ignored in writing and become 0 when reading.
2. Bits in which & is put are ignored in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.12 RFA Register

This register sets the constant speed for backlash correction or slip correction. The setting is also used as a reversion constant speed for origin return.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																

Setting range is 1 to 65,535. Note, however, that the practical speed (pps) depends on the magnification written in RMG register.

8.3.13 RENV1 Register

This is the register for environmental setting 1, which sets mainly the functions of input/output pins.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERCL	EPW2	EPW1	EPW0	EROR	EROE	ALML	ALMM	ORGL	SDL	SDLT	SDM	ELM	PMD2	PMD1	PMD0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PDTC	PCSM	INTM	DTMF	DRF	FLTR	DRL	PCSL	LTCL	INPL	CLR1	CLR0	STPM	STAM	ETW1	ETW0

Bit	Name	Description				
2-0	PMD2-0	Set the function of output pulse.				
		PMD2-0	Operation in plus direction		Operation in minus direction	
			OUT pin	DIR pin	OUT pin	DIR pin
		000		(High)		(Low)
		001		(High)		(Low)
		010		(Low)		(High)
		011		(Low)		(High)
		100		(High)	(High)	
		111		(Low)	(Low)	
3	ELM	Sets processing mode at EL input ON. (0: Immediate stop, 1: Deceleration stop)*1				
4	SDM	Sets processing mode at SD input ON (0: Deceleration only, 1: Stop after deceleration)				
5	SDLT	Sets SD input latch function (0: OFF, 1: ON). Set it to ON when the SD signal width is short. If SD input is off at the start, the latch signal is reset. Also, the latch signal is reset by setting SDLT = 0.				
6	SDL	Sets SD signal input logic (0: Negative, 1: Positive)				

Bit	Name	Description
7	ORGL	Sets ORG signal input logic (0: Negative, 1: Positive)
8	ALMM	Sets processing mode at ALM input ON. (0: Immediate stop, 1: Stop after deceleration)*2
9	ALML	Sets ALM signal input logic (0: Negative, 1: Positive)
10	EROE	1: Automatically outputs ERC signal when +EL, –EL, ALM or $\overline{\text{CEMG}}$ signal immediately stops pulse output. However, ERC signal is not output at the time of stop-after-deceleration. ERC signal is output if EL stop is made normal stop by setting MOD of RMD register to 010 X000 (moving to EL position).
11	EROR	1: Automatically outputs ERC signal at the time of completion of origin return.
14-12	EPW2-0	Set the pulsewidth of ERC output signal. 000: 12µs 011: 1.6ms 110: 104ms 001: 102µs 100: 13ms 111: Level output 010: 409µs 101: 52ms
15	ERCL	Sets ERC signal output logic. (0: Negative, 1: Positive)
17-16	ETW1-0	Set OFF time of ERC signal. 00: 0µs 10: 1.6ms 01: 12µs 11: 104ms
18	STAM	Sets the trigger mode of $\overline{\text{CSTA}}$ signal. (0: Level trigger, 1: Edge trigger)
19	STPM	Sets the $\overline{\text{CSTP}}$-initiated stop mode. (0: Immediate stop, 1: Stop after deceleration)
21-20	CLR1-0	Sets CLR-initiated clear mode. 00: Clears at the falling edge 10: Clears at low level 01: Clears at the rising edge 11: Clears at high level
22	INPL	Sets INP signal input logic. (0: Negative, 1: Positive)
23	LTCL	Sets LTC signal operating edge. (0: Falling edge, 1: Rising edge)
24	PCSL	Sets PCS signal input logic. (0: Negative, 1: Positive)
25	DRL	Sets +DR/–DR signal input logic. (0: Negative, 1: Positive)
26	FLTR	1: Inserts a filter to +EL, –EL, SD, ORG, ALM and INP inputs. When the filter is inserted, signals with a pulsewidth of shorter than 4µs are disregarded.
27	DRF	1: Inserts a filter to +DR, –DR and PE inputs. When the filter is inserted, signals with a pulsewidth of shorter than 3.2ms are disregaded.
28	DTMF	1: Sets the direction change timer (0.2ms) function to OFF.
29	INTM	1: Masks INT output (interrupt circuit changes).
30	PCSM	1: Makes PCS input the CSTA signal for that chip only.
31	PDTC	1: Sets the pulsewidth at duty 50% at all times.

*1. If the processing mode at the time of EL input ON is set for “stop after deceleration” (ELM = 1), deceleration starts at the time of EL input ON and, therefore, pulse output stops after passing the EL position. Be careful enough to avoid collision of the mechanical system. Also, if “stop after deceleration” is selected for the EL initiated processing mode, place the EL pin in the level input mode (which makes the EL input ON condition kept until pulse generation stops completely after deceleration).

*2. If the processing mode at the time of ALM input ON is set for “stop after deceleration” (ALMM = 1), place the ALM pin in the level input mode (which makes the ALM input ON condition kept until pulse generation stops completely after deceleration).

8.3.14 RENV2 Register

This is the register for environmental setting 2, which sets the functions of universal ports, EA/EB inputs and PA/PB inputs

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7M1	P7M0	P6M1	P6M0	P5M1	P5M0	P4M1	P4M0	P3M1	P3M0	P2M1	P2M0	P1M1	P1M0	P0M1	P0M0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	PDIR	PIM1	PIM0	EZL	EDIR	EIM1	EIM0	0	0	P1L	P0L

Bit	Name	Description
1-0	P0M1-0	Set the function of P0/FUP pin. 00: General-purpose input 01: General-purpose output 10: FUP (acceleration in progress) signal output 11: General-purpose one-shot signal output (t = 26ms)*1
3-2	P1M1-0	Set the function of P1/FDW pin. 00: General-purpose input 01: General-purpose output 01: FDW (deceleration in progress) signal output 11: General-purpose one-shot signal output (t = 26ms)*1
5-4	P2M1-0	Set the function of P2/MVC pin. 00: General-purpose input 01: General-purpose output 10: MVC (constant-speed operation) signal output in negaltive logic 11: MVC (constant-speed operation) signal output in positive logic
7-6	P3M1-0	Set the function of P3/CP1 (+SL) pin. 00: General-purpose input 01: General-purpose output 10: CP1 (comparator 1 condition being satisfied) signal output in negaltive logic 11: CP1 (comparator 1 condition being satisfied) signal output in positive logic
9-8	P4M1-0	Set the function of P4/CP2 (–SL) pin. 00: General-purpose input 01: General-purpose output 10: CP2 (comparator 2 condition being satisfied) signal output in negaltive logic 11: CP2 (comparator 2 condition being satisfied) signal output in positive logic
11-10	P5M1-0	Set the function of P5/CP3 pin. 00: General-purpose input 01: General-purpose output 10: CP3 (comparator 3 condition being satisfied) signal output in negaltive logic 11: CP3 (comparator 3 condition being satisfied) signal output in positive logic
13-12	P6M1-0	Set the function of P6/CP4/ID pin. 00: General-purpose input 01: General-purpose output 10: CP4 (comparator 4 condition being satisfied) signal output in negaltive logic 11: CP4 (comparator 4 condition being satisfied) signal output in positive logic

Bit	Name	Description
15-14	P7M1-0	Set the function of P7/CP5 pin. 00: General-purpose input 01: General-purpose output 10: CP5 (comparator 5 condition being satisfied) signal output in negaltive logic 11: CP5 (comparator 5 condition being satisfied) signal output in positive logic
16	P0L	Sets the output logic of P0 pin which is set for FUP or one-shot output (0: Negative logic, 1: Positive logic)
17	P1L	Sets the output logic of P1 pin which is set for FDW or one-shot output (0: Negative logic, 1: Positive logic)
19-18	Undefined	(Always set these bits at 0.)
21-20	E1M1-0	Select the type of input signal to the EA/EB pins. 00: 1-time multiplied 90° phase difference signal (counting up as EA input phase is advancing.) 01: 2-time multiplied 90° phase difference signal (counting up as EA input phase is advancing.) 10: 4-time multiplied 90° phase difference signal (counting up as EA input phase is advancing.) 11: Counting up at the rise of EA signal and counting down at the rise of EB signal.
22	EDIR	1: Reverses the direction of EA/EB input-initiated counting.
23	EZL	Sets EZ signal input logic. (0: Falling edge, 1: Rising edge)
25-24	PIM1-0	Select the type of input signal to the PA/PB pins. 00: 1-time multiplied 90° phase difference signal (counting up as PA input phase is advancing.) 01: 2-time multiplied 90° phase difference signal (counting up as PA input phase is advancing.) 10: 4-time multiplied 90° phase difference signal (counting up as PA input phase is advancing.) 11: Counting up at the rise of PA signal and counting down at the rise of PB signal.
26	PDIR	1: Reverses the direction of PA/PB input-initiated counting.
31-27	Undefined	(Always set these bits at 0.)

*1. For general-purpose one-shot signal output method, refer to “7.2 General-purpose Output Bit Control Command.

8.3.15 RENV3 Register

This is the register for environmental setting 3, which sets mainly the specifications of origin return and counter operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BSYC	CI41	CI40	CI31	CI30	CI21	CI20	EZD3	EZD2	EZD1	EZD0	ORM3	ORM2	ORM1	ORM0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CU4H	CU3H	CU2H	0	CU4B	CU3B	CU2B	CU1B	CU4R	CU3R	CU2R	CU1R	CU4C	CU3C	CU2C	CU1C

Bit	Name	Description
3-0	ORM3-0	Set the origin return operation mode. 0000: Origin return operation 0 ORG input turning from OFF to ON causes immediate stop (or stop after deceleration in varied-speed operation) Counter reset upon ORG input turning ON 0001: Origin return operation 1 ORG input turning from OFF to ON causes immediate stop (or stop after deceleration in varied-speed operation) and then moving at RFA constant speed in reverse direction until ORG input turns from ON to OFF, moving at RFA constant speed in the initial direction, and stop upon ORG input turning OFF to ON again. Counter reset upon ORG input turning ON 0010: Origin return operation 2 Immdiate stop upon counting up EZ after ORG input turns from OFF to ON in constant-speed operation. In varied-speed operation, deceleration upon ORG input turning from OFF to ON and stop upon counting up EZ. Counter reset upon counting up EZ 0011: Origin return operation 3 Immediate stop upon counting up EZ after ORG input turns from OFF to ON in constant-speed operation. In varied-speed operation, stop after deceleration upon counting up EZ after ORG input turns from OFF to ON. Counter reset upon counting up EZ 0100: Origin return operation 4 ORG input turning from OFF to ON causes moving at RFA constant speed in reverse direction (with deceleration in between in varied-speed operation) and stop upon counting up EZ. Counter reset upon counting up EZ 0101: Origin return operation 5 ORG input turning from OFF to ON causes moving at RFA constant speed in reverse direction after immediate stop (with deceleration in between in varied-speed operation) and stop (or stop after deceleration in varied-speed operation) upon counting up EZ. Counter reset upon counting up EZ 0110: Origin return operation 6 EL input turning ON causes moving at RFA constant speed in reverse direction after immediate stop (with deceleration in between if ELM = 1) and immediate stop upon EL input turning OFF. Counter reset upon EL input turning OFF 0111: Origin return operation 7 EL input turning ON causes moving at RFA constant speed in reverse direction after immediate stop and immediate stop upon counting up EZ. Counter reset upon counting up EZ

Bit	Name	Description
		1000: Origin return operation 8 EL input turning ON causes moving in reverse direction after immediate stop (or stop after deceleration if ELM = 1) and immediate stop (or stop after deceleration in varied-speed operation) upon counting up EZ. Counter reset upon counting up EZ 1001: Origin return operation 9 Return to 0 point (counter 2 = 0) after origin return operation 1. 1010: Origin return operation 10 Return to 0 point (counter 2 = 0) after origin return operation 3. 1011: Origin return operation 11 Return to 0 point (counter 2 = 0) after origin return operation 5. 1100: Origin return operation 12 Return to 0 point (counter 2 = 0) after origin return operation 8.
7-4	EZD3-0	Set the EZ counting value used for origin return. 0000 (1st one) to 1111 (16th one)
9-8	CI21-20	Set the input of counter 2 (mechanical position). 00: EA/EB input 10: PA/PB input 01: Output pulse
11-10	CI31-30	Set the input of counter 3 (deviation) 00: Deviation between output pulse and EA/EB input 01: Deviation between output pulse and PA/PB input 10: Deviation between EA/EB input and PA/PB input
13-12	CI41-40	Set the input of counter 4 (multi-purpose) 00: Output pulse 10: PA/PB input 01: EA/EB input 11: One-half the reference clock
14	BSYC	1: Operates counter 4 only during operation in progress ($\overline{\text{BSY}}$ = L).
15	Undefined	(Always set this bit at 0.)
16	CU1C	1: CLR input turning from OFF to ON resets counter 1.
17	CU2C	1: CLR input turning from OFF to ON resets counter 2.
18	CU3C	1: CLR input turning from OFF to ON resets counter 3.
19	CU4C	1: CLR input turning from OFF to ON resets counter 4.
20	CU1R	1: Completion of origin return resets counter 1.
21	CU2R	1: Completion of origin return resets counter 2.
22	CU3R	1: Completion of origin return resets counter 3.
23	CU4R	1: Completion of origin return resets counter 4.
24	CU1B	1: Operates counter 1 even during backlash/slip correction.
25	CU2B	1: Operates counter 2 even during backlash/slip correction.
26	CU3B	1: Operates counter 3 even during backlash/slip correction.
27	CU4B	1: Operates counter 4 even during backlash/slip correction.
28	Undefined	(Always set this bit at 0.)
29	CU2H	1: Stops counter 2 from counting.*1
30	CU3H	1: Stops counter 3 from counting.
31	CU4H	1: Stops counter 4 from counting.

*1. To stop counter 1 (command position) from counting, use MCCE (bit 11) of RMD register.

8.3.16 RENV4 Register

This is the register for environmental setting 4, which sets the specifications of comparators 1 to 4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	C2D1	C2D0	C2S2	C2S1	C2S0	C2C1	C2C0	0	C1D1	C1D0	C1D2	C1S1	C1S0	C1C1	C1C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C4D1	C4D0	C4S3	C4S2	C4S1	C4S0	C4C1	C4C0	0	C3D1	C3D0	C3D2	C3S1	C3S0	C3C1	C3C0

Bit	Name	Description
1-0	C1C1-0	Select the counter with which comparator 1 compares.*1 00: Counter 1 (command position) 10: Counter 3 (deviation) 01: Counter 2 (mecha. position) 11: Counter 4 (multi-purpose)
4-2	C1S2-0	Select the comparing method of comparator 1.*2 001: RCMP1 data = Comparing counter (no relation with counting direction. 010: RCMP1 data = Comparing counter (during counting up) 011: RCMP1 data = Comparing counter (during counting down) 100: RCMP1 data > Comparing counter 101: RCMP1 data < Comparing counter 110: To use as plus side soft limit (RCMP1 < Counter 1) Other: Condition where comparing condition is not satisfied in any case.
6-5	C1D1-0	Select an action at the time the comparator 1 condition is satisfied. 00: No processing (to be used for $\overline{\text{INT}}$, pin output, internal synchronization start) 01: Immediate stop 10: Stop after deceleration 11: Changes operation data to preregister data (speed change).
7	Undefined	(Always set this bit at 0.)
9-8	C2C1-0	Select the counter with which comparator 2 compares.*1 00: Counter 1 (command position) 10: Counter 3 (deviation) 01: Counter 2 (mecha. position) 11: Counter 4 (multi-purpose)
12-10	C2S2-0	Selects the comparing method of comparator 2.*2 001: RCMP2 data = Comparing counter (no relation with counting direction) 010: RCMP2 data = Comparing counter (during counting up) 011: RCMP2 data = Comparing counter (during counting down) 100: RCMP2 data > Comparing counter 101: RCMP2 data < Comparing counter 110: To be used as minus side soft limit (RCMP2 > Counter 1) Other: Condition where comparing condition is not satisfied in any case.
14-13	C2D1-0	Select an action at the time the comparator 2 condition is satisfied. 00: No processing (to be used for $\overline{\text{INT}}$, pin output, internal synchronization start) 01: Immediate stop 10: Stop after deceleration 11: Changes operation data to preregister data (speed change)
15	Undefined	(Always set this bit at 0.)

Bit	Name	Description
17-16	C3C1-0	Select the counter with which comparator 3 compares.*1 00: Counter 1 (command position) 10: Counter 3 (deviation) 01: Counter 2 (mecha. position) 11: Counter 4 (multi-purpose)
20-18	C3S2-0	Select the comparing method of comparator 3. 001: RCMP3 data = Comparing counter (no relation with counting direction. 010: RCMP3 data = Comparing counter (during counting up) 011: RCMP3 data = Comparing counter (during counting down) 100: RCMP3 data > Comparing counter 101: RCMP3 data < Comparing counter 110: Setting prohibited Other: Condition where comparing condition is not satisfied in any case.
22-21	C3D1-0	Select an action at the time the comparator 3 condition is satisfied. 00: No processing (to be used for INT, pin output, internal synchronization start) 01: Immediate stop 10: Stop after deceleration 11: Changes operation data to preregister data (speed change).
23	Undefined	(Always set this bit at 0.)
25-24	C4C1-0	Select the counter with which comparator 4 compares.*1 00: Counter 1 (command position) 10: Counter 3 (deviation) 01: Counter 2 (mecha. position) 11: Counter 4 (multi-purpose)
29-26	C4S3-0	Selects the comparing method of comparator 4.*2 0001: RCMP4 data = Comparing counter (no relation with counting direction) 0010: RCMP4 data = Comparing counter (during counting up) 0011: RCMP4 data = Comparing counter (during counting down) 0100: RCMP4 data > Comparing counter 0101: RCMP4 data < Comparing counter 0111: Condition where comparing condition is not satisfied in any case. 1000: To be used as ID (synchro.) signal output (no relation with counting direction. 1001: To be used as ID (synchro.) signal output (during counting up) 1010: To be used as ID (synchro.) signal output (during counting down) Other: Condition where comparing condition is not satisfied in any case
31-30	C4D1-0	Select an action at the time the comparator 4 condition is satisfied. 00: No processing (to be used for INT, pin output, internal synchronization start) 01: Immediate stop 10: Stop after deceleration 11: Changes operation data to preregister data (speed change)

*1. If counter 3 (deviation) is selected for the comparing counter, comparison is done between an absolute value of the counter and comparator data. (Range of absolute values: 0 to 32,767)

*2. If C1S2-0 are set at 110 (plus soft limit) or if C2S2-0 are set at 110 (minus soft limit), select counter 1 (command position) as the comparing counter.

*3. If C4S3-0 are set at 1000, 1001 or 1010 (synchronization signal output), select counter 4 (universal) for the comparating counter. Other counters cannot be selected. Also set the comparator value to a positive value.

8.3.17 RENV5 Register

This is the register for environmental setting 5, which sets mainly comparator 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTOF	LTFD	LTM1	LTM0	0	IDL2	IDL1	IDL0	C5D1	C5D0	C5S2	C5S1	C5S0	C5C2	C5C1	C5C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	SYI1	SYI0	SYO3	SYO2	SYO1	SYO0

Bit	Name	Description
2-0	C5C2-0	Select the counter with which comparator 5 compares. 000: Counter 1 (command position) 001: Counter 2 (mechanical position) 010: Counter 3 (deviation) 100: In-position counter 011: Counter 4 (universal) 101: Present speed data
5-3	C5S2-0	Select the comparing method of comparator 5. 001: RCMP5 data = Comparing counter (no relation with counting direction. 010: RCMP5 data = Comparing counter (during counting up) 011: RCMP5 data = Comparing counter (during counting down) 100: RCMP5 data > Comparing counter 101: RCMP5 data < Comparing counter Other: Condition where comparing condition is not satisfied in any case.
7-6	C5D1-0	Select an action at the time the comparator 5 condition is satisfied. 00: No action (using only INT and pin output) 01: Immediate stop 10: Stop after deceleration 11: Changes operation data to preregister data (speed change).
10-8	IDL1-0	Set the number of idling pulses (0 to 7 pulses).
11	Undefined	(Always set this bit at 0.)
13-12	LTM1-0	Set the latch timing of counters 1 to 4. 00: LTC input turning from OFF to ON 01: ORG signal input 10: Comparator 4 condition satisfied 11: Comparator 5 condition satisfied
14	LTFD	1: Latches present speed data in place of counter 3.
15	LTOF	1: Suspends latch with hardware timing. (Only soft timing valid)
19-16	SYO3-0	Select output timing of internal synchronization signal. 0001: Comparator 1 condition satisfied 0010: Comparator 2 condition satisfied 0011: Comparator 3 condition satisfied 0100: Comparator 4 condition satisfied 0101: Comparator 5 condition satisfied 1000: At the start of acceleration 1001: At the end of acceleration 1010: At the start of deceleration 1011: At the end of deceleration Other: Internal synchronization signal output OFF
21-20	SYI1-0	Select the axis of the internal synchro. signal which starts operation. 00: X axis 01: Y axis 10: Z axis 11: U axis
31-22	Undefined	(Always set these bits at 0.)

8.3.18 RENV6 Register

This is the register for environmental setting 6, which sets mainly data for correction of moving amount.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	ADJ1	ADJ0	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
11-0	BR11-0	Set the amount for correction of backlash or slip.
13-12	ADJ1-0	Select the moving amount correction method. 00: Correction function OFF 10: Slip correction 01: Backlash correction
31-14	Undefined	(Always set these bits at 0.)

8.3.19 RENV7 Register

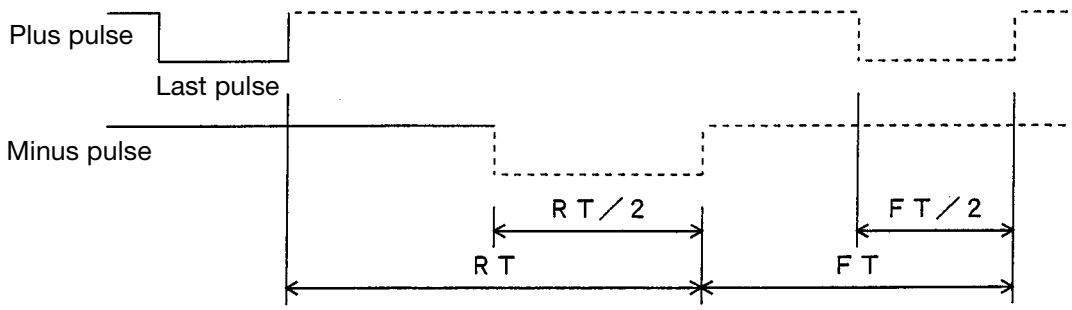
This is the register for environmental setting 7, which sets the time for vibration suppression function. The vibration suppression function is made valid when RT and FT data are other than 0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT15	RT14	RT13	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FT15	FT14	FT13	FT12	FT11	FT10	FT9	FT8	FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0

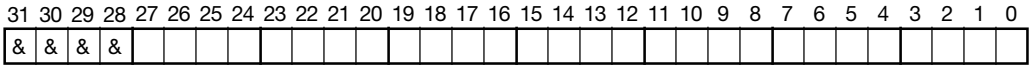
Bit	Name	Description
15-0	RT15-0	Set the time width of RT shown in the figure below. Setting unit is 32 times the reference clock, that is approx. 1.6μs.
31-16	FT15-0	Set the time width of FT shown in the figure below. Setting unit is 32 times the reference clock, that is approx. 1.6μs.

Pulses of dotted line are the pulses added by the vibration suppression function.



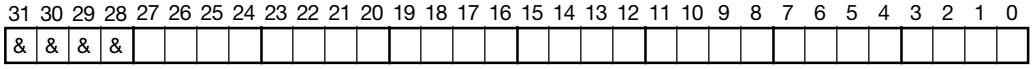
8.3.20 RCUN1 Register

This register is the counter 1 (command position counter) which is exclusively used for counting command pulses. Setting range is –134,217,728 to +134,217,727.



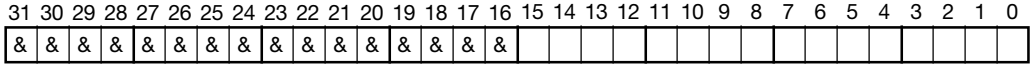
8.3.21 RCUN2 Register

This register is the counter 2 (mechanical position counter) which can count command pulses, encoder signals (EA/EB input) or pulse signals (PA/PB input). Setting range is –134,217,728 to +134,217,727.



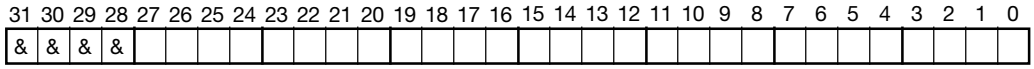
8.3.22 RCUN3 Register

This register is the counter 3 (deviation counter) which can count deviation between command pulses and encoder signals, between command pulses and pulser signals or between encoder signals and pulse signals. Setting range is –32,768 to +32,767.



8.3.23 RCUN4 Register

This register is the counter 4 (multi-purpose counter) which can count command pulses, encoder signals (EA/EB input), pulser signal (PA/PB input) or clock signals of one-half the reference clock. Setting range is –134,217,728 to +134,217,727.

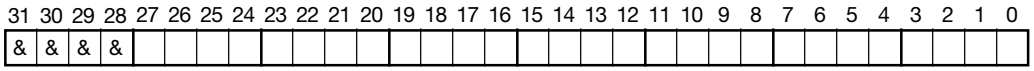


For further information on counters, refer to “”11.10 Counters.”

NOTES: 1. Bits in which ∗ is put are disregarded in writing and become 0 when reading.
2. Bits in which & is put are disregarded in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

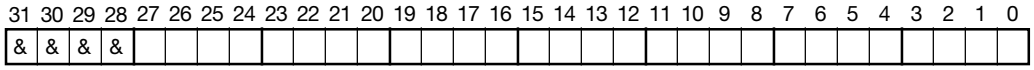
8.3.24 RCMP1 Register

This register sets the data with which comparator 1 compares a parameter.
Setting range is –134,217,728 to +134,217,727.



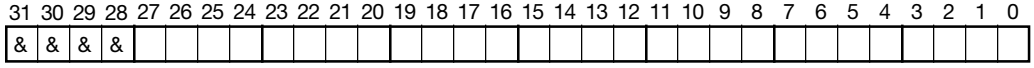
8.3.25 RCMP2 Register

This register sets the data with which comparator 2 compares a parameter.
Setting range is –134,217,728 to +134,217,727.



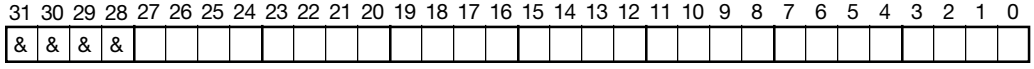
8.3.26 RCMP3 Register

This register sets the data with which comparator 3 compares a parameter.
Setting range is –134,217,728 to +134,217,727.



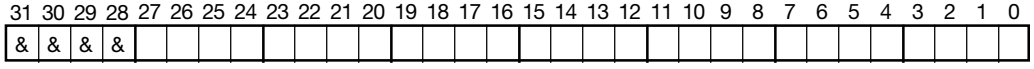
8.3.27 RCMP4 Register

This register sets the data with which comparator 4 compares a parameter.
Setting range is –134,217,728 to +134,217,727.



8.3.28 RCMP5 (PRCP5) Register

This register sets the data with which comparator 5 compares a parameter.
PRCP is the 2nd preregister for RCP5.
Setting range is –134,217,728 to +134,217,727.



For further information on comparators, refer to “”11.11 Comparators.”

NOTES: 1. Bits in which ∗ is put are disregarded in writing and become 0 when reading.
2. Bits in which & is put are disregarded in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.29 RIRQ Register

This register sets event interrupt factors. Set the bits which you wish to initiate event interrupt, at 1.

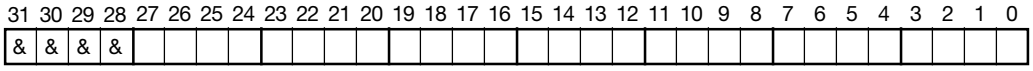
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IROL	IRLT	IRCL	IRC5	IRC4	IRC3	IRC2	IRC1	IRDE	IRDS	IRUE	IRUS	IRND	IRNM	IRN	IREN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	IRSA	IRDR	IRSD

Bit	Name	Description
0	IREN	Normal stop
1	IRN	Successive start of the next operation
2	IRNM	2nd preregister for operation write-enabled
3	IRND	2nd preregister for comparator 5 write-enabled
4	IRUS	Start of acceleration
5	IRUE	End of acceleration
6	IRDS	Start of deceleration
7	IRDE	End of deceleration
8	IRC1	Comparator 1 condition satisfied
9	IRC2	Comparator 2 condition satisfied
10	IRC3	Comparator 3 condition satisfied
11	IRC4	Comparator 4 condition satisfied
12	IRC5	Comparator 5 condition satisfied
13	IRCL	CLR signal input resetting counter value
14	IRLT	LTC input making counter value latched
15	IROL	ORG input making counter value latched
16	IRSD	SD input ON
17	IRDR	±DR input change
18	IRSA	CSTA input ON
31-19	Undfined	(Always set these bits at 0.)

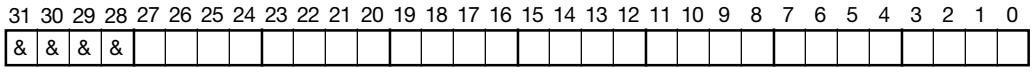
8.3.30 RLTC1 Register

This read-only register latches data of counter 1 (command position counter) aaccording to LTC, ORG input or LTCH command. Data range is –134,217,728 to +134,217,727.



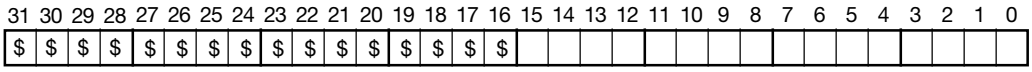
8.3.31 RLTC2 Register

This read-only register latches data of counter 2 (mechanical position counter) according to LTC, ORG input or LTCH command. Data range is –134,217,728 to +134,217,727.



8.3.32 RLTC3 Register

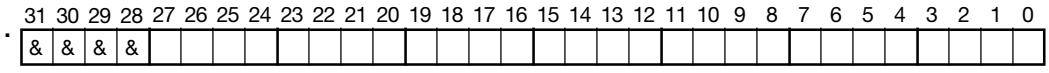
This read-only register latches data of counter 3 (deviation counter) or the present speed according to LTC, ORG input or LTCH command. If RENV5 register's LTFD = 0, it latches data of counter 3 and if LTFD = 1, it latches the present speed. Under stop condition with LTFD = 0, latched data is 0. Data range is –32,768 to +32,767 with LTFD = 0 and 0 to 65535 with LTFD = 1.



Bits in which $ is put have the same value as bit 15 with RENV5's LTFD (bit 14) = 0, and 0 with LTFD = 1.

8.3.33 RLTC4 Register

This read-only register latches data of counter 4 (universal counter) according to LTC, ORG input or LTCH command. Data range is –134,217,728 to +134,217,727



For further information on latching counter data, refer to ""11.10 Counters."

NOTES: 1. Bits in which ∗ is put are disregarded in writing and become 0 when reading.
2. Bits in which & is put are disregarded in writing and have the same value as the highest-place bit now in blank when reading. (code extension)

8.3.34 RSTS Register

This read-only register allows reading the extension status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDIN	SLTC	SCLR	SDRM	SDRP	SEZ	SERC	SPCS	SEMG	SSTP	SSTA	SDIR	CND3	CND2	CND1	CND0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SINP

Bit	Name	Description
3-0	CND3-0	Indicate operation status as follows 0000: Cessation 0001: Waiting for DR input 0010: Waiting for $\overline{\text{CSTA}}$ input 0011: Waiting for internal synchronization signal 0100: Waiting for cessation of other axis 0101: Waiting for completion of ERC timer operation 0110: Waiting for completion of direction change timer operation 0111: Backlash correction in progress 1000: Waiting for PA/PB input 1001: Constant-speed operation in progress at FA rate 1010: Constant-speed operation in progress at FL rate 1011: Acceleration in progress 1100: Constant-speed operation in progress at FH rate 1101: Deceleration in progress 1110: Waiting for INP input 1111: Other (during start control)
4	SDIR	Operating direction (0: Plus direction, 1: Minus direction)
5	SSTA	1 when $\overline{\text{CSTA}}$ input signal is ON
6	SSTP	1 when $\overline{\text{CSTP}}$ input signal is ON
7	SEMG	1 when $\overline{\text{CEMG}}$ input signal is ON
8	SPCS	1 when PCS input signal is ON
9	SERC	1 when ERC output signal is ON
10	SEZ	1 when EZ input signal is ON
11	SDRP	1 when +DR input signal is ON
12	SDRM	1 when –DR input signal is ON
13	SCLR	1 when CRL input signal is ON
14	SLTC	1 when LTC input signal is ON
15	SDIN	1 when SD input signal is ON (SD input pin status)
16	SINP	1 when INP input signal is ON
31-17	Undfined	0 at all times

8.3.35 REST Register

This read-only register allows checking of error interrupt factor. When an error interrupt occurs, the corresponding bit becomes 1. This register is reset by reading the data.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ESAO	ESPO	ESIP	ESDT	0	ESSD	ESEM	ESSP	ESAL	ESML	ESPL	ESC5	ESC4	ESC3	ESC2	ESC1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	ESPE	ESEE

Bit	Name	Description
0	ESC1	Comparator 1 condition satisfied (+SL) interrupts pulse output.
1	ESC2	Comparator 2 condition satisfied (–SL) interrupts pulse output.
2	ESC3	Comparator 3 condition satisfied interrupts pulse output.
3	ESC4	Comparator 4 condition satisfied interrupts pulse output.
4	ESC5	Comparator 5 condition satisfied interrupts pulse output.
5	ESPL	+EL input turning ON interrupts pulse output.
6	ESML	–EL input turning ON interrupts pulse output.
7	ESAL	ALM input turning ON interrupts pulse output.
8	ESSP	$\overline{\text{CSTP}}$ input turning ON interrupts pulse output.
9	ESEM	$\overline{\text{CEMG}}$ input turning ON interrupts pulse output.
10	ESSD	SD signal turning ON interrupts pulse output after deceleration.
11	Undefined	(Always 0)
12	ESDT	Abnormal operation data interrupts pulse output.
13	ESIP	Abnormal stop of other axis during interpolation causes simultaneous stop.
14	ESPO	PA/PB input buffer counter overflows.
15	ESAO	In-position counter counts beyond the range at the time of interpolation.
16	ESEE	EA/EB input error
17	ESPE	PA/PB input error
31-18	Undefined	(Always 0)

8.3.36 RIST Register

This read-only register allows checking of event interrupt factor. When an event interrupt occurs, the corresponding bit becomes 1. This register is reset by reading the data.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISOL	ISLT	ISCL	ICS5	ISC4	ISC3	ISC2	ISC1	ISDE	ISDS	ISUE	ISUS	ISND	ISNM	ISN	ISEN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	ISSA	ISMD	ISPD	ISSD

Bit	Name	Description
0	ISEN	Automatic stop
1	ISN	Successive start of the next operation
2	ISNM	2nd preregister for operation is write-enabled.
3	ISND	2nd preregister for comparator 5 is write-enabled.
4	ISUS	Start of acceleration
5	ISUE	End of acceleration
6	ISDS	Start of deceleration
7	ISDE	End of decelation
8	ISC1	Comparator 1 condition satisfied
9	ISC2	Comparator 2 condition satisfied
10	ISC3	Comparator 3 condition satisfied
11	ISC4	Comparator 4 condition satisfied
12	ISC5	Comparator 5 condition satisfied
13	ISCL	CLR signal input resets the counter value.
14	ISLT	LTC input makes the counter value latched.
15	SIOL	CRG input makes the counter value latched.
16	ISSD	SD input turns ON.
17	ISPD	+DR input changes.
18	ISMD	–DR input changes.
19	ISSA	$\overline{\text{CSTA}}$ input turns ON.
31-20	Undefined	(Always 0)

8.3.37 RPLS Register

This read-only register is the counter which allows you to check the number of remaining pulses. At the start of operation it is set at an absolute value of RMV register and counts down at every pulse output.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0																												

8.3.38 RSPD Register

This read-only register allows you to check the EZ counter value and the present speed.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AS15	AS14	AS13	AS12	AS11	AS10	AS9	AS8	AS7	AS6	AS5	AS4	AS3	AS2	AS1	AS0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	IDC2	IDC1	IDC0	ECZ3	ECZ2	ECZ1	ECZ0

Bit	Name	Description
15-0	AS15-0	These bits allows you to read the present speed as a step value in the same unit as RFL or RFH. These bits are 0 when the chip stops generating pulses.
19-16	ECZ3-0	These bits allows you to read the EZ counter value used for origin return.
22-20	IDC2-0	These bits allows you to read idling pulse counting value.
31-23	Undefined	(Always 0)

8.3.39 RSDC Register

This read-only register allows you to check an automatically calculated value of the ramping-down point for in-positioning.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0																								

8.3.40 RIPS Register

This read-only register allows you to check the interpolation setting and operation status. It is a common register to all axes and shows the same contents if read from any axis.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPFu	IPFz	IPFy	IPFx	IPSu	IPSz	IPSy	IPSx	IPEu	IPEz	IPEy	IPEx	IPLu	IPLz	IPLy	IPLx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	SED1	SED0	SDM1	SDM0	IPCC	IPCW	IPE	IPL

Bit	Name	Description
0	IPLx	1: X axis is in linear interpolation 1 mode.
1	IPLy	1: Y axis is in linear interpolation 1 mode.
2	IPLz	1: Z axis is in linear interpolation 1 mode.
3	IPLu	1: U axis is in linear interpolation 1 mode.
4	IPEx	1: X axis is in linear interpolation 2 mode.
5	IPEy	1: Y axis is in linear interpolation 2 mode.
6	IPEz	1: Z axis is in linear interpolation 2 mode.
7	IPEu	1: U axis is in linear interpolation 2 mode.
8	IPSx	1: X axis is in circular interpolation mode.
9	IPSy	1: Y axis is in circular interpolation mode.
10	IPSz	1: Z axis is in circular interpolation mode.
11	IPSu	1: U axis is in circular interpolation mode.
12	IPFx	1: X axis is designated for composite speed constant control.
13	IPFy	1: Y axis is designated for composite speed constant control.
14	IPFz	1: Z axis is designated for composite speed constant control.
15	IPFu	1: U axis is designated for composite speed constant control.
16	IPL	1: Linear interpolation 1 in progress
17	IPE	1: Linear interpolation 2 in progress
18	IPCW	1: Circular interpolation in CW direction in progress
19	IPCC	1: Circular interpolation in CCW direction in progress
21-20	SDM1-0	Present quadrant of circular interpolation 00: 1st 01: 2nd 10: 3rd 11: 4th
23-22	SED1-0	Ending quadrant of circular interpolation 00: 1st 01: 2nd 10: 3rd 11: 4th
31-21	Undefined	(Always set these bits at 0.)

9. Operation Modes

The basic operation mode is set by writing the data to bits 6 to 0 (MOD) of RMD (operation mode) register.

9.1 Continuous Operation Mode under Command Control

In this mode the chip continues generating pulses after receiving the start command until the stop command is written .

MOD: 00HEX (continuous pulse output in plus direction)
08HEX (continuous pulse output in minus direction)

EL signal also stops the continuous pulse output. +EL signal is valid to stop pulse output in plus direction and –EL signal is valid to stop pulse output in minus direction. To restart in reverse direction after EL signal stops pulse output, you need to write the start command anew.

9.2 In-position Mode

In-position mode can be executed in any of the following five ways.

MOD: 41HEX (in-positioning with relative target position designated)
44HEX (in-positioning to command position 0)
45HEX (in-positioning to mechanical position 0)
46HEX (one-pulse operation in plus direction)
4EHEX (one-pulse operation in minus direction)
47HEX (timer operation)

9.2.1 In-positioning with Relative Target Position Designated (MOD: 41HEX)

In this mode the chip generates pulses in the number written in the RMV (target position) register. The moving direction is as set in the RMV register. When the in-position counter counts down to 0, the chip stops generating pulses. If in-positioning is started with the RMV register set at 0, the chip does not generate any pulse and is placed in immediate stop condition.

9.2.2 In-positioning to Command Position 0 (MOD: 44HEX)

In this mode the chip generates pulses until the counter 1 (command position) counts down to 0. The number of output pulses and moving direction are automatically determined through internal calculation according to the counter 1 value at the start.

9.2.3 In-positioning to Mechanical Position 0 (MOD: 45HEX)

In this mode the chip generates pulses until the counter 2 (mechanical position) counts down to 0. The number of output pulses and moving direction are automatically determined through internal calculation according to the counter 2 value at the start.

9.2.4 One-pulse Operation (MOD: 46HEX, 4EHEX)

In this mode the chip generates one pulse only.

MOD: 46HEX (one pulse output in plus direction)

4EHEX (one pulse output in minus direction)

The effect is same as in-positioning with relative target designated and by setting the RMV register at 1 or –1 but in this case you need not set the RMV register.

9.2.5 Timer Operation (MOD: 47HEX)

This mode allows you to use the internal operation time as a timer. Though the internal operation is the same as in-positioning, the chip does not generate any pulse, that is, pulses are masked. If the start command is written for constant-speed operation, the internal operation time is the product of the cycle of output pulse and the value written in the RMV register.

e.g. If 1000pps and 120 pulses are set, internal operation time is 120ms.

Write a positive value (1 to 134,217,727) to the RMV register.

In this mode;

$\pm$EL and SD signals and soft limit are ignored (always regarded as 0). ALM, $\overline{\text{CSTP}}$ and $\overline{\text{CEMG}}$ input signals are valid.

Functions such as backlash/slip correction, vibration suppression and timer for direction change are suspended.

The counter 1 (commond position) stops counting.

INP signal does not delay the completion of operation irrespective of setting of bit 9 (MINP) of RMD (operation mode) register.

To eliminate an error of the internal operation time, set bit 12 (METM) of RMD register at 0 so as to make the time of completion of output pulse cycle the operation completion timing.

9.3 Pulser (PA/PB) Input Mode

In this mode the chip operates based on pulser input. To make the pulser input valid, set the $\overline{PE}$ pin at low level. A filter may be inserted to the $\overline{PE}$ input. Write the start command, and the chip will output pulses from the OUT pin upon receiving signals from the pulser. In this mode, use the start command for constant-speed operation at FL rate (STAFL; 50HEX) or at FH rate (STAFH; 51HEX). For PA/PB input pins, you can select the pulser signal input method from two by setting the RENV2 (environmental setting 2) register.

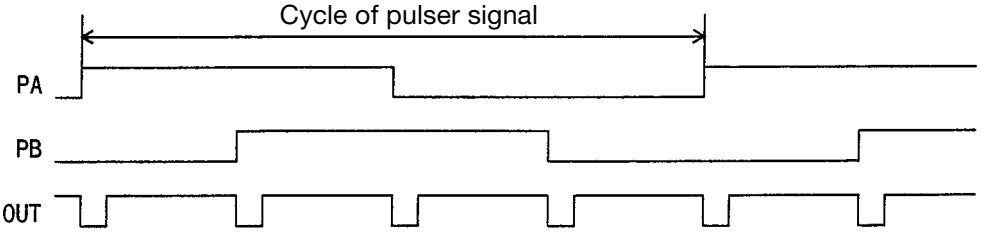
90° phase difference signal (1, 2 or 4 times multiplied)
2 types of pulses (plus and minus pulses)

In addition, the pulser input mode can be executed in any of the following four ways. The moving direction in continuous operation can be changed by setting the RENV2 register without changing wiring of PA/PB pins.

MOD	Operation	Moving direction
01HEX	Continuous operation based on pulser	Depends on PA/PB input.
51HEX	In-positioning based on pulser	Depends on the sign of RMV value.
54HEX	In-positioning to command position 0 based on pulser	Automatically set based on RCUN1 value at the start
55HEX	In-positioning to mechanical position 0 based on pulser	Automatically set based on RCUN2 value at the start

The OUT pin outputs pulses based on PA/PB input at the following timing.

e.g. In the case PA/PB pins input 4-times multiplied 90° phase difference signal



In the pulser input mode, the EL signal in moving direction stops pulse output but does not restrict pulse output in reverse direction. Also, error interrupt does not occur ($\overline{INT}$ signal is not output). To cancel the operation, write the immediate stop command (49HEX).

A maximum input frequency of pulser signal is restricted by the FL rate in constant-speed operation at the FL rate and by the FH rate in constant-speed operation at FH rate. If PA and PB input signals change at a time or if the input frequency is beyond the range, thereby letting the input buffer counter overflow, it may be regarded as an error to output the $\overline{INT}$ signal. Also, it can be monitored by reading the REST (error interrupt factor) register.

Relations between FH (FL) Rate (pps) and Pulser Input Frequency FP (pps)

PA/PB Input Method	Usable Range
2-pulse input	FP < FH (or FL)
90° phase difference signal, 1 time multiplied	FP < FH (or FL)
90° phase difference signal, 2 times multipled	FP < FH (or FL)/2
90° phase difference signal, 4 times multiplied	FP < FH (or FL)/4

To select the type of PA/PB input signal, set bits 25 and 24 (PIM1 and 0) of the RENV2 register as follows:

00: 90° phase difference signal, 1 time multiplied
01: 90° phase difference signal, 2 times multiplied
10: 90° phase difference signal, 4 times multiplied
11: 2 types of pulses, plus and minus

[RENV2] (WRITE)

31							24
0	0	0	0	0	–	n	n

To select the PA/PB input counting direction, set bit 26 (PDIR) of the RENV2 register as follows:

0: Counts up when PA phase is advancing or at the rise of PA.
1: Counts up when PB phase is advancing or at the rise of PB

[RENV2] (WRITE)

31							24
0	0	0	0	0	n	–	–

To insert a filter to ±DR and PE inputs, set bit 27 (DRF) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidth shorter than 32ms are ignored.

[RENV1] (WRITE)

31							24
–	–	–	–	n	–	–	–

To check the operation status, read bits 3 to 0 (CND) of the RSTS register.

1000: Waiting for PA/PB input

[RSTS] (READ)

7							0
–	–	–	–	n	n	n	n

To check PA/PB input error, read bit 17 (ESPE) of the REST register.

1: PA/PB input error generated

[REST] (READ)

23							16
0	0	0	0	0	0	n	–

To check the status of PA/PB input buffer counter, read bit 14 (ESPO) of the REST register.

1: Overflow

[REST] (READ)

15							8
–	n	–	–	–	–	–	–

NOTE:

In the register bit explanation chart illustrated at the right of each description, “n” indicates the bit position to write or read and “0” indicates the bit position to which writing other than “0” is prohibited or which is fixed to “0” when reading. This applies to all the charts above and hereafter.

9.3.1 Continuous Operation based on Pulser Input (MOD: 01HEX)

In this mode the chip continues outputting pulses from the OUT pin by receiving signals through PA/PB pins after the start command is written. The moving direction depends on the type of PA/PB signal and the setting of PDIR.

Type of PA/PB Input	PDIR	Moving Direction	PA/PB Input Status
90° phase difference signal (1, 2 or 4 times multiplied)	0	Plus	PA phase advances over PB phase.
		Minus	PB phase advances over PA phase.
	1	Plus	PB phase advances over PA phase.
		Minus	PA phase advanced over PB phase.
Plus and minus pulses	0	Plus	Rise of PA input
		Minus	Rise of PB input
	1	Plus	Rise of PB input
		Minus	Rise of PA input

9.3.2 In-positioning based on Pulser Input (MOD: 51HEX)

The moving direction is determined by the sign of RMV (target position) register value. At the start, the RMV register value is loaded in the in-position counter and when receiving pulser signals through the PA or PB pin, the chip outputs pulses from the OUT pin while counting down the in-position counter. The chip stops outputting pulses when the in-position counter counts down to 0. If started with the RMV register set at 0, the chip does not output any command pulse and is placed in the immediate stop condition.

9.3.3 In-positioning to Command Position 0 based on Pulser Input (MOD: 54HEX)

In this mode, the chip outputs pulses by receiving signals from the pulser until the counter 1 (command position) counts down to 0. The number of output pulses and the moving direction are automatically set through internal calculation based on the counter 1 value at the start. If started with the counter 1 set at 0, the chip does not output any pulse and is placed in the immediate stop condition.

9.3.4 In-positioning to Mechanical Position 0 based on Pulser Input (MOD: 55HEX)

In this mode, the chip outputs pulses by receiving signals from the pulser until the counter 2 (mechanical position) counts down to 0. The number of output pulses and the moving direction are automatically set through internal calculation based on the counter 2 value at the start. If started with the counter 2 set at 0, the chip does not output any pulse and is placed in immediate stop condition.

9.4 External Switch (±DR) Based Operation Mode (MOD: 02HEX, 56HEX)

To use this mode, enable the external switch input by setting the $\overline{PE}$ pin at low level. In this mode the chip outputs pulses from the OUT pin when receiving +DR or –DR signal after the start command is written. This mode can be executed in any of the following two ways:

MOD: 02HEX: Continuous operation based on external switch
56HEX: In-positioning based on external switch

The input logic of ±DR signal is set using the RENV1 (environmental setting 1) register and the $\overline{INT}$ signal may be output at the time ±DR signal changes. The operation status including ±DR input can be checked by reading the extension status (RSTS) register. Also, a filter can be inserted to ±DR and $\overline{PE}$ inputs.

To select the input logic of +DR/–DR signals, set bit 25 (DRL) of the RENV1 register as follows:

0: Negative logic
1: Positive logic

[RENV1] (WRITE)

31							24
–	–	–	–	–	–	n	–

To insert a filter to ±DR and $\overline{PE}$ inputs, set bit 27 (DRF) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidths shorter than 32ms are ignored.

[RENV1] (WRITE)

31							24
–	–	–	–	n	–	–	–

To output the $\overline{INT}$ signal (event interrupt signal) at the time the ±DR signal input changes, set bit 17 (IRDR) of the RIRQ register at 1.

[RIRQ] (WRITE)

23							16
0	0	0	0	0	–	n	–

To check the event interrupt factor, read bits 17 and 18 of the RIST register.

Bit 17 (ISPO) = 1: +DR signal input changes.
Bit 18 (ISMD) = 1: –DR signal input changes.

[RIST] (READ)

23							16
0	0	0	0	–	n	n	–

To check the operation status, read bits 3-0 (CND) of the REST register.

0001: Waiting for DR signal input

[RSTS] (READ)

7							0
–	–	–	–	n	n	n	n

To check ±DR signal status, read bits 11-12 of the RSTS register.

Bit 11 (SDRP) = 0: +DR signal OFF, 1: +DR signal ON
Bit 12 (SDRM) = 0: –DR signal OFF, 1: –DR signal ON

[RSTS] (READ)

15							8
–	–	–	n	n	–	–	–

9.4.1 External Switch-Based Continuous Operation (MOD: 02HEX)

In this mode the chip generates pulses only when the DR switch is turned on. It operates in a designated pattern by generating pulses in plus direction when the +DR signal turns on, and in minus direction when the –DR signal turns on, after the start command is written. In this mode the EL signal in the moving direction stops the chip from generating pulses but does not restrict it to output in the reverse direction. Also, the error interrupt ($\overline{INT}$ output) does not occur. To cancel this mode, write the immediate stop command (49HEX).

If started for varied-speed operation, the chip decelerates and then stops pulse output when the DR input turns off. If the DR input turns on during deceleration in progress, the chip completes deceleration and then restarts to the new direction.

Typical operation procedure

(1) Set the PE input at low level.
(2) Set RFL, RFH, PUR, PDR and PMG registers (speed setting).
(3) Set bits 6-0 (MOD) of the RMD (operation mode) register at 0000010.
(4) Write the start command (50HEX to 53HEX).
(5) Bits 3-0 (CND) of the RSTS (extension status) register will be set at 0001 (waiting for DR input). Under the condition, turn the +DR or –DR input pin on. The chip will start operating in the speed pattern designated by the start command until the DR input turns off.

9.4.2. External Switch-Based In-positioning (MOD: 56HEX)

In this mode in-positioning is made by the timing of turning the DR input from OFF to ON. At the start, the RMV register value is loaded in the in-position counter. When the DR input turns on, the chip generates pulses until the in-position counter counts down to 0. If the DR input turns off during pulse output in progress, it does not affect the pulse output. If started with the RMV register set at 0, the chip does not output any pulse and is placed in the immediate stop condition.

The +DR signal initiates pulse output in plus direction and the –DR signal, in minus direction. When the EL signal in the moving direction turns on, the chip stops generating pulses while outputting the error interrupt signal ($\overline{INT}$).

9.5 Origin-Related Modes

The PCL6045 provides the following three origin-related modes:

Origin return mode

MOD: 10HEX for origin return in plus direction

MOD: 18HEX for origin return in minus direction

Origin escape mode

MOD: 12HEX for origin escape in plus direction

MOD: 1AHEX for origin escape in minus direction

Origin search mode

MOD: 15HEX for origin search in plus direction

MOD: 1DHEX for origin search in minus direction

For origin-related modes, ORG, EZ and/or ±EL inputs are used depending on the operation method.

The logic of ORG input signal is set by the RENV1 (environmental setting 1) register and the ORG pin status can be checked by reading the sub status (SSTSW) register.

The logic of EZ input signal is set by the RENV2 (environmental setting 2) register and the EZ pin status can be checked by reading the extension status (RSTS) register. The value the EZ counter counts to complete an origin return is set by the RENV3 (environmental setting 3) register.

The logic of ±EL input signals is set by the ELL input pin and the action (immediate stop or stop after deceleration) initiated at the time the EL signal turns on is selected by the RENV1 register. The pin status can be checked by reading the SSTSW.

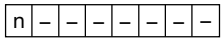
To ORG and ±EL input signals, an input filter can be inserted by setting the RENV1 register.

To select the input logic of ORG signal, set bit 7 (ORGL) of the RENV1 register.

0: Negative logic

1: Positive logic

[RENV1] (WRITE)

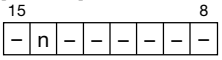


To check the ORG signal status, read bit 14 (SORG) of SSTSW.

0: ORG signal OFF

1: ORG signal ON

[SSTSW] (READ)

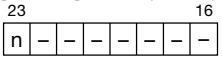


To select the input logic of EZ signal, set bit 23 (EZL) of the RENV2 register.

0: Falling edge

1: Rising edge

[RENV2] (WRITE)



To set the EZ counter value, write the value (counting value – 1) to bits 7-4 (EZD3-0) of the RENV3 register in a range of 0 to 15. The chip will output pulses in the number written to these bits before completing an origin return.

[RENV3] (WRITE)

7							0
n	n	n	n	–	–	–	–

To check the EZ signal status, read bit 10 (SEZ) of the RSTS register.

0: EZ signal OFF
1: EZ signal ON

[RSTS] (READ)

15							8
–	–	–	–	–	n	–	–

To select the input logic of ±EL signals, set the ELL input pin.

Low level: Positive logic
High level: Negative logic

To select the action initiated by +EL or –EL signal turning on, set bit 3 (ELM) of the RENV1 register.

0: Immediate stop
1: Stop after deceleration

[RENV1] (WRITE)

7							0
–	–	–	–	n	–	–	–

To check the ±EL signal status, read bits 12 (SPEL) and 13 (SMEL) of SSTSW.

SPEL = 0: +EL signal OFF SPEL = 1: +EL signal ON
SMEL = 0: –EL signal OFF SMEL = 1: –EL signal ON

[SSTSW] (WRITE)

15							8
–	–	n	n	–	–	–	–

To insert the ±EL and ORG input filter, set bit 26 (FLTR) of the RENV1 filter at 1. If the filter is inserted, signals of pulsewidths shorter than 4µs are ignored.

[RENV1] (WRITE)

27							20
–	n	–	–	–	–	–	–

9.5.1 Origin Return Operation

In the origin return mode the start command lets the chip continue generating pulses until the condition to complete an origin return is satisfied.

MOD: 10_{HEX}: Origin return in plus direction
18_{HEX}: Origin return in minus direction

The counter can be reset and the ERC (deviation counter clear) signal can be output at the time of origin return completion . The basic origin return method and the presence of counter reset at origin return completion are set by the RENV3 register. The presence of ERC signal output is set by the RENV1 register. For details on the ERC signal, refer to “11.6.2 ERC Signal.”

To select the origin return method, set bits 3-0 (ORM3-0) of the RENV3 register as follows:

[RENV3] (WRITE)

7							0
–	–	–	–	n	n	n	n

0000: Origin return operation 0
ORG signal turning from OFF to ON causes immediate stop (stop after deceleration in varied-speed operation).
The counter is reset upon ORG signal turning from OFF to ON

0001: Origin return operation 1
ORG signal turning from OFF to ON causes immediate stop (stop after deceleration in varied-speed operation), then the chip generates pulses until the ORG signal turns from ON to OFF and after the signal turns off, it generates pulses at the RFA rate in initial direction and immediately stops when the ORG signal turns from OFF to ON again. The counter is reset upon the ORG signal turning from OFF to ON.

0010: Origin return operation 2
In constant-speed operation, the chip immediately stops pulse output upon the EZ counter counting up to the preset value after the ORG signal turns from OFF to ON.
In varied-speed operation, the chip decelerates pulse output when the ORG signal turns from OFF to ON and stops immediately upon the EZ counter counting up to the preset value.
The counter is reset upon the EZ counter counting up to the preset value.

0011: Origin return operation 3
In constant-speed operation, the chip immediately stops pulse output upon the EZ counter counting up to the preset value after the ORG signal turns from OFF to ON.
In varied-speed operation, the chip decelerates and stops pulse output upon the EZ counter counting up to the preset value after the ORG signal turns from OFF to ON.
The counter is reset upon the EZ counter counting up to the preset value.

0100: Origin return operation 4
The chip immediately stops pulse output (stops after decerlation in varied-speed operation) upon the ORG signal turning from OFF to ON and then generates pulses in reverse direction at the RFA rate before immediate stop again upon the EZ counter counting up to the preset value.
The counter is reset upon the EZ counter counting up to the preset value.

[RENV3] (WRITE)

7							0
–	–	–	–	n	n	n	n

0101: Origin return operation 5
The chip immdiately stops pulse output (stops after deceleration invaried-speed operation) upon the ORG signal turning from OFF to ON and then generates pulses in reverse direction before immed-ate stop (stop after deceleration in varied-speed operation) upon the EZ counter counting up to the preset value.
The counter is reset when the EL signal turns off.

0110: Origin return operation 6
The chip immediately stops pulse output (stops after deceleration if ELM = 1) upon the EL signal turning ON and then generates pulses in reverse direction at the RFA rate before immediate stop again upon the EL signal turning off.
The counter is reset when the EL signal turns off.

0111: Origin return operation 7
The chip immediately stops pulse output (stops after deceleration if ELM = 1) and then generates pulses in reverse direction at the RFA rate before immediate stop again upon the EZ counter counting up to the preset value.
The counter is reset at the immediate stop upon the EZ counter counting up to the preset value.

1000: Origin return operation 8
The chip immediately stops pulse output (stops after deceleration if ELM = 1) and then generates pulses in reverse direction before immediate stop again (stop after deceleration in varied-speed operation) upon the EZ counter counting up to the preset value.
The counter is reset upon the EZ counter counting up to the preset value.

1001: Origin return operation 9
After performing origin return operation 0, the chip generates pulses to return to 0 point, that is, until the counter 2 counts down to 0.

1010: Origin return operation 10
After performing origin return operation 3, the chip generates pulses to return to 0 point, that is, until the counter 2 counts down to 0.

1011: Origin return operation 11
After performing origin return operation 5, the chip generates pulses to return to 0 point, that is, until the counter 2 counts down to 0.

1100: Origin return operation 12
After performing origin return operation 8, the chip generates pulses to return to 0 point, that is, until the counter 2 counts down to 0.

To select the counter which is reset at the completion of origin return, sets bits 23-20 (CU4R-1R) of the RENV3 register.

[RENV3] (WRITE)

23							16
n	n	n	n	–	–	–	–

CU1R (bit 20) = 1: Counter 1 (command position) is reset.
CU2R (bit 21) = 1: Counter 2 (mechanical position) is reset.
CU3R (bit 22) = 1: Counter 3 (deviation) is reset.
CU4R (bit 23) = 1: Counter 4 (multi-purpose) is reset.

To automatically output the ERC signal or not, set bit 11 (EROR) of the RENV1 register.

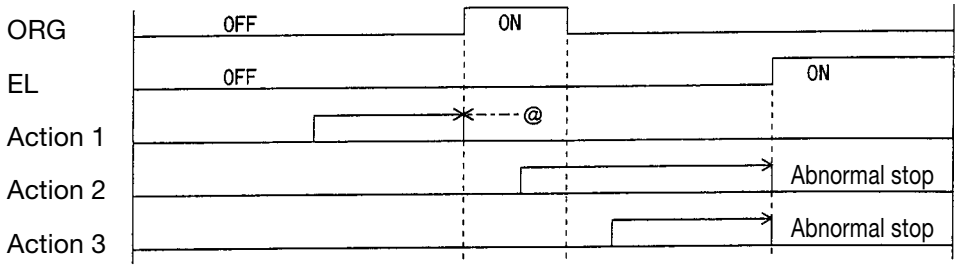
[RENV1] (WRITE)

15							8
–	–	–	–	n	–	–	–

0: No ERC signal is output at the completion of origin return.
1: ERC signal is output at the completion of origin return.

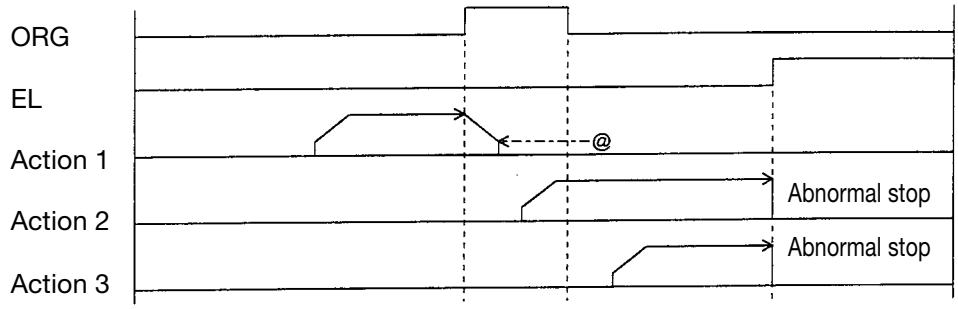
9.5.1.1 Origin Return Operation 0 (ORM = 0000)

Constant-Speed Operation [Sensor: EL (ELM = 0), ORG]



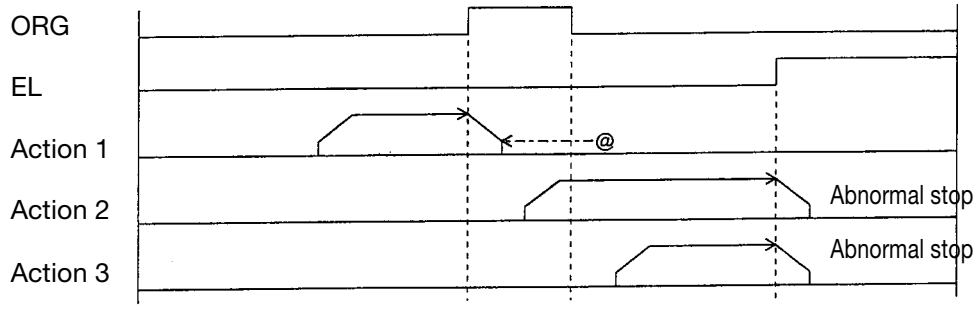
Varied-Speed Operation [Sensor: EL (ELM = 0), ORG]

Though it does not return to the origin position even at normal stop, the value of counter 2 (mechanical position) is reliable

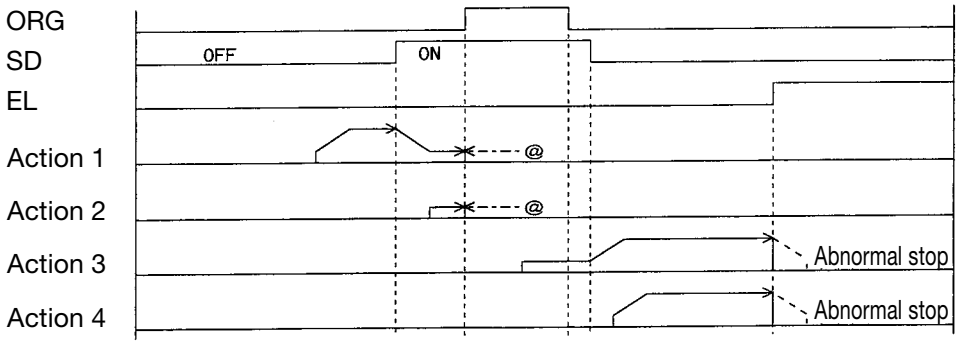


Varied-Speed Operation [Sensor: EL (ELM = 1), ORG]

Though it does not return to the origin position even at normal stop, the value of counter 2 (mechanical position) is reliable



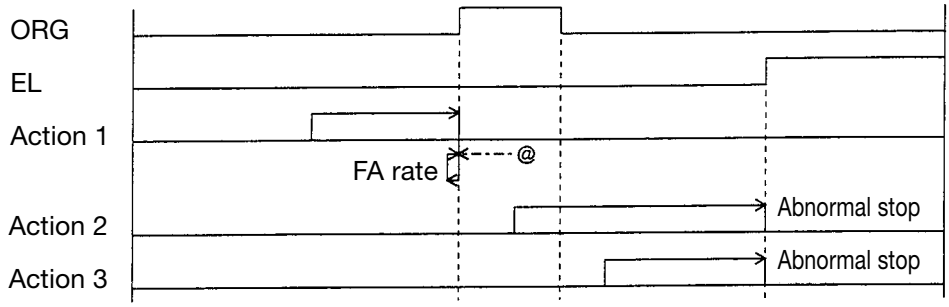
Varied-Speed Operation [Sensor: EL (ELM = 1), SD (SDM = 0, SDLT 0), ORG]



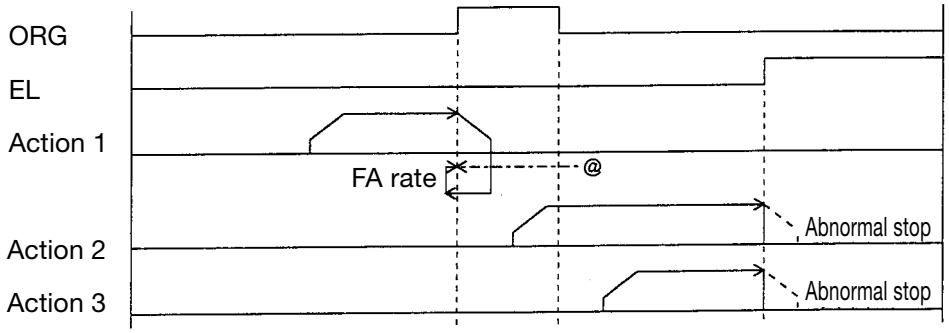
Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return.

9.5.1.2 Origin Return Operation 1 (ORM = 0001)

Constant-speed Operation [Sensor: EL (ELM = 0), ORG]

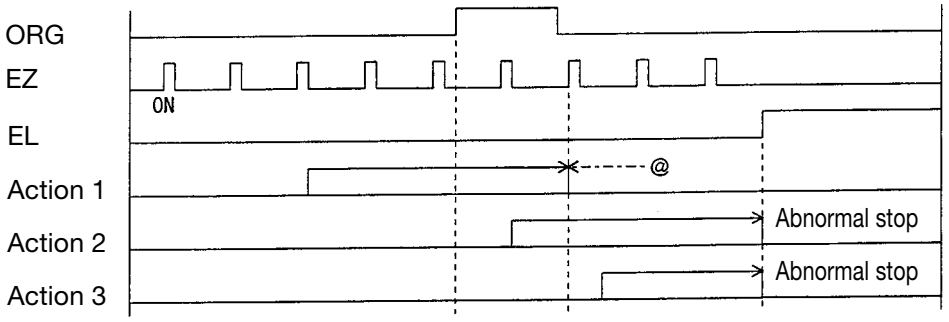


Varied-speed Operation [Sensor: EL, ORG]

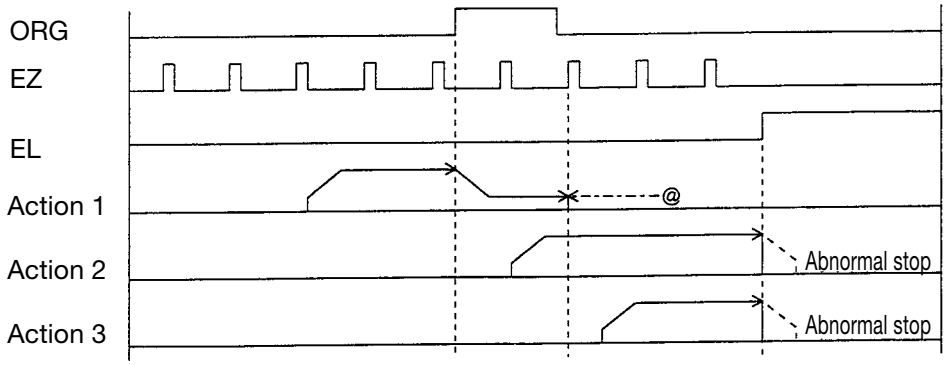


9.5.1.3 Origin Return Operation 2 (ORM = 0010)

Constant-speed Operation [Sensor: EL (ELM = 0), ORG, EZ (EZD = 0001)]



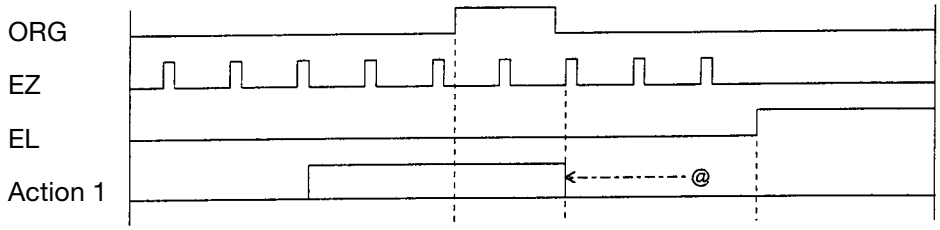
Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001]



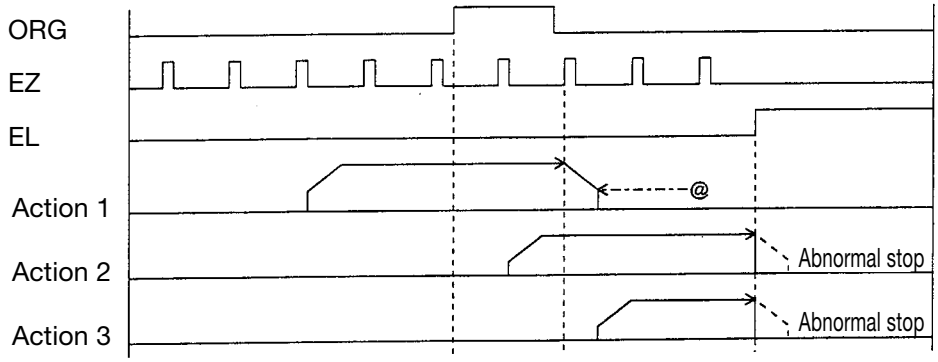
Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return.

9.5.1.4 Origin Return Operation 3 (ORM = 0011)

Constant-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]

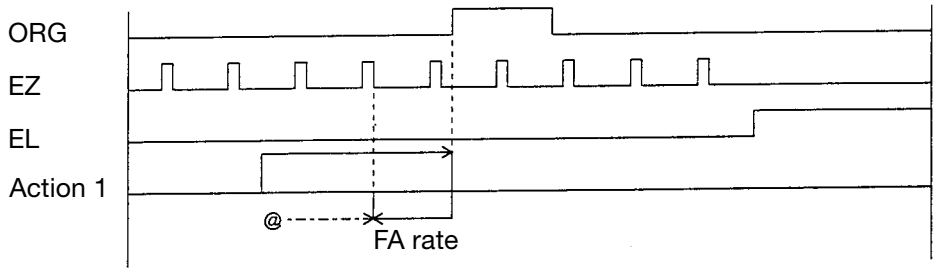


Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]

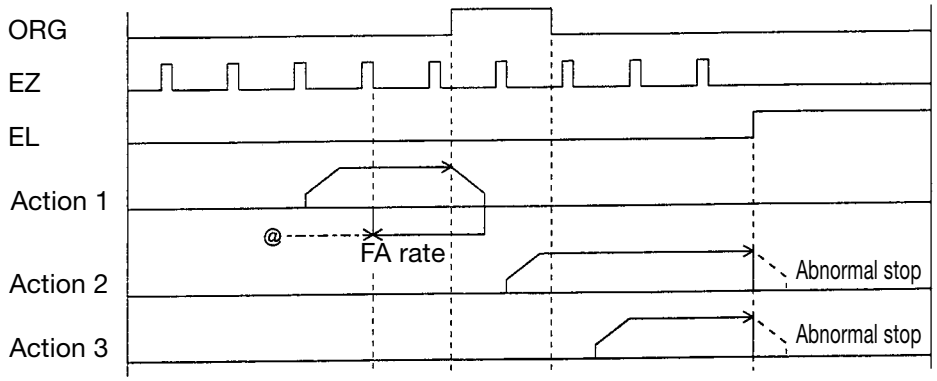


9.5.1.5 Origin Return Operation 4 (ORM = 0100)

Constant-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]



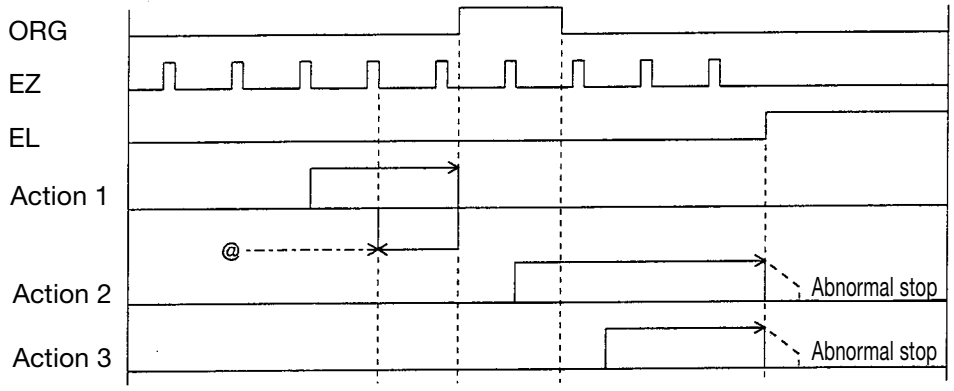
Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]



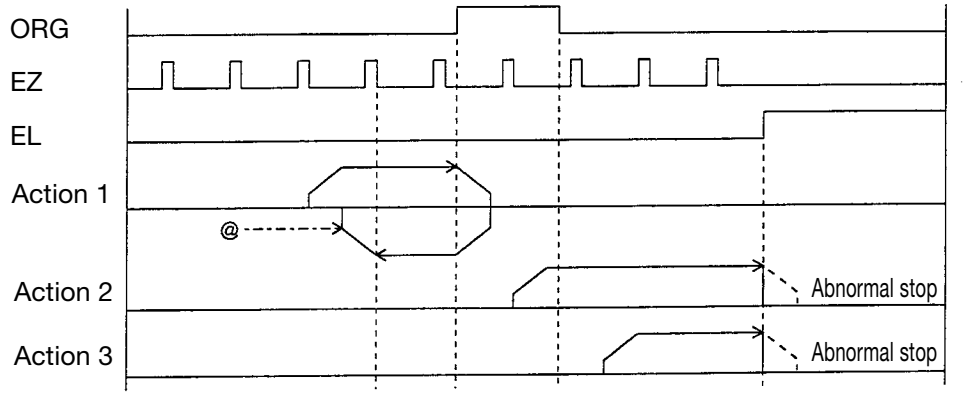
Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return.

9.5.1.6 Origin Return Operation 5 (ORM = 0101)

Constant-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]

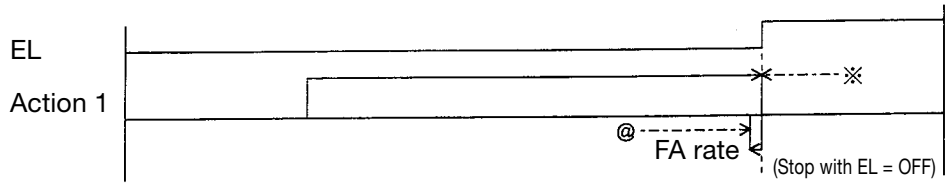


Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]

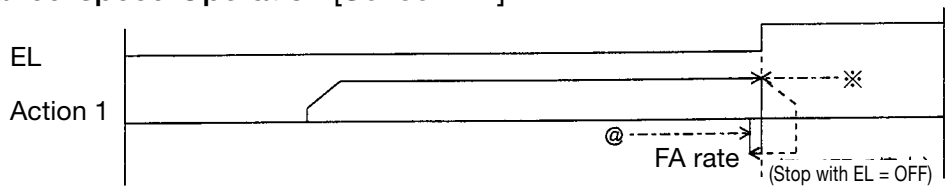


9.5.1.7 Origin Return Operation 6 (ORM = 0110)

Constant-speed Operation [Sensor: EL]



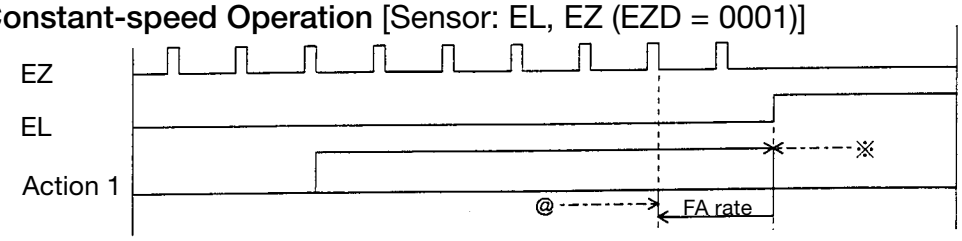
Varied-speed Operation [Sensor: EL]



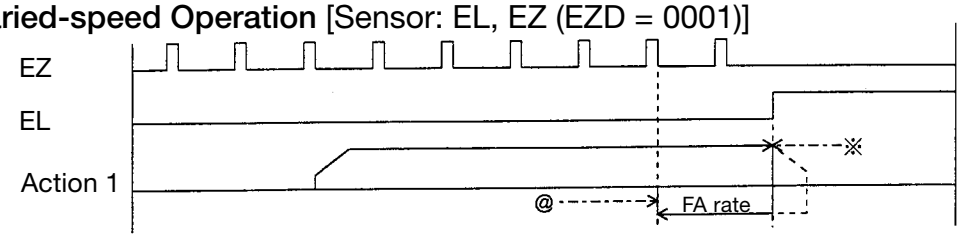
Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return. The ERC signal is also output at ※ position if bit 10 (EROE) of the RENV1 register is set at 1 and bit 3 (ELM), at 0.

9.5.1.8 Origin Return Operation 7 (ORM = 0111)

Constant-speed Operation [Sensor: EL, EZ (EZD = 0001)]

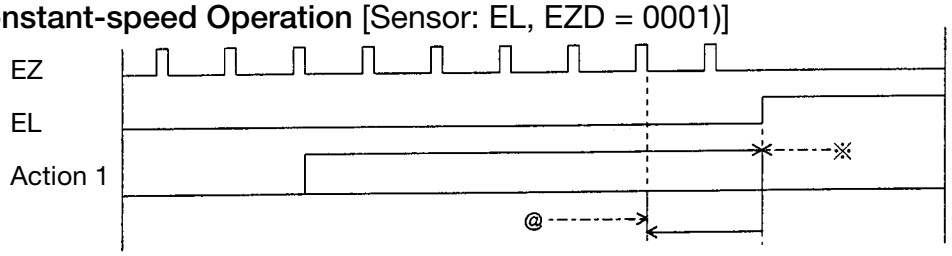


Varied-speed Operation [Sensor: EL, EZ (EZD = 0001)]

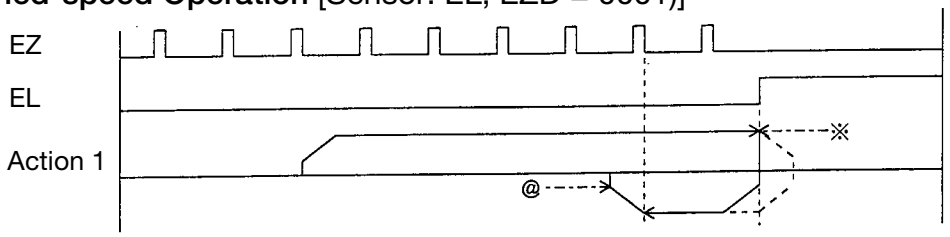


9.5.1.9 Origin Return Operation 8 (ORM = 1000)

Constant-speed Operation [Sensor: EL, EZD = 0001)]

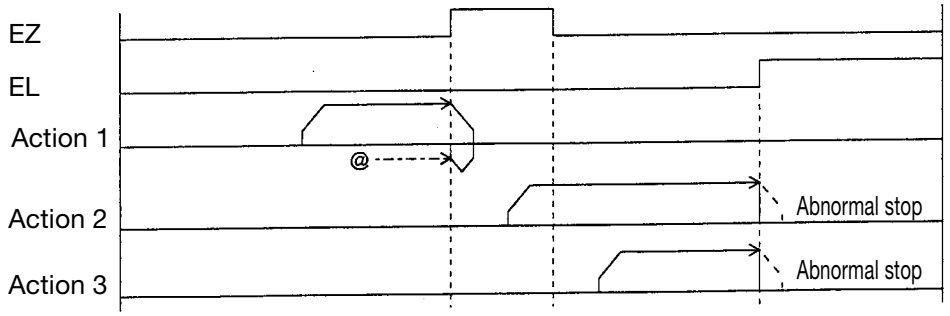


Varied-speed Operation [Sensor: EL, EZD = 0001)]



9.5.1.10 Origin Return Operation 9 (ORM = 1001)

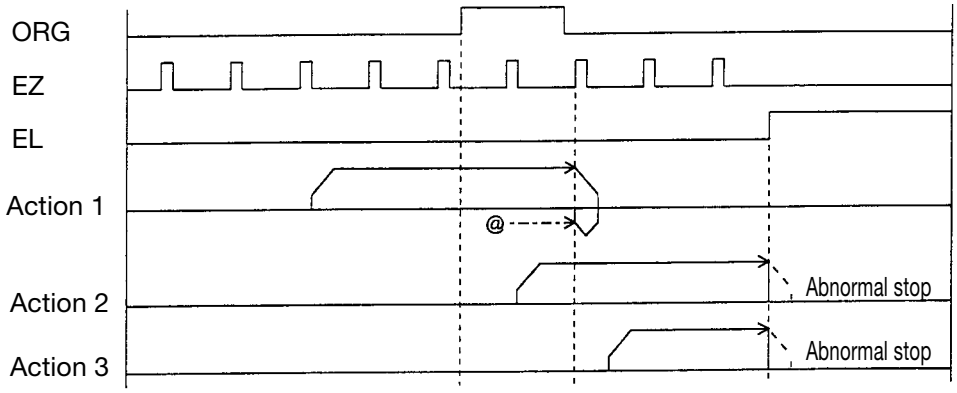
Varied-speed Operation [Sensor: EL, ORG]



Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return. The ERC signal is also output at ※ position if bit 10 (EROE) of the RENV1 register is set at 1 and bit 3 (ELM), at 0.

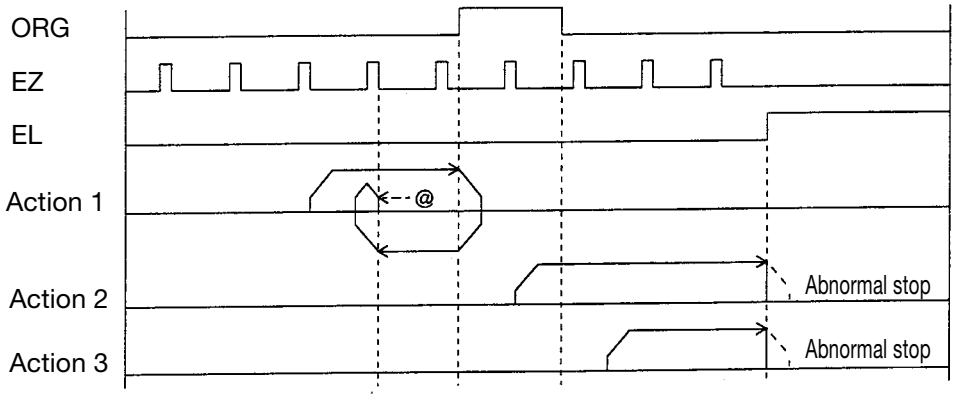
9.5.1.11 Origin Return Operation 10 (ORM = 1010)

Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]



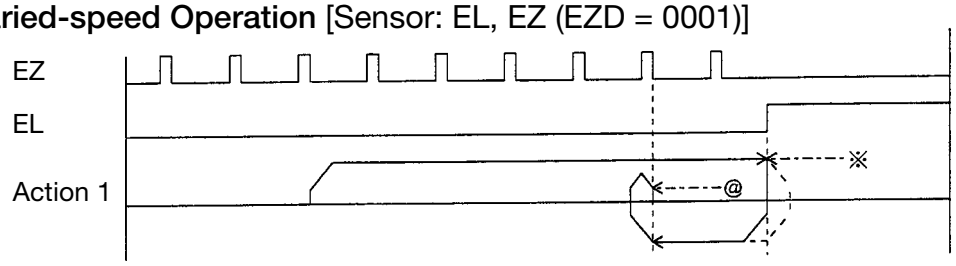
9.5.1.12 Origin Return Operation 11 (ORM = 1011)

Varied-speed Operation [Sensor: EL, ORG, EZ (EZD = 0001)]



9.5.1.13 Origin Return Operation 12 (ORM = 1100)

Varied-speed Operation [Sensor: EL, EZ (EZD = 0001)]



Note: @ position is the ERC signal output timing with “automatic output of ERC signal” made valid at the stop of origin return. The ERC signal is also output at posi- tion if bit 10 (EROE) of the RENV1 register is set at 1 and bit 3 (ELM), at 0.

9.5.2 Origin Escape Mode

After the start command is written, the chip continues generating pulses until it escapes from the origin (ORG signal ON status). Be sure to write the start command for constant-speed operation to start the chip in the origin escape mode.

If the start command is written with the ORG signal OFF, the chip does not generate any pulse and is placed in the normal stop condition. If the chip is started at the constant speed with the ORG signal ON, it continues generating pulses and when the ORG signal turns off, it immediately stops generating pulses after outputting one pulse (normal stop).

MOD: 12HEX for origin escape in plus direction
1AHEX for origin escape in minus direction

9.5.3 Origin Search Mode

The origin search mode is the mode providing an additional function to the origin return mode. It enables an origin return in any of the following three ways.

(1) "Origin Return" in reverse direction to the designated direction
The chip is placed in the normal stop condition when it stops due to the ORG singal turning ON after the start command is written.

(2) "Origin Escape by In-positioning" in reverse direction to the designated direction
If the ORG signal is ON at the start, the chip escapes from the origin by in-positioning and then starts origin return operation.

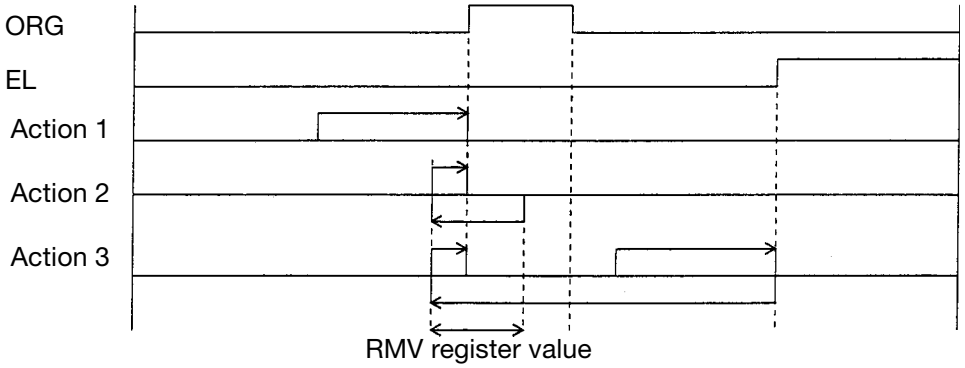
(3) "Origin Return" in the designated direction
If the EL signal in the moving direction stops the chip from generating pulses, it performs "origin return (in the way of ORM = 0000)" in reverse direction and "origin escape by in-positioning" and then performs "origin return" again in the designated direction.

At the time of "origin escape by in-positioning" the chip repeatedly performs in-positioning operation by generating pulses in the number written in the RMV (target position) register until it escapes from the origin. Write a positive value (1 to 134,217,727) to the RMV register.

MOD: 15HEX for origin search in plus direction
1DHEX for origin search in minus direction

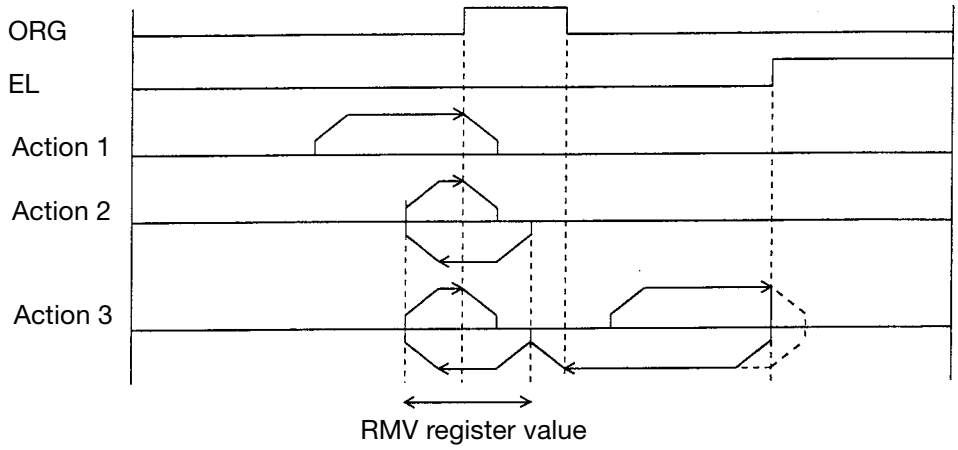
9.5.3.1 Origin Return Operation 0 (ORM = 0000)

Constant-speed Operation [Sensor: EL, ORG]



Varied-speed Operation [Sensor: EL, ORG]

Though it does not return to the origin position even at normal stop, the value of counter 2 (mechanical position) is reliable



9.6 EL or SL Operation Mode

The EL or SL (soft limit) operation mode enables the following operation.

MOD: 20HEX to move to the EL or SL position in plus direction
28HEX to move to the EL or SL position in minus direction
22HEX to escape from the EL or SL position in plus direction
2AHEX to escape from the EL or SL position in minus direction

The input logic of ±EL signals is set by the ELL input pin and the action (immediate stop or stop after deceleration) initiated by the EL signal ON is selected by the RENV1 (environmental setting 1) register. The pin status can be checked by reading the sub status (SSTSW).

For setting of SL (soft limit), refer to "11.11.2 Soft Limit Function."

To select the input logic of ±EL signals, set the ELL input pin.

Low level: Positive logic
High level: Negative logic

To select the action initiated by the EL signal ON, set bit 3 (ELM) of the REVN1 register.

0: Immediate stop
1: Stop after deceleration

To check the ±EL signal status, read bits 12 (SPEL) and 13 (SMEL) of SSTSW.

SPEL = 0: +EL signal OFF SPEL = 1: +EL signal ON
SMEL = 0: –EL signal OFF SMEL = 1: –EL signal ON

To insert the ±EL input filter, set bit 26 (FLTR) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidth shorter than 4µs are ignored.

9.6.1 Moving to EL or SL Position

The chip generates pulses until the EL or SL signal turns on, and is then placed in the normal stop condition. If the start command is written with the EL or SL signal ON, the chip does not generate any pulse and is placed in the normal stop condition. If started with both EL and SL signals OFF, the chip stops generating pulses when the EL or SL signal turns on (normal stop).

MOD: 20HEX for moving to +EL or –SL position
28HEX for moving to –EL or –SL position

9.6.2 Escape from EL or SL Position

The chip generates pulses until the EL or SL signal turns off. If the start command is written with both EL and SL signals OFF, the chip does not generate any pulse and is placed in the normal stop condition. If started with both EL and SL signals ON, the chip generates pulses until the EL or SL signal turns on.

MOD: 22HEX for escape from –EL or –SL position
2AHEX for escape from +EL or +SL position

9.7 EZ Count-Based Mode

In this mode the chip generates pulses until the EZ signal is counted in the number written in the RENV3 register (EZD setting value – 1).

MOD: 24HEX for operation in the preset number of EZ signals in plus direction
2CHEX for operation in the preset number of EZ signals in minus direction

After the start command is written, the chip immediately stops generating pulses or stops after deceleration when the EZ signal is counted in the preset number. The setting range of counting EZ signals is 1 to 16. For this mode, use the start command for constant-speed operation (50HEX or 51HEX). If started for the varied-speed operation, counting the EZ signal in the preset number lets the chip start deceleration before stop, thereby going beyond the EZ position.

The input logic of EZ signal is set by the RENV2 (environmental setting 2) register and the number of counting EZ signals is set by the RENV3 (environmental setting 3) register. The pin status can be checked by reading the extension status (RSTS).

To select the input logic of EZ signal, set bit 23 (EZL) of the RENV2 register.
0: Falling edge
1: Rising edge

To select the number of counting EZ signals, set bits 7-4 (EZD3-0) of the RENV3 register at a value of (counting number – 1) in a range of 0 to 15. The number will be used as a condition to complete an origin return.

To check the EZ signal status, read bit 10 (SEZ) of the RSTS register.
0: EZ signal OFF
1: EZ signal ON

9.8 Interpolation

9.8.1 Interpolation

Besides independent operation of each axis, the chip provides the following interpolation modes.

MOD: 60HEX for continuous linear operation 1 among two to four axes
61HEX for linear interpolation 1 among two to four axes
62HEX for continuous linear interpolation 2 among one to four axes
63HEX for linear interpolation 2 among one to four axes
64/65HEX for circular interpolation between two axes in CW/CCW

Like in the linear interpolation, the chip generates pulses for plural axes at a preset ratio but in the continuous linear interpolation it starts and stops based on start and stop commands like in the continuous operation mode.

The linear interpolation 1 is used for interpolation among two to four axes of the chip. The linear interpolation 2 is used for linear interpolation among five or more axes of two or more chips. The axes which are not subjected to interpolation can be independently operated.

The interpolation setting condition and the operation status can be checked by reading the RIPS (interpolation status) register. The RIPS register is a common register to all axes and, therefore, the content is same if it is read from any axis.

Write the start or stop command to all interpolation axes by setting SELx to SELu of COMB1.

The chip allows combination of the following interpolations.

(1) Linear interpolation 1 between two axes
(2) Linear interpolation 1 among three axes
(3) Linear interpolation 1 among four axes
(4) Circular interpolation between two axes
(5) Linear interpolation 1 between two axes and circular interpolation between two axes

Independent operation or linear interpolation 2 can be applied to the axes which are not used for interpolations (1) to (5).

9.8.2 Interpolation Control Axis

For circular interpolation and linear interpolation 1, the speed is set for one axis which is called the interpolation control axis. It is defined in the order of X, Y, Z and U axes among those used for interpolation. If circular interpolation and linear interpolation 1 are done simultaneously, two axes are interpolation control axes. In linear interpolation 2, each concerned axis is interpolation control axis.

Relation between Interpolation and Interpolation Control Axis

No.	Interpolation	Interpolation control axis
1	Linear interpolation 1 among X, Y, Z and U axes	X
2	Linear interpolation 1 among X, Y and Z axes	X
3	Linear interpolation 1 among Y, Z and U axes	Y
4	Linear interpolation 1 between Y and U axes	Y
5	Circular interpolation between X and U axes	X
6	Circular interpolation between X and Z axes and linear interpolation 1 between Y and U axes	X for circular interpolation Y for linear interpolation 1

9.8.3 Composite Speed Constant Control

This function is to keep constant the composite speed of the axes to which linear interpolation 1 and circular interpolation are applied. This function is not available for linear interpolation 2.

To effect the function, set the bit 15 (MIPF) of the RMD (operation mode) register of the axes to which the composite speed constant control is applied at 1. In the same interpolation mode, the time to the next output is multipled by $\sqrt{2}$ if pulse output is simultaneously done to two axes among these of which MIPF is set at 1, multiplied by $\sqrt{3}$ if pulse output is simultaneously done to three axes. The composite speed constant control are available for two or three axes. If the MIPF of four axes is set at 1 in linear interpolation 1 among four axes. The time to the next output is multiplied by $\sqrt{3}$ when pulse output is simultaneously done to four axes.

The speed (FH or FL) of the interpolation control axis becomes the composite speed when the composite speed constant control is made valid by setting MIPF at 1. SRUN, SEND and SERR of the main status (MSTSW) register of interpolation axes change similarly. Also, only data of the interpolation control axis is effective for RSPD (speed monitor) register. However, in linear interpolation 2, the speed of the main axis is read.

9.8.4 Linear Interpolation 1

In the linear interpolation (MOD: 61HEX), interpolation among desired two to four axes of the chip is made. If started with only one axis designated for interpolation, an error results (ESDT: stop due to abnormal operation data). After setting the interpolation control axis at the operation speed, set the RMD register of all concerned interpolation axes for the composite speed constant control and write the ending position to the RMV register. The moving direction depends on the sign of RMV register.

The axis providing a maximum moving amount (the highest absolute value of RMV register) is automatically made the main axis and other axes become slave axes.

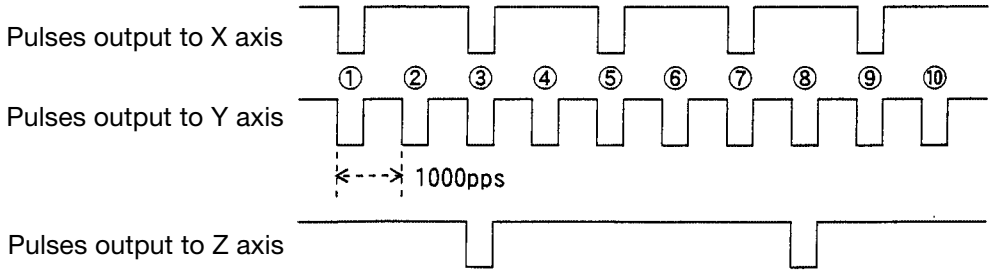
When the start command is written, the chip generates pulses constantly to the main axis and intermittently to slave axes (with pulses omitted in some intervals from those of the main axis). Write the start command to all interpolation axes.

In the continuous linear interpolation 1 (MOD: 60HEX), the chip generates pulses at the same timing as in the linear interpolation 1 but does not stop until the stop command is written.

Setting Sample

Set the chip as shown on the table below and write the start command (e.g. 0751HEX) to all interpolation axes. The chip will generate pulses at the timing shown below. If data is written in the blank field on the table, it does not give any effect to the operation.

	X axis	Y axis	Z axis
MOD	61HEX	61HEX	61HEX
MIPF	0 (OFF)	0 (OFF)	0 (OFF)
RMV value	5	10	2
Operation speed	1000pps		
Interpolation control axis	Yes	—	—
Main/slave axis	Slave	Main	Slave



9.8.5 Linear Interpolation 2

The linear interpolation 2 (MOD: 63HEX) is mainly used for linear interpolation among five or more axes selected from plural chips. Use the simultaneous start signal ($\overline{\text{CSTA}}$) for interpolation between plural chips. For details on the $\overline{\text{CSTA}}$ signal, refer to "11.7 External Start/Simultaneous Start."

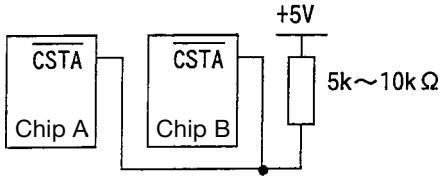
The axis providing the largest moving amount among interpolation axes is made the main axis and other axes are slave axes. Set the RIP register of all axes including the main axis at the value of RMV register of main axis. Set the RMV register of slave axes at their respective ending position. Set speed data (RFL, RFH, RUR, RDR, RMG, RDP, RUS and RDS) of slave axes at the same values as the main axis. The moving direction depends on the sign of RMV register value.

After setting bits 19-18 (MSY) of the RMV (operation mode) register of interpolation axes at 01, write the start command to make the chips ready for $\overline{\text{CSTA}}$ signal input. Then, send the $\overline{\text{CSTA}}$ signal to start all concerned chips generating pulses simultaneously. The main axis generates pulses constantly and slave axes intermittently generate pulses (with pulses omitted in some intervals from those of the main axis).

In the continuous linear interpolation 2 (MOD: 62HEX), pulses are output at the same timing as in the linear interpolation 2 but operation does not stop until the stop command is written.

Setting Sample

(1) Connect chips A and B through $\overline{\text{CSTA}}$ pin.



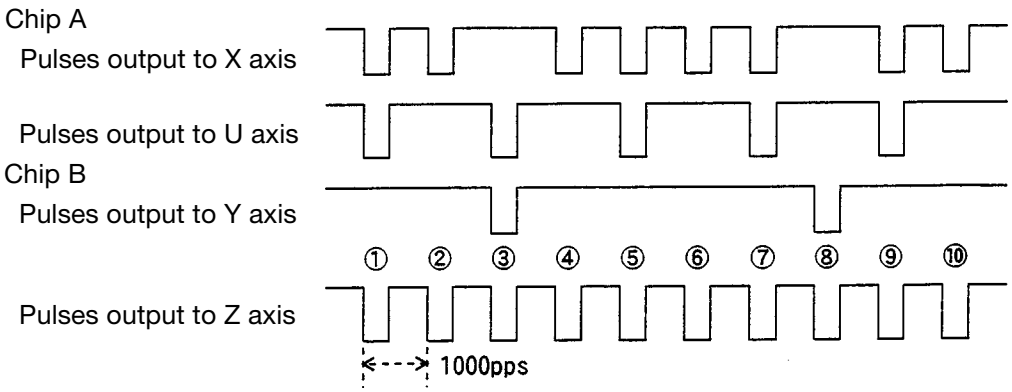
(2) Set chips A and B as shown on the table below. (RMD is set for starting with $\overline{\text{CSTA}}$ signal input.

(3) Write the start command to all axes (0951HEX for chip A and 0651HEX for chip B).

(4) Write the $\overline{\text{CSTA}}$ signal input command (06HEX) to the X axis of chip A.

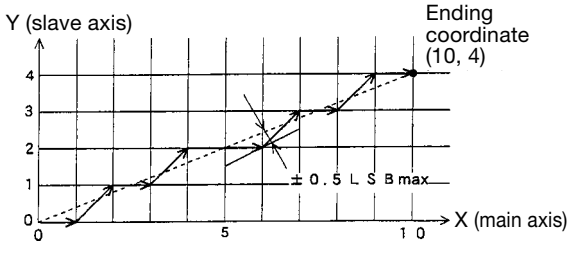
Then, these chips will generate pulses at the timing shown below.

	Chip A		Chip B	
	X axis	U axis	Y axis	Z axis
RMD	00040063HEX	00040063HEX	00040063HEX	00040063HEX
RMV value	8	5	2	10
RIP value	10	10	10	10
Operation speed	1000pps	1000pps	1000pps	1000pps
Main/slave axis	Slave	Slave	Slave	Main



Accuracy of Linear Interpolation

As shown at the right, linear interpolation is made from the present coordinates to the ending coordinates. Accuracy of the position to the designated straight line for linear interpolation is ±0.5 LSB max. in the whole interpolation range.



9.8.6 Circular Interpolation

The chip can perform circular interpolation in CW direction (MOD: 64HEX) or in CCW direction (MOD: 65HEX) between two desired axes. If one, three or four axes are designated for circular interpolation, data setting error occurs at the start. In circular interpolation, the present position is the starting point (coordinates 0, 0) irrespective of values of counters 1 to 4.

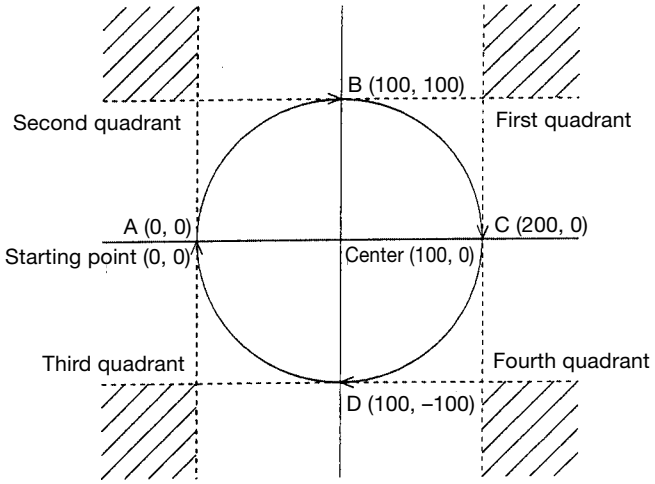
After setting the speed of the interpolation control axis, set the composite speed constant control (MIPF of RMD register) to ON or OFF and set the RMV register at the value of ending position and the RIP register at the value of the center position, with each axis. If the ending position of both axes is 0 (starting point), the result is a complete round.

The composite speed in circular interpolation is the speed (FL or FH) of the interpolation control axis if the composite speed constant control of both axes is set to ON (MIPF = 1). The start command should be written to both axes.

Setting Sample

Set the chip as shown on the table below and write the start command to both axes. Operation results will be as illustrated.

Action No.	A		B		C		D	
	X axis	Y axis	X axis	Y axis	X axis	Y axis	X axis	Y axis
MOD	64HEX (circular interpolation in CW direction)							
MIPF	1 (composite speed constant control ON)							
RMV value	0	0	100	100	200	0	100	–100
RIP value	100	0	100	0	100	0	100	0
Operation result	Complete round		Circular arc of 90°		Circular arc of 180°		Circular arc of 270°	

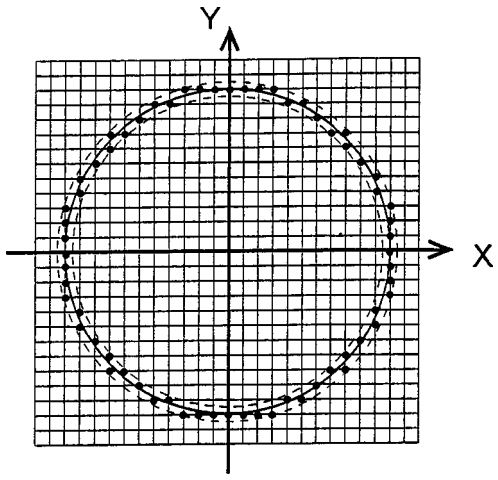


In the case of circular interpolation, it is complete at the position where an axis reaches the ending position in the ending quadrant and does not come to the designated coordinates. If in-positioning operation (MOD: 41HEX) is executed after completing circular interpolation by writing the restart command to output remaining pulses, it moves from the ending point of circular interpolation to the ending point coordinates.

If the ending point of circular interpolation is in any area filled with slant lines, it does not stop and endlessly rotates.

Accuracy of Circular Interpolation

Circular interpolation is made from the present coordinates to the ending coordinates while drawing a circular arc. Accuracy of the position to the designated circular arc is ±0.5 LSB in the whole interpolation range. The figure at the right is a sample where a complete round with a radius of 11 is drawn.



•: Interpolation locus
Solid line: Round with a radius of 11
Dotted line: Round with a radius of 11 ±0.5

9.8.7 Operations Available on the Way of Interpolation

Acceleration/Deceleration

For linear interpolation, linear or S-curve acceleration and deceleration, as well as automatic ramping-down point setting, are available. For circular interpolation, acceleration and deceleration cannot be executed.

Error-initiated Stop

If any interpolation axis stops due to error, all other interpolation axes stop correspondingly (SERR = 1). The error axis can be judged by reading the REST (error stop factor) register.

SD Input

If the SD input is made valid by setting bit 8 (MSDE) of the RMD register at 1, all interpolation axes decelerate or stop after deceleration when the SD pin of any of interpolation axes turns on.

Idling Control

Acceleration is not made if any of interpolation axes is in the idling range.

Correction Function

Backlash correction and slip correction are not available during interpolation. Set the correction function to OFF by setting bit 13-12 of the RENV6 register at 00.

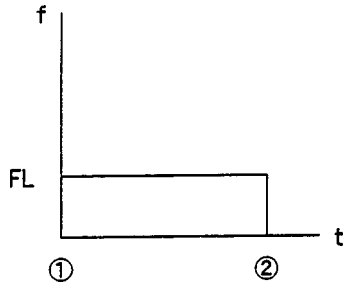
Continuous Interpolation

Use of preregister enables continuous interpolation. For a setting sample of continuous interpolation using preregister, refer to “11.14.1 Starting by Stop of Other Axis.”

10. Speed Patterns

10.1 Speed Patterns

10.1.1 Constant-speed Operation at FL Rate



In continuous mode

① The start command (50HEX) for constant-speed operation at FL rate is written.

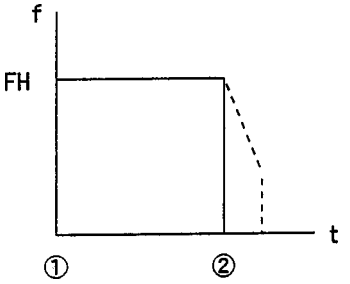
② The immediate stop command (49HEX) or the stop-after-deceleration command (4AHEX) is written.

In in-positioning mode

① The start command (50HEX) for constant-speed operation at FL rate is written.

② The in-positioning counter counts down to 0, the immediate stop command (49HEX), or the stop-after-deceleration command (4AHEX) is written.

10.1.2 Constant-speed Operation at FH Rate



In continuous mode

① The start command (51HEX) for constant-speed operation at FH rate is written.

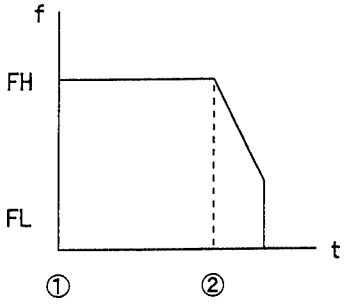
② The immediate stop command (49HEX) is written. If the stop-after-deceleration command (4AHEX) is written, deceleration starts.

In in-positioning mode

① The start command (51HEX) for constant-speed operation at FH rate is written.

② The in-positioning counter counts down to 0 or the immediate stop command (49HEX) is written. If the stop-after-deceleration command (4AHEX) is written, deceleration starts.

10.1.3 Varied-speed Operation 1



In continuous mode

① The start command (52HEX) for varied-speed operation 1 is written.

② The stop-after-deceleration command (4AHEX) is written.

If the immediate stop command (49HEX) is written, it stops immediately without deceleration.

In in-positioning mode

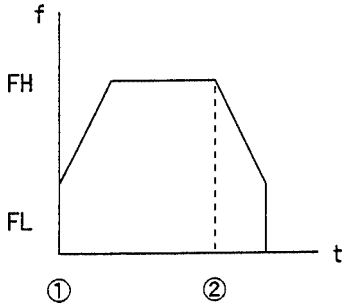
① The start command (52HEX) for varied-speed operation 1 is written.

② The ramping-down point is reached or the stop-after-deceleration command (4AHEX) is written.

In in-positioning operation using the start command (52HEX) for varied-speed operation 1, ramping-down point setting is limited to manual setting irrespective of setting of bit 13 (MSDP) of the RMD register. If the ramping-down point is set at 0 (RDP = 0), it stops immediately.

If the immediate stop command (49HEX) is written, it stops immediately.

10.1.4 Varied-speed Operation 2



In continuous mode

① The start command (53HEX) for varied-speed operation 2 is written.

② The stop-after-deceleration command (4AHEX) is written.

If the immediate stop command (49HEX) is written, it stops immediately without deceleration.

In in-positioning mode

① The start command (53HEX) for varied-speed operation 2 is written.

② The ramping-down point is reached or the stop-after-deceleration command (4AHEX) is written.

If the ramping-down point is manually set (MSDP of RMD = 1), and the ramping-down point is set at 0 (RDP = 1), it stops immediately.

If the stop-after-deceleration comand (49HEX) is written it stops immediately.

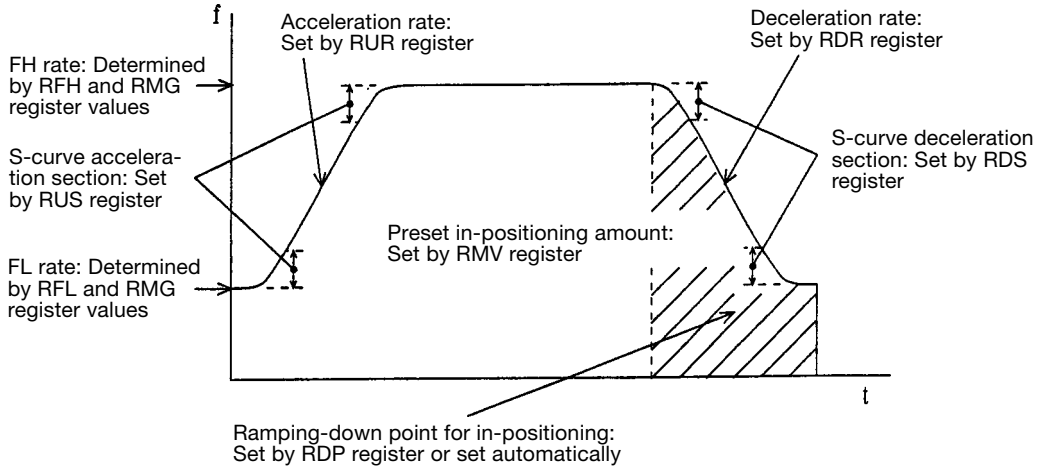
10.2 Setting Speed Pattern

To set a speed pattern, use the registers (or preregisters) listed on the table below. If the setting is the same as previous, you do not need to rewrite.

Register	Content	Bit length	Setting range	Pre-register
RMV	In-positioning amount	28	–134,217,728 (8000000HEX) to 134,217,727 (7FFFFFFHEX)	PRMV
RFL	Initial (or low) speed	16	1 to 65,535 (0FFFFHEX)	PRFL
RFH	Operation (or high) speed	16	1 to 65,535 (0FFFFHEX)	PRFH
RUR	Acceleration rate	16	1 to 65,535 (0FFFFHEX)	PRUR
RDR	Deceleration rate*	16	0 to 65,535 (0FFFFHEX)	PRDR
RMG	Speed multiplication factor	12	2 to 4,095 (0FFFHEX)	PRMG
RDP	Ramping-down point	24	0 to 16,777,215 (0FFFFFFHEX)	PRDP
RUS	S-curve acceleration range	15	0 to 32,767 (7FFFHEX)	PRUS
RDS	S-curve deceleration range	15	0 to 32,767 (7FFFHEX)	PRDS

* If the RDR register is set at 0, the acceleration rate written to the RUR register is used for deceleration.

Sites to which register data are applied for acceleration and deceleration



10.2.1 RFL: FL Rate Setting Register, 16-bit

This register sets the speed of constant-speed operation at FL rate or the initial speed of varied-speed operation. The setting range is 1 to 65,535 (0FFFFHEX). The practical FL rate is the value obtained through the following equation:

$$\text{FL rate (pps)} = \text{RFL} \times \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

10.2.2 RFH: FH Rate Setting Register, 16-bit

This register sets the speed of constant-speed operation at FH rate or the high speed of varied-speed operation. The setting range is 1 to 65,535 (0FFFF$_{HEX}$). The practical FH rate is the value obtained through the following equation:

$$\text{FH rate (pps)} = \text{RFH} \times \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

10.2.3 RUR: Acceleration Rate Setting Register, 16-bit

This register sets the acceleration rate in varied-speed operation. The setting range is 1 to 65,535 (0FFFF$_{HEX}$). The setting value and acceleration time have the following relations:

In the case of linear acceleration (MSMD of RMD register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RUR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve acceleration with no linear section (MSMD of RMD register = 1 and RUS register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RUR} + 1) \times 8}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve acceleration with linear section (MSMD of RMD register = 1 and RUS register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL} + 2 \times \text{RUS}) \times (\text{RUR}) + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

10.2.4 RDR: Deceleration Rate Setting Register, 16-bit

Usually, this register sets the deceleration rate in varied-speed operation in a range of 1 to 65,535 (0FFFF$_{HEX}$). If the ramping-down point is automatically set, the RDR register value is used as deceleration rate. If this RDR register is set at 0, the RUR register value is used for deceleration.

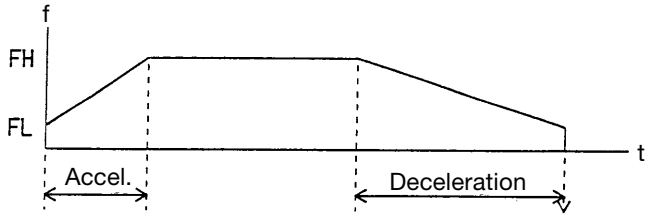
When setting the ramping-down point automatically, set so that:

The deceleration time is equal to, or shorter than, (acceleration time x 2) for the independent operation;

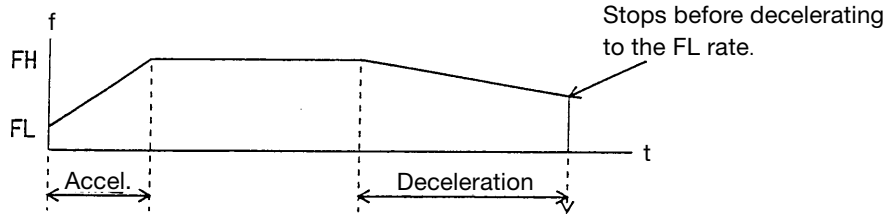
The deceleration time is equal to the acceleration time for the interpolated operation.

If the deceleration time is longer than (acceleration time x 2) in the independent operation or if it is longer than the acceleration time in the interpolated operation, the chip may not decelerate to the FL rate before stop. In such a case, therefore, set MSDP of the RMD register at 1 to effect the manual setting of ramping-down point.

Ramping-down point automatically set with (deceleration time) ≤ (acceleration time x 2).



Ramping-down point automatically set with (deceleration time) ≥ (acceleration time x 2).



The setting value and deceleration time have the following relations:

In the case of linear deceleration (RSMD of RMD register = 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{PDR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve deceleration with no linear section (MSMD of RMD register = 1 and RDS register = 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RDR} + 1) \times 8}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve deceleration with linear section (MSMD of RMD register = 1 and RDS register > 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL} + 2 \times \text{RDS}) \times (\text{RDR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

10.2.5 RMG: Multiplication Setting Register, 12-bit

This register sets the value by which the RFL and RFH register values are multiplied to provide the practical pulse output rate. The setting range is 2 to 4,095 ($0FFF_{HEX}$). The higher the setting value, the coarser the setting rate; therefore, use the smallest possible multiplication. The setting value has the following relation with the multiplication.

$$\text{Multiplication} = \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

Typical Settings of multiplication with reference clock = 19.6608MHz

Setting value	Multiplication	Range of output pulse rate in pps
2999 ($0BB7_{HEX}$)	0.1	0.1 to 6,553.5
1499 ($5DB_{HEX}$)	0.2	0.2 to 13,107.0
599 (257_{HEX})	0.5	0.5 to 32,767.5
299 ($12B_{HEX}$)	1	1 to 65,535
149 (95_{HEX})	2	2 to 131,070
59 ($3B_{HEX}$)	5	5 to 327,675
29 ($1D_{HEX}$)	10	10 to 655,350
14 ($0E_{HEX}$)	20	20 to 1,310,700
5 (5_{HEX})	50	50 to 3,276,750
2 (2_{HEX})	100	100 to 6,553,500

10.2.6 RDP: Ramping-down Point Setting Register, 24-bit

This register sets the value to determine the starting point of deceleration in acceleration/deceleration and in-positioning. Meaning of the value written to the RDP register differs depending on the ramping-down point setting method (MSDP) of the RMD register.

When MSDP of the RMD register is set at 1 (manual setting)

Set the deceleration starting point in the number of pulses in a range of 0 to 16,777,215 ($0FFFFFF_{HEX}$). An optimum value of the ramping-down point is obtained through the following equation.

(1) Linear deceleration (MSMD of RMD register = 0)

$$\text{Optimum value (pulses)} = \frac{(RFH^2 - RFL^2) \times (RDR + 1)}{(RMG + 1) \times 32768}$$

However, if triangular drive is done with the FH correction function OFF (MADJ of RMD register = 1) and with RFH register value not changed, an optimum value is obtained through the following equation. (If idling control is used, substitute the value obtained by subtracting the number of idling pulses from the RMV register value for the RMV in the equation below. The number of idling pulses is 1 to 6 when IDL of RENV5 = 2 to 7.)

$$\text{Optimum value (pulses)} = \frac{RMV \times (RDR + 1)}{PUR + RDR + 2}$$

(2) S-curve deceleration with no linear section (MSMD of RMD register = 1 and RDS register = 0)

$$\text{Optimum value (pulses)} = \frac{(RFH^2 - RFL^2) \times (RDR + 1) \times 2}{(RMG + 1) \times 32768}$$

(3) S-curve deceleration with linear section (MSMD of RMD register = 1 and RDS register > 0)

Optimum value (pulses) =

$$\frac{(RFH + RFL) \times (RFH - RFL + 2 \times RDS) \times (RDR + 1)}{(RMG + 1) \times 32768}$$

Deceleration starts when the in-position counter value becomes equal to, or lower than RDP setting value.

When MSDP of RMD register is set at 0 (automatic setting)

The RDP register value offsets the automatically set ramping-down point. The setting range is –8,388,608 (800000_{HEX}) to 8,388,607 ($7FFFFFF_{HEX}$). If the offset value is positive, deceleration starts earlier and after deceleration the chip generates pulses at the FL rate. If the offset value is negative, start of deceleration is delayed. If offset is not required, set the register at 0.

If the ramping-down point setting value is smaller than the optimum value, the chip stops generating pulses at a rate higher than the FL rate. On the contrary, if the value is larger than the optimum value, the chip performs constant-speed operation at the FL rate after deceleration.

10.2.7 RUS: S-curve Acceleration Range Setting Register, 15-bit

This register sets the S-curve acceleration section in a range of 1 to 32,767 ($7FFF_{HEX}$). The S-curve acceleration section S_{SU} is obtained through the following equation:

$$S_{SU}\ (pps) = RUS \times \frac{\text{Reference clock frequency (Hz)}}{(RMG + 1) \times 65536}$$

That is, S-curve acceleration is made in the sections from the FL rate to (FL rate + S_{SU}) and from the (FH rate – S_{SU}) to the FH rate. And linear acceleration is applied to the section in between. If the register is set at 0, a value obtained through internal calculation of (RFH – RFL)/2 is substituted, resulting in S-curve acceleration with no linear acceleration section.

10.2.8 RDS: S-curve Deceleration Range Setting Register, 15-bit

This register sets the S-curve deceleration section in a range of 1 to 32,767 ($7FFF_{HEX}$). The S-curve deceleration section S_{SD} is obtained through the following equation:

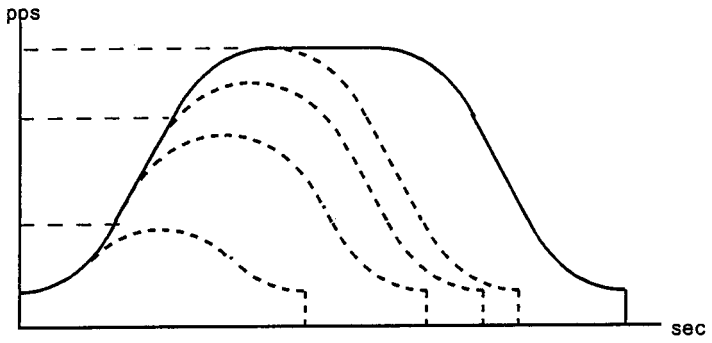
$$SSD\ (pps) = RDS \times \frac{\text{Reference clock frequency (Hz)}}{(RMG + 1) \times 65536}$$

That is, S-curve acceleration is made in the sections from the FH rate to (FH rate – S_{SD}) and from (FL + S_{SD}) to FL rate. If the register is set at 0, a value obtained through internal calculation of (RFH – RFL)/2 is substituted, resulting in S-curve deceleration with no linear acceleration section.

10.3 Manual FH Correction

If the FH correction function is made valid by setting MADJ of RMD register at 0, triangular drive can be avoided by automatically reducing the FH rate against less moving amount at the time acceleration/deceleration is applied for in-positioning. However, do not use the FH correction function if RUR and PDR registers are set to make the deceleration time longer than (acceleration time x 2).

To avoid triangular drive with the FH correction function made invalid by setting MADJ of the RMD register at 1, it is required to change the FH rate in advance. (If idling control is used, substitute the value obtained by subtracting the number of idling pulses from the RMV register value for the RMV in the equations below. The number of idling pulses is 1 to 6 when IDL of RENV5 register = 2 to 7.)



Maximum speed is automatically adjusted according to moving amount

For manual FH correction

(1) Linear acceleration/deceleration (MSMD of RMD register = 0)

$$\text{When RMV} \leq \frac{(RFH^2 - RFL^2) \times (RUR + RDR + 2)}{(RMG + 1) \times 32768}$$

$$RFH \leq \sqrt{\frac{(RMG + 1) \times 32768 \times RMV}{RUR + RDR + 2} + RFL^2}$$

(2) S-curve acceleration/deceleration with no linear section (MSMD of RMD register = 1, RUS register = 0 and RDS register = 0)

$$\text{When RMV} \leq \frac{(RFH^2 - RFL^2) \times (RUR + RDR + 2) \times 2}{(RMG + 1) \times 32768}$$

$$RFH \leq \sqrt{\frac{(RMG + 1) \times 32768 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

(3) S-curve acceleration/deceleration with linear acceleration section (MSMD of RMD register = 1, RUS register > 0 and RDS register > 0)

(3)-1. When RUS = RDS

• To shorten the linear acceleration/deceleration section

$$\text{When RMV} \leq \frac{(RFH + RFL) \times (RFH - RFL + 2 \times RUS) \times (RUR + RDR + 2)}{(RMG + 1) \times 32768}$$

$$\text{and RMV} > \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

$$RFH \leq -RUS + \sqrt{(RUS - RFL)^2 + \frac{(RMG + 1) \times 32768 \times RMV}{(PUR + RDR + 2)}}$$

• To eliminate linear acceleration/deceleration section

$$\text{When RMV} \leq \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

Change to S-curve acceleration/deceleration with no linear acceleration/deceleration section (by setting RUS = 0, RDS =), then

$$RFH \leq \sqrt{\frac{(RMG + 1) \times 32768 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

(3)-2. When RUS < RDS

• To shorten the linear acceleration/deceleration section

$$\text{When RMV} \leq \frac{(RFH + RFL) \times [(RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)]}{(RMC + 1) \times 32768}$$

$$\text{and RMV} > \frac{(RDS + RFL) \times [RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)] \times 4}{(RMG + 1) \times 32768}$$

$$RFH \leq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$$

where, $A = RUS \times (RUR + 1) + RDS \times (RDR + 1)$

$B = [(RMG + 1) \times 32768 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2] \times (RUR + RDR + 2)$

• To eliminate linear deceleration section and shorten linear acceleration section

$$\text{When RMV} \leq \frac{(RDS + RFL) \times [RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)] \times 4}{(RMG + 1) \times 32768}$$

$$\text{and RMV} > \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

Change to S-curve acceleration/deceleration with no linear acceleration/deceleration section by setting RUS > 0, RDS = 0, then

$$RFH \leq \frac{-A + \sqrt{A^2 + B}}{RUR + 2 \times RDR + 3}$$

where, $A = RUS\ (RUR + 1)$

$B = [(RMG + 1) \times 32768 \times RMV - 2 \times A \times RFL + (RUR + 2 \times RDR + 3) \times RFL^2] \times (RUR + 2 \times RDR + 3)$

- To eliminate linear acceleration/deceleration

$$\text{When } RMV \leq \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

Change to S-curve acceleration/deceleration with no linear acceleration/deceleration by setting RUS = 0, RDS = 0, then

$$RFH \leq \sqrt{\frac{(RMG + 1) \times 32768 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

(3)-3. When RUS > RDS

- To shorten linear acceleration/deceleration section

When

$$RMV \leq \frac{(RFH + RFL) \times [(RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)]}{(RMG + 1) \times 32768}$$

$$\text{and } RMV > \frac{(RUS + RFL) \times [RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)] \times 4}{(RMG + 1) \times 32768}$$

$$RFH \leq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$$

where, $A = RUS \times (RUR + 1) + RDS \times (RDR) + 1)$

$B = [(RMG + 1) \times 32768 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2) \times (RUR + RDR + 2)$

- To eliminate linear acceleraton section and shoten linear deceleration section

$$\text{When } RMV \leq \frac{(RUS + RFL)\ X\ [RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)] \times 4}{(RMG + 1) \times 32768}$$

$$\text{and } RMV > \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

Change to S-curve acceleration/deceleration with no linear acceleration/deceleration by setting RUS = 0, RDS > 0, then

$$RFH \leq \frac{-A + \sqrt{A^2 + B}}{2 \times RUR + RDR + 3}$$

where, $A = RDS\ (RDR + 1)$

$B = [(RMG + 1) \times 32768 \times RMV - 2 \times A \times RFL + (2 \times RUR + RDR + 3) \times RFL^2] \times (2 \times RUR + RDR + 3)$

• To eliminate linear acceleration/deceleration section

$$\text{When} \leq \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 32768}$$

Change to S-curve acceleration/deceleration with no linear acceleration/deceleration section by setting RUS = 0, RDS = 0, then

$$RFH \leq \sqrt{\frac{(RMG + 1) \times 32768 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

10.4 Setting Speed Pattern with Acceleration/Deceleration

To set, for example, the starting speed at 10 pps, the operation speed at 100 kpps and the acceleration/deceleration time at 300ms with the reference clock = 19.6608MHz.

(1) Select a multiplication of 2 times by setting the RMG register at 149 (95_{HEX}).
(2) Since a multiplication of 2 times is selected, set the RFH register at 50000 ($C350_{HEX}$) to obtain the operation speed of 100 kpps.
(3) Similarly, set the RFL register at 5 (0005_{HEX}) to obtain the starting speed of 10 pps.
(4) To make the acceleration/deceleration time 300ms, set the RUR register at 28.494 based on the relational expression of acceleration time and RUR setting value.

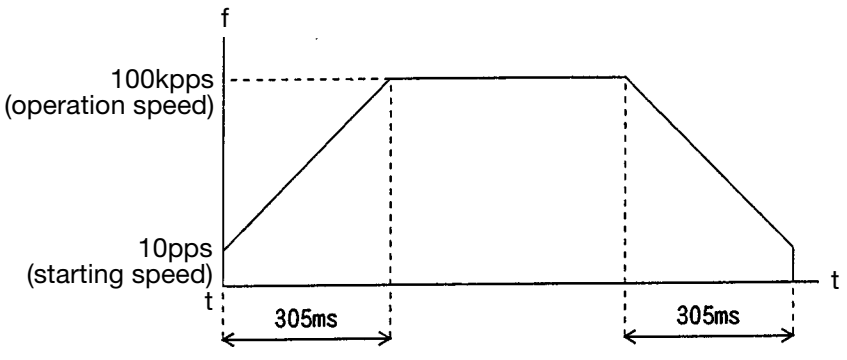
$$\text{Acceleration/deceleration time (s)} = \frac{(RFH - RFL) \times (RUR + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

$$0.3 = \frac{(50000 - 5) \times (RUR + 1) \times 4}{19.6608 \times 10^6}$$

$$RUR = 28.494$$

Since the RUR register can be set only at an integer, write 28 or 29 to the RUR register. Therefore, the practical acceleration/deceleration time is 295ms (with the RUR register set at 28) or 305ms (with the RUR register set at 29).

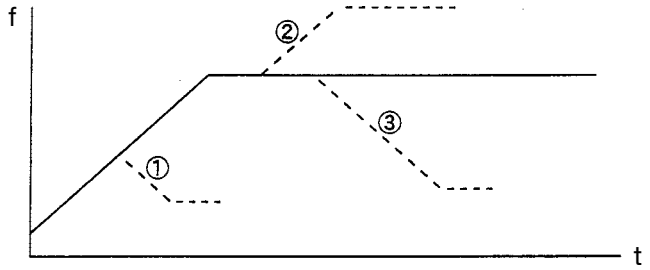
Sample of speed pattern with RUR = 29



10.5 Changing Speed Pattern during Operation in Progress

By writing new values to RFH, RUR, RDR, RUS and RDS registers, you can change speed and acceleration/deceleration patterns even during operation in progress. However, do not change these register values during operation in in-positioning mode with automatic ramping-down point setting (MSDP of RMD register = 0). If changed, the automatic ramping-down point setting function cannot follow the parameters.

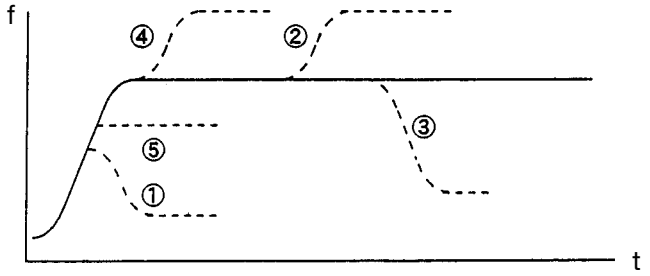
Samples of speed pattern change with linear acceleration/deceleration



① A new RFH value written during acceleration is lower than the preset one and the chip performs deceleration to the new FH rate.

②, ③ A new value is written to the RFH register during operation at the FH rate and the chip accelerates or decelerates to the new rate.

Samples of speed pattern change with S-curve acceleration/deceleration



① A new RFH value written during acceleration is lower than the preset one. If the new FH rate is lower than the rate at the time, the chip performs S-curve deceleration to the new FH rate.

⑤ A new RFH value written during acceleration is lower than the preset one. If the new FH rate is equal to, or higher than the rate at the time, the chip performs acceleration to the new FH rate with no change made to S-curve characteristics.

④ A new RFH value written during acceleration is higher than the preset one. The chip performs acceleration to the preset FH rate with no change made to S-curve characteristics and then re-accelerates to the new FH rate.

②, ③ A new value is written to the RFH register during operation at the FH rate and the chip performs S-curve acceleration or decleration to the new FH rate.

11. Functions

11.1 Reset

After turning the power on, be sure to reset the chip before starting operation. To reset the chip, input more than eight cycles of reference clock during the time the $\overline{RST}$ pin is low level. Reset conditions (initial conditions) are as follows.

Items	Reset (Initial) Condition
Internal registers	0
Control command buffer	0
Axis designation buffer	0
Input/output buffer	0
INT pin	High level
WRQ pin	High level
IFB pin	High level
Pins D0 to D7	High impedance
Pins D8 to D15	High impedance
Pins P0x/y/z/u to P7x/y/z/u	Input pins
CSTA pin	High level
CSTP pin	High level
OUTx/y/z/u pins	High level
DIRx/y/z/u pins	High level
ERCx/y/z/u pins	High level
BSYx/y/z/u pins	High level

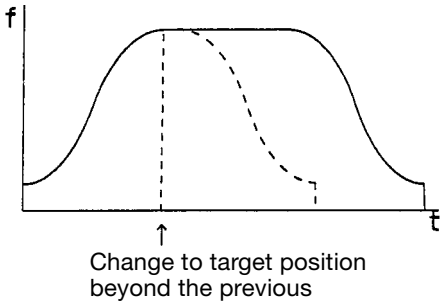
11.2 Overriding Target Position

The PCL6045 allows you to freely override (rewrite) the target position in two ways.

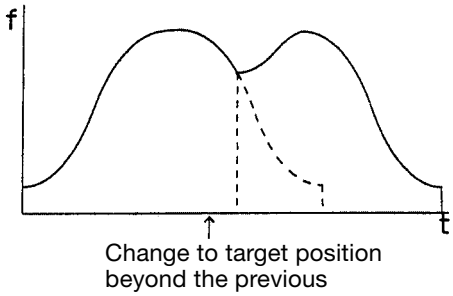
11.2.1 Target Position Override 1

Rewrite a desired target value to the RMV register. The value will override the preset one. The target position is changed referring to the starting position.

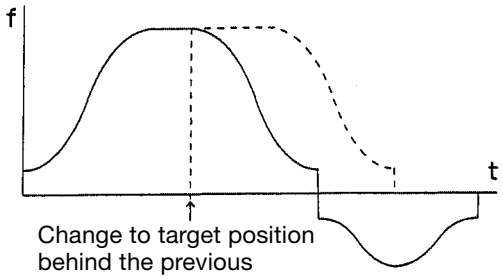
(1) If the value which is rewritten during acceleration or operation at the constant speed is beyond the previous one, the chip keeps the speed pattern to the new target position and then completes in-positioning.



(2) If the value which is rewritten during deceleration is beyond the previous one, the chip accelerates anew from the decelerated position to the FH rate and then completes in-positioning from the new target position (new RMV register value).



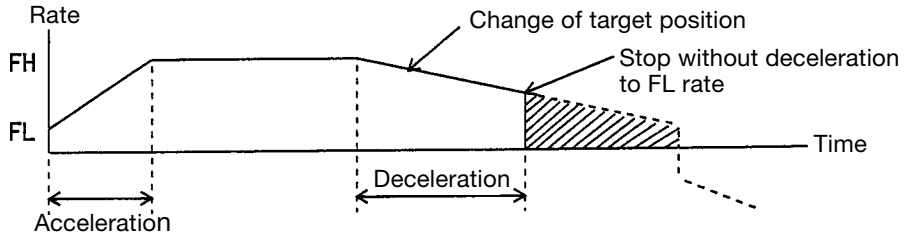
(3) If the value which is rewritten during operation at the constant speed or during deceleration is behind the previous one, the chip stops deceleration and then generates pulses in reverse direction and completes in-positioning from the new target position.



Acceleration and deceleration are available only in varied-speed operation. Also, the target position can be rewritten in any number of times until in-positioning is complete.

Precaution

If the deceleration time is made longer than (acceleration time x 2) in automatic ramping-down point setting, the chip may not perform deceleration to the FL rate (see figure below). In such a case, if the target position which is rewritten during deceleration is behind the initial one, the chip decelerates along the deceleration curve as shown by dotted line in the figure and after stopping at the FL rate, it completes in-positioning at the new target position. Due to this, overrun occurs in an amount from deceleration to stop (area filled with slant lines in the figure).



To avoid overrun, make the deceleration time shorter than (acceleration time x 2). If the deceleration time is over two times the acceleration time in automatic setting, set the ramping-down point in manual mode.

11.2.2 Target Position Override 2 (PCS Signal)

Set the MPCS bit of RMD (operation mode) register at 1 and start the chip generating command pulses. Then, you can perform in-positioning in the moving amount written in the RMV register by writing the command or at the timing the PCS input signal turns on.

The input logic of PCS signal can be changed and the pin status can be checked by reading the extension status (RSTS) register.

To make valid the PCS signal-based target position override, set bit 14 (MPCS) of the RMV register.

[RMD] (WRITE)

15							8
–	n	–	–	–	–	–	–

1: In-positioning will be done in the amount written in the RMV register at the timing the PCS input signal turns on.

To select the input logic of PCS signal, set bit 24 (PCSL) of the RENV1 register.

[RENV1] (WRITE)

31							24
–	–	–	–	–	–	–	n

0: Negative logic
1: Positive logic

To check the PCS signal status, read bit 8 (SPCS) of the MRSTS register.

[RSTS] (READ)

15							8
–	–	–	–	–	–	–	n

0: PCS signal OFF
1: PCS signal ON

[Operation Command]

You can use the operation command STAON in place of the PCS signal to obtain the same effect as the PCS signal turning on. 28HEX

11.3 Output Pulse Control

11.3.1 Output Pulse Modes

The PCL6045 provides four types of common pulse modes and two types of 2-pulse modes.

In the common pulse mode, the chip generates command pulses from the OUT pin and outputs the direction signal from the DIR pin. In the 2-pulse mode, the chip generates plus direction pulses from the OUT pin and minus direction pulses from the DIR pin.

Select a desired command pulse output mode by setting bits 2-0 (PMD) of the RENV1 (environmental setting 2) register. If the motor driver using the common pulse mode takes some time to receive command pulses after the direction judgment signal changes, use the direction change timer. Also, by setting bit 28 (DTMF) of the RENV1 (environmental setting 1) register at 0, you can delay the start of operation by 0.2ms (the time the direction change timer operates) from the time the direction judgment signal changes.

To select a command pulse output mode, set bits 2-0 (PMD2-0) of the RENV1 register as follows.

[RENV1] (WRITE)

7							0
–	–	–	–	–	n	n	n

PMD2-0	Operation in plus direction		Operation in minus direction	
	OUT pin	DIR pin	OUT pin	DIR pin
000		(High)		(Low)
001		(High)		(Low)
010		(Low)		(High)
011		(Low)		(High)
100		(High)	(High)	
111		(Low)	(Low)	

To use the direction change timer, set bit 28 (DTMF) of the RENV1 register.

0: ON

1: OFF

[RENV1] (WRITE)

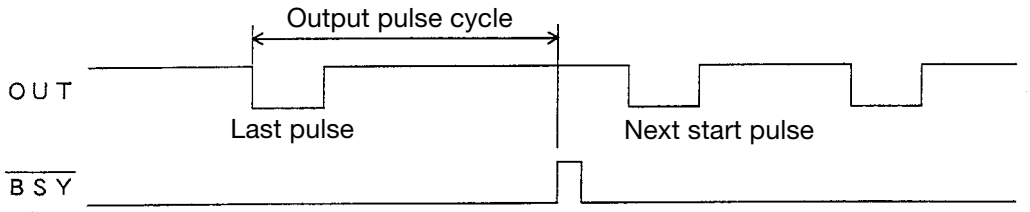
31							24
–	–	–	n	–	–	–	–

11.3.2 Output Pulsewidth Control and Operation-Complete Timing

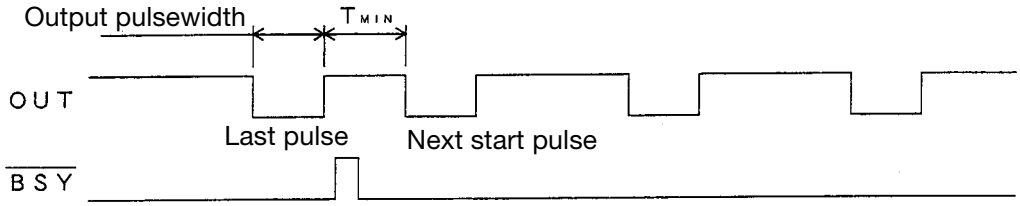
You can expedite the stop timing by controlling the output pulsewidth. When the output pulse rate is lower than 1/8192 (approx. 2.4 kpps with reference clock = 19.6608MHz), the stop timing is 4096 cycles of reference clock (approx. 200µs with reference clock = 19.6608MHz) with the pulsewidth constant. When the output pulse rate is higher than the above, the duty is constant (approx. 50%). By setting bit 13 (PDTC) of the RENV1 (environmental setting 2), you can make the output pulsewidth fixed to duty constant (approx. 50%).

Operation-complete timing can be changed by setting the METM bit of RMD (operation mode) register.

(1) Set the METM bit of RMD register at 0. The chip will complete operation after finishing the last output pulse cycle.



(2) Set the METM bit of RMD register at 1. The chip will complete operation at the time the last pulse turns off.



In this case, a minimum time, TMIN, from the end of last pulse to the start of the first pulse for the next operation is 14 times the reference clock (TMIN = 14 x TCLK).

To select the operation-complete timing, set bit 12 (METM) of the RMD register.

[RMV] (WRITE)

15							8
–	–	–	n	–	–	–	–

0: At the time the last output frequency cycle is complete
1: At the time the last pulse turns off

To select the output pulsewidth, set bit 31 (PDTC) of the RENV1 register.

[RENV1] (WRITE)

31							24
n	–	–	–	–	–	–	–

0: Output pulsewidth constant or duty constant (approx. 50%) is automatically selected according to the rate of pulse output.
1: Output pulsewidth is fixed to duty constant (approx. 50%).

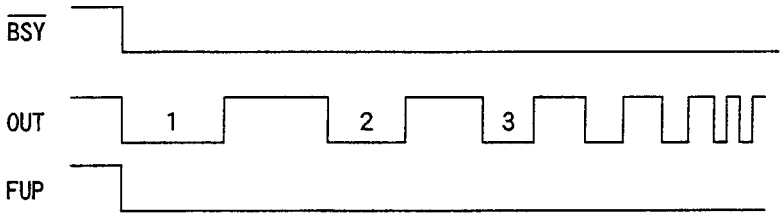
11.4 Idling Control

At the start of varied-speed operation, you can let the chip output idling pulses at the FL rate before starting acceleration. The number of idling pulses can be set by the IDL bit of RENV5 (environmental setting 5) register. When you do not use this function, set the bits at 0 or 1. Then, the chip will start accelerating upon outputting pulses. Accordingly, the rate at the start obtained from the cycle of first two pulses is higher than the FL rate.

To use the idling control function, set the IDL bits at 2 to 7. The chip will start acceleration upon outputting idling pulses in that number. Accordingly, the rate at the start is FL rate, thereby allowing you to set the FL rate at a value near the upper limit of self-starting frequency. If used in in-positioning mode, the function does not affect the total moving amount.

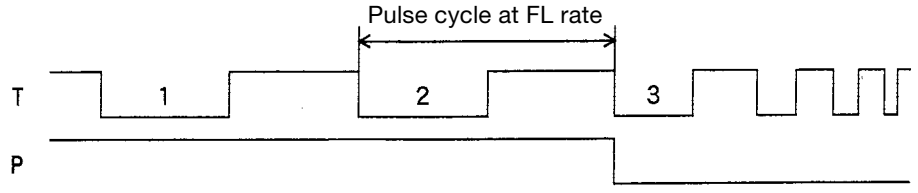
Number of idling pulses and acceleration start timing

Number of idling pulses = 0 or 1



▲ Acceleration starts before outputting the first pulse.

Number of idling pulses = 3



Acceleration starts from the third pulse ▲

To select the number of idling pulses, set bits 10-8 (IDL2-0) of the RENV5 register in a range of 0 to 7. Acceleration will start after outputting idling pulses in that number.

[RENV5] (WRITE)

15							8
–	–	–	–	–	n	n	n

To check the value of idling control counter, read bits 22-20 (IDC2-0) of the RSPD register.

[RSPD] (READ)

23							16
0	n	n	n	–	–	–	–

11.5 External Input Signals from Mechanical System

11.5.1 +EL and – EL Signals

When the end limit signal in the moving direction turns on during operation, the chip stops immediately or stops after deceleration. If the EL signal turns off thereafter, the chip keeps stopping. Also, if the start command is written with the EL signal ON, the chip cannot start in the same direction as the EL signal.

By setting the ELM bit of RENV1 (environmental setting 1) register, you can select an EL signal-initiated action, immediate stop or stop after deceleration (available only for varied-speed operation). Though the minimum pulsewidth of EL signal is 80 cycles of the reference clock (4μs) with the input filter set to ON, it can be made 2 cycles of the reference clock (0.1μs) by setting the input filter to OFF.

The EL signal can be checked by reading the sub status (SSTSW) and the interrupt EL signal, plus or minus, can be checked by reading the REST register. Though the EL signal is ignored in timer mode, it can be checked by reading the sub status (SSTSW).

The input logic of EL signals can be set by the ELL pin for each individual axis.

To select the input logic of ±EL signals, set the ELL pin.
Low level: Positive logic
High level: Negative logic

To select ±EL signal-initiated action, set bit 3 (ELM) of the RENV1 register.
0: Immediate stop
1: Stop after deceleration

[RENV1] (WRITE)

7	6	5	4	3	2	1	0
–	–	–	–	n	–	–	–

To check the ±EL signal status, read bits 12 (SPEL) and 13 (SMEL) of the SSTW.
SPEL = 0: +EL signal OFF SPEL = 1: +EL signal ON
SMEL = 0: –EL signal OFF SMEL = 1: –EL signal ON

[SSTSW] (READ)

7	6	5	4	3	2	1	0
–	–	n	n	–	–	–	–

To check the interrupt EL signal, read bits 5 (ESPL) and 6 (ESML) of the REST register.
ESPL = 1: Stop by +EL signal ON
ESML = 1: Stop by –EL signal ON

[REST] (READ)

7	6	5	4	3	2	1	0
–	n	n	–	–	–	–	–

To insert the ±EL input filter, set bit 26 (FLTR) of the RENV1 register at 1. Signals of pulsewidth shorter than 4μs will be ignored.

[RENV1] (WRITE)

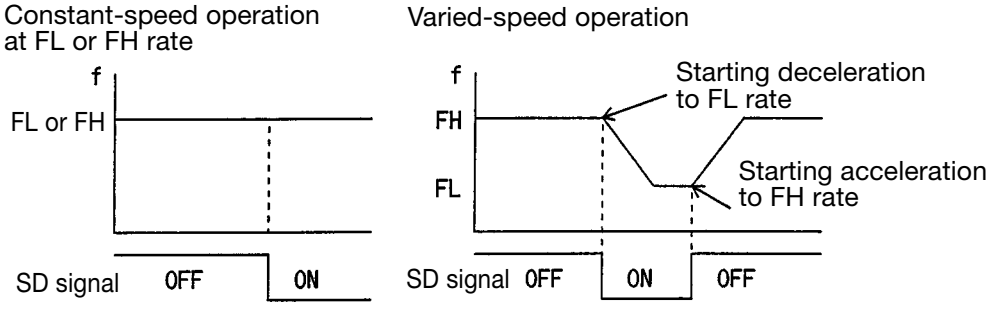
27	26	25	24	23	22	21	20
–	n	–	–	–	–	–	–

Note that EL signal-initiated operation may differ from the above in the origin return (9.5.1), origin search (9.5.3) and EL or SL operation mode (9.6). Refer to these sections for details.

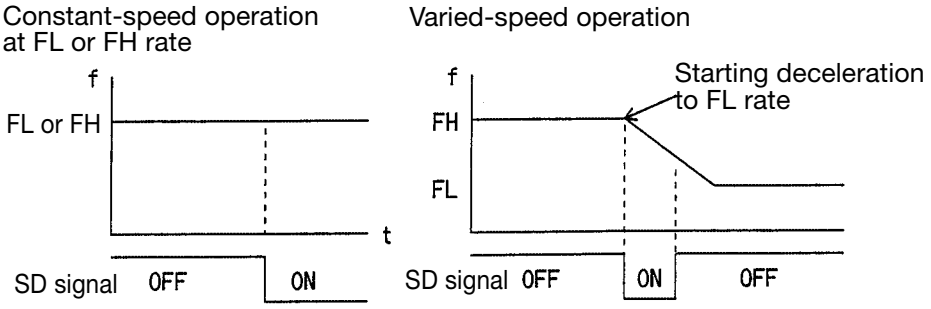
11.5.2 SD Signal

The SD signal is ignored if the SD signal input is made invalid by setting the MSDE bit of the RMD (operation mode) register. With the SD signal input made valid, if the SD signal turns on during operation, the chip performs (1) deceleration, (2) latch and deceleration, (3) stop after deceleration or (4) latch and stop after deceleration, according to setting of SDM and SDLT bits of the RENV1 (environmental setting 1) register.

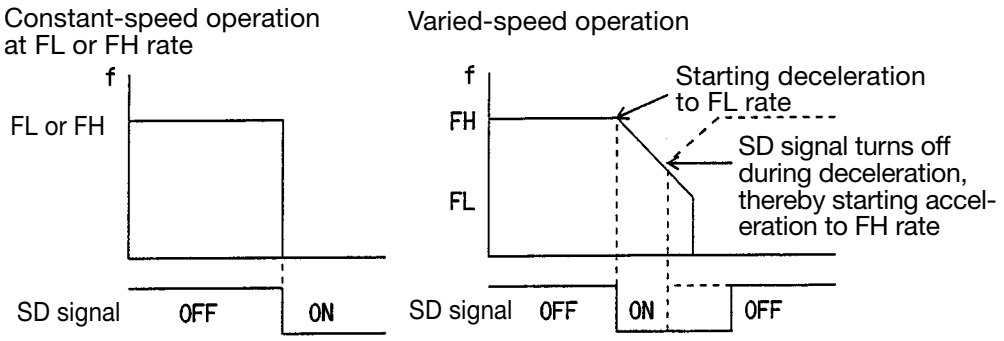
(1) Deceleration [bit 4 (SDM) = 0, bit 5 (SDLT) = 0]
In constant-speed operation, any SD signal is ignored. In varied-speed operation, the SD signal which turns on lets the chip decelerate to the FL rate. If the SD signal turns off during deceleration, the chip accelerates to the FH rate.
If the SD signal is on at the time the start command for varied-speed operation is written, the chip generates pulses at the FL rate and when the SD signal turns off, it accelerates to the FH rate.



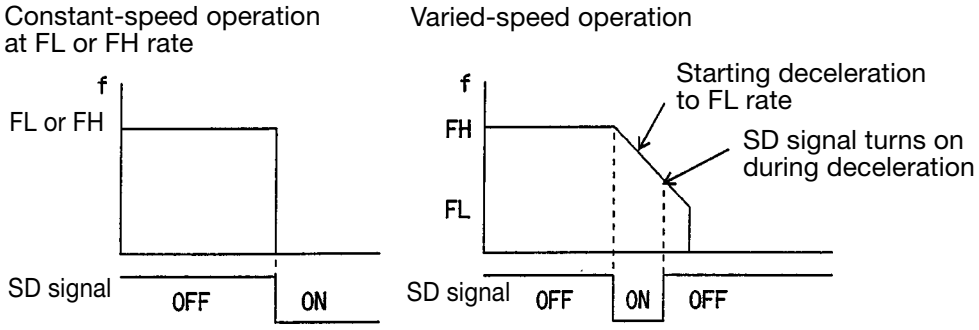
(2) Latch and Deceleration [bit 4 (SDM) = 0, bit 5 (SDLT) = 1]
In constant-speed operation, any SD signal is ignored. In varied-speed operation, the SD signal which turns on lets the chip decelerate to the FL rate. If the SD signal turns off after or during deceleration, the chip keeps the FL rate and does not accelerate to the FH rate.
If the SD signal is on at the time the start command for varied-speed operation is written, the chip generates pulses at the FL rate but does not accelerate to the FH rate if the SD signal turns off.



(3) Stop after Deceleration [bit 4 (SDM) = 1, bit 5 (SDLT) = 0]
In constant-speed operation, the SD signal which turns on stops the chip from generating pulses. In varied-speed operation, the SD signal which turns on lets the chip stop after decelerating to the FL rate. If the SD signal turns off during deceleration, the chip does not start but completes operation. When the SD signal stops the chip, the $\overline{INT}$ signal is output.



(4) Latch and Stop after Deceleration [bit 4 (SDM) = 1, bit 5 (SDLT) = 1]
In constant-speed operation, the SD signal which turns on stops the chip from generating pulses. In varied-speed operation, the SD signal which turns on lets the chip stop after decelerating to the FL rate. If the SD signal turns off during deceleration, the chip does not accelerate to the FH rate.
If the SD signal is on at the time the start command is written, the chip does not start but completes operation. When the SD signal stops the chip, the $\overline{INT}$ signal is output.



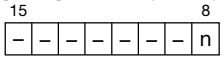
The input logic of SD signal can be changed. The latched condition is reset if the SD signal is off at the next start. Also, it is reset by setting the SDLT bit at 0.

Though the minimum pulsewidth of SD signal is 80 cycles of the reference clock (4.0µs with reference clock = 19.6608MHz) with the input filter set to ON, it is made two cycles of the reference clock (0.1µs) by setting the input filter to OFF.

The SD latch signal can be checked by reading the sub status (SSTSW), and the SD pin status can be checked by reading the extension status (RSTS) register. The REST register allows you to check whether the interrupt factor is SD signal or not.

To make the SD signal input valid or invalid, set bit 8 (MSDE) of the RMD register.

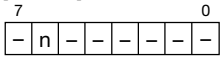
[RMD] (WRITE)



0: Invalid
1: Valid

To select the input logic of SD signal, set bit 6 (SDL) of the RENV1 register.

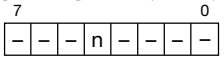
[RENV1] (WRITE)



0: Negative logic
1: Positive logic

To select an action initiated by the SD signal, set bit 4 (SDM) of the RENV1 register.

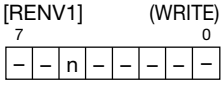
[RENV1] (WRITE)



0: Constant-speed operation at FL rate after deceleration
1: Stop after deceleration

To select the SD signal input mode, set bit 5 (SDLT) of the RENV1 register.

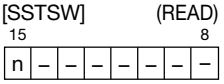
[RENV1] (WRITE)



0: Level input
1: Latch input (latch is reset when the SD input is off at the next start or by setting to level input.)

To check the SD latch signal, read bit 15 (SSD) of SSTSW.

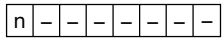
[SSTSW] (READ)



0: SD latch signal OFF
1: SD latch signal ON

To check the SD signal, read bit 15 (SDIN) of RSTS.

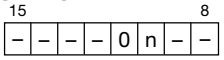
[RSTS] (READ)



0: SD signal OFF
1: SD signal ON

To check the interrupt factor, read bit 10 (ESSD) of the REST register.

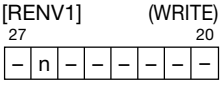
[REST] (READ)



1: Stop after deceleration due to the SD signal which turns on.

To insert the SD input filter, set bit 26 (FLTR) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidth shorter than 4μs are disregarded.

[RENV1] (WRITE)



11.5.3 ORG and EZ Signals

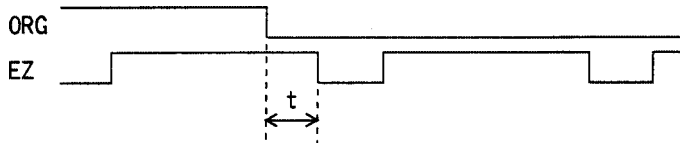
These signals are effective in origin-related modes (origin return, origin escape and origin search) and EZ count-based termination mode. The operation mode and moving direction are set by the RMD (operation mode) register.

Since the ORG signal input is internally latched, you need not keep it on externally. The ORG latch signal is reset at the time of stop. Though the minimum pulsewidth of ORG signal is 80 cycles of the reference clock (4μs) the input filter set to ON, it can be made two cycles of the reference clock (0.1μs) by setting the input filter to OFF.

The input logic of ORG and EZ signals can be changed by setting the RENV1 (environmental setting 1) register. The ORG pin status can be checked by reading the sub status (SSTSW) and the EZ pin status can be checked by reading the extension status (RSTS) register.

For origin-related modes, refer to "9.5 Origin-related Modes."

Timing relation between ORG and EZ signals



- The EZ signal is counted if $t \geq 2 \times T_{CLK}$.
- The EZ signal may be counted or not if $T_{CLK} < t < 2 \times T_{CLK}$.
- The EZ signal is not counted if $t \leq T_{CLK}$.

  T_{CLK}: Reference clock cycle

To make ORG signal input and EZ count-based operation valid, set bits 6-0 (MOD) of the RMD register.

[RMD] (WRITE)

7							0
0	n	n	n	n	n	n	n

001 0000: Origin return in plus direction
001 1000: Origin return in minus direction
001 0010: Origin escape in plus direction
001 1010: Origin escape in minus direction
001 0101: Origin search in plus direction
001 1101: Origin search in minus direction
010 0100: Pulse output in plus direction based on EZ count
010 1100: Pulse output in minus direction based on EZ count

To select the origin return method, set bits 3-0 (ORM3-0) of the RENV3 register. Refer to the section of RENV3 register for details.

[RENV3] (WRITE)

7							0
–	–	–	–	n	n	n	n

To select the input logic of ORG signal, set bit 7 (ORGL) of the RENV1 register.

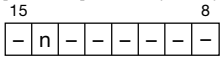
[RENV1] (WRITE)

7							0
n	–	–	–	–	–	–	–

0: Negative logic
1: Positive logic

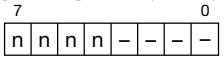
To check the ORG pin status, read bit 14 (SORG) of SSTSW.
0: ORG signal OFF
1: ORG signal ON

[SSTSW] (READ)



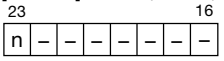
To enter the EZ counter value, set bit 7-4 (EZD3-0) of the RENV3 register. Set a number of (counting value – 1) in a range of 0 to 15. The chip will output pulses in that number before completing an origin return.

[RENV3] (WRITE)



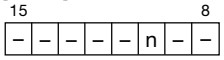
To select the input logic of EZ signal, set bit 23 (EZL) of the RENV2 register.
0: Falling edge
1: Rising edge

[RENV2] (WRITE)



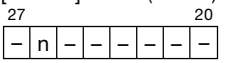
To check the EZ pin status, read bit 10 (SEZ) of the RSTS register.
0: EZ signal OFF
1: EZ signal ON

[RSTS] (READ)



To insert the EZ input filter, set bit 26 (FLTR) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidth shorter than 4μs are disregarded.

[RENV1] (WRITE)



11.6 Servomotor Interface

11.6.1 INP Signal

The pulse-train input type servo driver has the built-in deviation counter which counts deviation between input command pulses and input feedback pulses. The servo driver controls the motor so that the deviation becomes 0. That is, the servomotor operates with some delay from command pulses and continues operating until the driver's deviation counter counts down to 0 if the control chip stops generating command pulses.

The PCL6045 can be set so that it judges completion of operation not at the time it completes outputting pulses but at the time it receives the in-position (INP) signal from the servo driver. If judgment of completion of operation is based on the INP signal input, the $\overline{\text{BSY}}$ signal, main status (bits 5 to 0 of MSTSW, stop condition) and extension status (CND3 to 0, operation status) are based on the INP signal.

The input logic of INP signal can be changed. Though the minimum pulsewidth of INP signal is 80 cycles of the reference clock (4μs with reference clock = 19.6608MHz) with the input filter set to ON, it can be made two cycles of the reference clock (0.1μs) by setting the input filter to OFF. The INP pin status can be checked by reading the RSTS (extension status) register.

To make INP signal-based completion of operation valid or invalid, set bit 9 (MINP) of the RMD register.

[RMD] (WRITE)

15							8
–	–	–	–	–	–	n	–

0: INP signal does not cause any delay in completion of operation.
1: INP signal delays completion of operation (status, $\overline{\text{BSY}}$).

To select the input logic of INP signal, set bit 22 (INPL) of the RENV1 register.

[RENV1] (WRITE)

23							16
–	n	–	–	–	–	–	–

0: Negative logic
1: Positive logic

To check the INP signal status, read bit 16 (SINP) of the RSTS register.

[RSTS] (READ)

23							16
0	0	0	0	0	0	0	n

0: INP signal OFF
1: INP signal ON

To insert the INP input filter, set bit 26 (FLTR) of the RENV1 register at 1. If the filter is inserted, signals of pulsewidth shorter than 4μs are ignored.

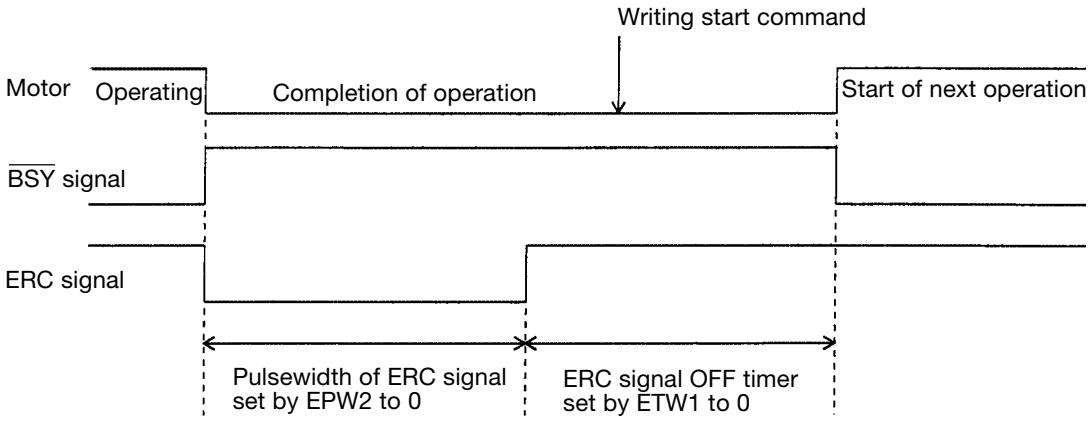
[RENV1] (WRITE)

27							20
–	n	–	–	–	–	–	–

11.6.2 ERC Signal

If the chip completes outputting command pulses, the servomotor operates until the servo driver's deviation counter counts down to 0. To immediately stop the servomotor without delay, the servo driver's deviation counter should be cleared.

The PCL6045 can output the ERC signal to clear the servo driver's deviation counter. The ERC signal is output as one-shot signal or level signal, which can be selected by the RENV1 (environmental setting 1) register. If the servo driver requires time for accepting command pulses after the ERC signal becomes high level (OFF), the time of the ERC signal OFF timer can be selected by setting the RENV1 register.



To output the ERC signal at the time of completing the origin return, set bit 11 (EROR) of the RENV1 (environmental setting 1) register at 1 (automatic ERC signal output). For ERC signal output timing, refer to the timing waveform of "9.5.1 Origin Return." To output the ERC signal when the EL, ALM or CEMG signal or the emergency stop command (05HEX) causes immediate stop, set bit 10 (EROE) of the RENV1 register at 1 (automatic ERC signal output). Note that if stop-after-deceleration is selected, the ERC signal is not output irrespective of EROE bit setting.

Also, the ERC signal can be output by writing the ERC output command (24HEX). The output logic of the ERC signal can be changed by setting RENV1 register and the ERC input status can be checked by reading the extension status (RSTS) register.

To automatically output ERC signal when EL, ALM or CEMG signal stops the chip, set bit 10 (EROE) of the RENV1 register.

[RENV1] (WRITE)

15							8
–	–	–	–	–	n	–	–

0: No ERC output
1: ERC output

To automatically output ERC signal upon completing the origin return, set bit 11 (EROR) of the RENV1 register.

0: No ERC signal output
1: ERC signal output

[RENV1] (WRITE)

15							8
–	–	–	–	n	–	–	–

To select the ERC signal output width, set bits 14-12 (EPW2-0) of the RENV1 register.

000: 12µs 101: 102µs 010: 408µs
011: 1.6ms 100: 13ms 101: 52ms
110: 104ms 111: Level output

[RENV1] (WRITE)

15							8
–	n	n	n	–	–	–	–

To select the output logic of ERC signal, set bit 15 (ERCL) of the RENV1 register.

0: Negative logic
1: Positive logic

[RENV1] (WRITE)

15							8
n	–	–	–	–	–	–	–

To select the time of ERC signal OFF timer, set bits 17-16 (ETW1-0) of the RENV1 register.

00: 0µs 01: 12µs
10: 1.6ms 11: 104ms

[RENV1] (WRITE)

23							16
–	–	–	–	–	–	n	n

To check the ERC signal status, read bit 9 (SERCR) of the RSTS register.

0: ERC signal OFF
1: ERC signal ON

[RSTS] (READ)

15							8
0	–	–	–	–	–	n	–

The emergency stop command (05HEX, CMEMG: bit control command) lets the chip output the ERC signal.

[Bit Control Command]

05HEX

The ERC output command (24HEX, ERCOUT: bit control command) turns the ERC signal on.

[Bit Control Command]

24HEX

The ERC signal output reset command (25HEX, ERCRST: bit control command) turns the ERC signal off.

[Bit Control Command]

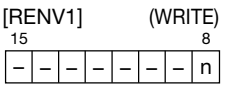
25HEX

11.6.3 ALM Signal

The chip can input the alarm (ALM) signal. If the ALM signal turns on during operation, the chip immediately stops generating pulses or stops after deceleration in the case of varied-speed operation. If the start command is written with the ALM signal ON, the chip does not generate any command pulse.

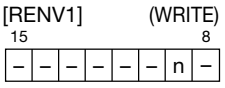
Though the minimum pulsewidth of ALM signal is 80 cycles of the reference clock (4μs with reference clock = 19.6608MHz) with the input filter set to ON, it is made two cycles of the reference clock (0.1μs) by setting the input filter to OFF. The input logic of ALM signal can be changed and the signal status can be checked by reading the sub status (SSTSW).

To select whether the ALM signal stops the chip immediately or after deceleration, set bit 8 (ALMM) of the RENV1 register.



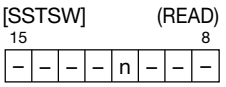
0: Immediate stop
1: Stop after deceleration (available only for varied-speed operation)

To select the input logic of ALM signal, set bit 9 (ALML) of the RENV1 register.



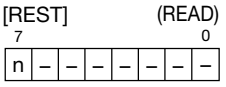
0: Negative logic
1: Positive logic

To check the ALM signal status, read bit 11 (SALM) of SSTSW.



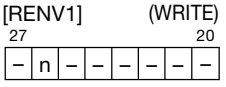
0: ALM signal OFF
1: ALM signal ON

To check whether the ALM signal is the interrupt factor or not, read bit 7 (ESAL) of the REST register.



1: ALM signal is the interrupt factor.

To insert the ALM input filter, set bit 26 (FLTR) of the RENV1 filter at 1. If the filter is inserted, signals of pulsewidth shorter than 4μs are ignored.



11.7 External Start/Simultaneous Start

11.7.1 $\overline{\text{CSTA}}$ Signal

Use of the $\overline{\text{CSTA}}$ pin enables the external signal to start the chips. Set bits 19-18 (MSY) of the RMD (operation mode) register at 01 in advance. Then, the chip will start at the timing when the $\overline{\text{CSTA}}$ pin becomes low level. For control of more than four axes, connect multiple chips via the $\overline{\text{CSTA}}$ pin, and the axes ready for $\overline{\text{CSTA}}$ input can be simultaneously started. In this case, the $\overline{\text{CSTA}}$ pin can output the start signal. The input logic of $\overline{\text{CSTA}}$ signal cannot be changed.

By setting the RIST (event interrupt factor) register, the INT signal can be output at the simultaneous start ($\overline{\text{CSTA}}$ input ON). By reading the RIST register, you can check the event interrupt factor. Also, by reading the extension status (RSTS) register, you can check the operation status (ready for $\overline{\text{CSTA}}$ input) and $\overline{\text{CSTA}}$ pin status.

Method for Simultaneous Start

Set bits 19-18 (MSY1-0) of the RMD register of concerned axes at 01. Write the start command to make the chips ready for $\overline{\text{CSTA}}$ input. Then, start the chips simultaneously in one of the following two ways.

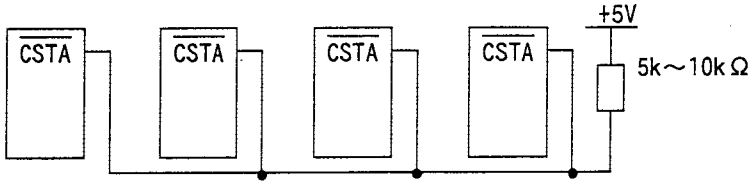
(1) Write the simultaneous start command. The $\overline{\text{CSTA}}$ pin will output a one-shot signal of the pulsewidth of eight cycles of reference clock (approx. 0.4μs with reference clock = 19.6608MHz)

(2) Input a hard signal from an external device. Input the hard signal after driving it with an open collector output (74LS06 or the like).

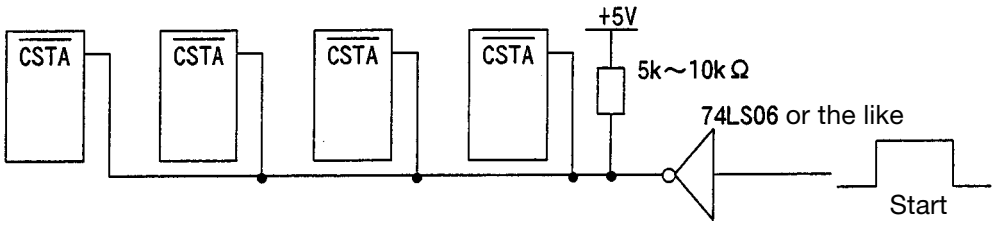
Also the $\overline{\text{CSTA}}$ signal input method, either level trigger input or edge trigger input can be selected. Note, however, that if the level trigger input is selected, writing the simultaneous start command with the $\overline{\text{CSTA}}$ pin at low level starts the chips immediately. Also, if the chips are connected via the $\overline{\text{CSTA}}$ pin, each axis can be started independently by writing the start command.

To cancel the $\overline{\text{CSTA}}$ input ready condition, write the immediate stop command (49HEX).

• Connection for simultaneous start of multiple chips



• Connection for simultaneous start of multiple chips by external signal



The external start signal should be one-shot signal of which the pulsewidth is four cycles of the reference clock (approx. 0.2µs with reference clock = 19.6608MHz).

To make it ready for the $\overline{\text{CSTA}}$ signal input, set bits 19-18 (MSY1-0) of the RMD register.

01: The $\overline{\text{CSTA}}$ signal input starts the chips operating.

[RMD] (WRITE)

23							16
–	–	–	–	n	n	–	–

To select the $\overline{\text{CSTA}}$ signal input type, set bit 18 (STAM) of the RENV1 register.

0: Level trigger input

1: Edge trigger input

[RENV1] (WRITE)

23							16
–	–	–	–	–	n	–	–

To check the CSTA signal status, read bit 5 (SSTA) of the RSTS register.

0: $\overline{\text{CSTA}}$ signal OFF

1: $\overline{\text{CSTA}}$ signal ON

[RSTS] (READ)

7							0
–	–	n	–	–	–	–	–

To check the operation status, read bits 3-0 (CND) of the RSTS register.

0010: Waiting for $\overline{\text{CSTA}}$ input

[RSTS] (READ)

7							0
–	–	–	–	n	n	n	n

To make the $\overline{\text{CSTA}}$ signal an event interrupt factor, set bit 18 (IRSA) of the RIRQ register.

1: $\overline{\text{CSTA}}$ signal which turns on lets the chip output the $\overline{\text{INT}}$ signal.

[RIRQ] (WRITE)

23							16
–	–	–	–	n	n	n	n

To check the event interrupt factor, read bit 19 (ISSA) of the RIST register.

1: Event interrupt factor is the $\overline{\text{CSTA}}$ signal which turns on.

[RIST] (READ)

23							16
0	0	0	0	n	–	–	–

The simultaneous start command (06HEX, CMSTA: operation command) lets each $\overline{\text{CSTA}}$ pin output one shot pulse of the width of eight cycles of reference clock.

[Operation Command]

06HEX

The start command (2AHEX, SPSTA: operaton command) to the $\overline{\text{CSTA}}$ pin lets only the axis operate.

[Operation Command]

2AHEX

11.7.2 PCS Signal

Essentially, the PCS pin is intended for use in target position override 2. But it can be made a pin to input the $\overline{\text{CSTA}}$ signal effective only for the axis by setting bit 30 (PCSM) of the RENV1 (environmental setting 1) register at 1 and bits 19-18 (MSY) of the RMD (operation mode) register at 01.

The input logic of PCS signal can be changed and the pin status can be checked by reading the extension status (RSTS) register.

To select the function of PCS signal, set bit 30 (PCSM) of the RENV1 register.

[RENV1] (WRITE)

31							24
–	n	–	–	–	–	–	–

1: PCS signal is made the $\overline{\text{CSTA}}$ signal effective only for the axis.

To make the chip ready for $\overline{\text{CSTA}}$ input, set bits 19-18 (MSY1-0) of the RMD register.

[RMD] (WRITE)

23							16
–	–	–	–	n	n	–	–

01: $\overline{\text{CSTA}}$ signal which turns on starts the axis.

To select the input logic of PCS signal, set bit 24 (PCSL) of the RENV1 register.

[RENV1] (WRITE)

31							24
–	–	–	–	–	–	–	n

0: Negative logic
1: Positive logic

To check the PCS signal status, read bit 8 (SPCS) of the RSTS register.

[RSTS] (READ)

15							8
–	–	–	–	–	–	–	n

0: PCS signal OFF
1: PCS signal ON

11.8 External Stop/Simultaneous Stop

Use of the $\overline{\text{CSTP}}$ pin enables the external signal to stop the chips. Set bit 24 (MSPE) of the RMD (operation mode) register at 1. Then, the chip will stop immediately or after deceleration at the timing when the $\overline{\text{CSTP}}$ pin becomes low level. Note that stop after deceleration is available only in varied-speed operation. In constant-speed operation, only immediate stop is available. The input logic of $\overline{\text{CSTP}}$ signal cannot be changed.

For control of more than four axes, connect multiple chips via the $\overline{\text{CSTP}}$ pin, and the axes ready for $\overline{\text{CSTP}}$ input can be simultaneously stopped. In this case, the $\overline{\text{CSTP}}$ pin can output the stop signal.

The $\overline{\text{INT}}$ signal can be output when the $\overline{\text{CSTP}}$ signal, which turns on, stops the operation. By reading the REST register, you can check the error interrupt factor. Also, by reading the extension status (RSTS) register, you can check the $\overline{\text{CSTP}}$ pin status.

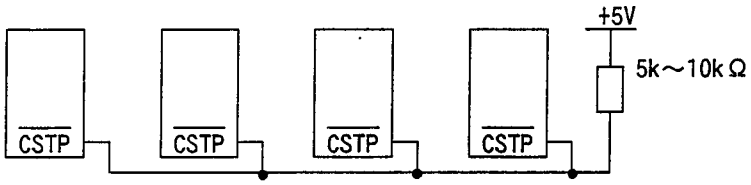
Method for Simultaneous Stop

Set bit 24 (MSPE) of the RMD register of concerned axes at 1 and start. After then, you can simultaneously stop in any of the following two ways.

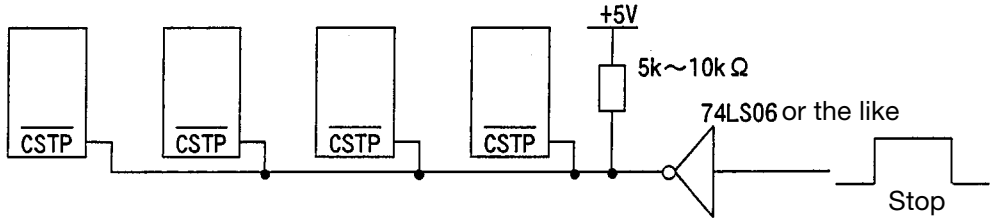
(1) Write the simultaneous stop command. Each $\overline{\text{CSTP}}$ pin will output one-shot signal of pulsewidth of eight cycles of reference clock (approx. 0.4µs with reference clock = 19.6608MHz).
(2) Input a hard signal from external circuit. Input the hard signal after driving with open collector output (74LS06 or the like).

If chips are connected via the $\overline{\text{CSTP}}$ pin, each axis can be stopped independently by writing the stop command.

• Connection for simultaneous stop of multiple axes



• Connection for simultaneous stop of multiple axes by external signal



The input signal should be one-shot signal of which the pulsewidth is longer than four cycles of reference clock (approx. 0.2µs with reference clock = 19.6608MHz).

To make the $\overline{\text{CSTP}}$ input valid or invalid, set bit 24 (MSPE) of the RMD regiser.

1: $\overline{\text{CSTP}}$ input causes immediate stop or stop after deceleration.

[RMD] (WRITE)

31							24
0	0	0	0	0	–	–	n

To select the way of stop due to the $\overline{\text{CSTP}}$ signal, set bit 19 (STPM) of the RENV1 register.

0: Immediate stop
1: Stop after deceleration

[RENV1] (WRITE)

23							16
–	–	–	–	n	–	–	–

To check the $\overline{\text{CSTP}}$ signal status, read bit 6 (SSTP) of the RSTS register.

0: $\overline{\text{CSTP}}$ signal OFF
1: $\overline{\text{CSTP}}$ signal ON

[RSTS] (READ)

7							0
–	n	–	–	–	–	–	–

To check the error interrupt factor, read bit 8 (ESSP) of the REST register.

1: $\overline{\text{CSTP}}$ signal which turns on stops the operation.

[REST] (READ)

16							8
–	–	–	–	–	–	–	n

To simultaneously stop, write the simultaneous stop command (07HEX, CMSTP: operation command). The CSTP pin will output one-shot pulse of the width of eight cycles of reference clock.

11.9 Emergency Stop

For emergency stop, the PCL6045 provides the $\overline{\text{CEMG}}$ input pin. If the $\overline{\text{CEMG}}$ signal becomes low level or if the emergency stop command is written during operation, all axes stop immediately. With the $\overline{\text{CEMG}}$ signal at low level, any axis cannot operate. The input logic of $\overline{\text{CEMG}}$ signal cannot be changed.

The $\overline{\text{INT}}$ signal is output when the $\overline{\text{CEMG}}$ signal turns on, causing an immediate stop and by reading the REST register, the error interrupt factor can be checked. Also, the $\overline{\text{CEMG}}$ pin status can be checked by reading the RSTS (extension status) register.

To check the $\overline{\text{CEMG}}$ signal status, read bit 7 (SEMG) of the RSTS register.

0: $\overline{\text{CEMG}}$ signal OFF
1: $\overline{\text{CEMG}}$ signal ON

[RSTS] (READ)

7							0
n	–	–	–	–	–	–	–

To check the error interrupt factor, read bit 9 (ESEM) of the REST register.

1: $\overline{\text{CEMG}}$ signal which turns on causes emergency stop.

[REST] (READ)

16							8
–	–	–	–	–	–	n	–

The emergency stop command (05HEX, CMEMG: operation command) provides the same effect as the $\overline{\text{CEMG}}$ signal which turns on.

[Operation Command]

05HEX

11.10 Counters

11.10.1 Types of Counters and Their Input Methods

Besides the in-position counter, the PCL6045 provides four internal counters for each axis to permit:

- Controlling command and mechanical positions
- Out-of-step detection using the counter 3 (deviation) and comparator
- Synchronzation signal output using counter 4 (multi-purpose) and comparator

The in-position counter has the absolute value of the RMV (target position) register loaded at the start in any operation mode and counts down at every pulse output. However, during execution of the target position override 2 with bit 14 (MPCS) of the RMD register (operation mode) set at 1, it does not count down until the PCS signal turns on.

While the input of counter 1 is limited to output pulses, the input of counters 2 to 4 can be selected as shown on the table below by setting the RENV3 (environmental setting 3).

	Counter 1	Counter 2	Counter 3	Counter 4
Name	Command position	Mecha. position	Deviation	Multi-purpose
Type	Up/down counter	Up/down counter	Deviation counter	Up/down counter
Bit length	28	28	16	28
Output pulse	Yes	Yes	Yes	Yes
Encoder (EA/EB) input		Yes	Yes	Yes
Pulser (PA/PB) input		Yes	Yes	Yes
Reference clock x 1/2				Yes

To select the input of counter 2 (mechanical), set bits 9-8 (CI21-20) of RENV3 register.

[RENV3] (WRITE)

15							8
–	–	–	–	–	–	n	n

00: EA/EB input
01: Output pulse
10: PA/PB input

To select the input of counter 3 (deviation), set bits 11-10 (CI31-30) of REVN3 register.

[RENV3] (WRITE)

15							8
–	–	–	–	n	n	–	–

00: Deviation between output pulse and EA/EB input
01: Deviation between output pulse and PA/PB input
10: Deviation between EA/EB input and PA/PB input

To select the input of counter 4 (multi-purpose), set bits 13-12 (CI41-40) of REN3 register.

[RENV3] (WRITE)

15							8
–	–	n	n	–	–	–	–

00: Output pulse
01: EA/EB input
10: PA/PB input
11: One-half the reference clock

For the EA/EB and PA/PB input pins selected as counter input, you can select the type of input signal from the following two by setting the RENV2 (environmental setting 2) register:

(1) Input signal: 90° phase difference signal (1, 2 or 4 times multiplied)
Counting direction: Counting up when the phase of EA signal advances and counting down when the phase of EB signal advances

(2) Input signal: Plus and minus pulses
Counting direction: Counting up at the rise of EA signal and counting down at the rise of EB signal

The counting direction of EA/EB and PA/PB signals can be reversed if desired.

If EA input and EB input or PA input and PB input change simultaneously, an error results. You can check the fact by reading the REST (error interrupt factor) register.

To select the EA/EB input, set bits 21-20 (EIM1-0) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	–	n	n	0	0	–	–

00: 90° phase difference signal, 1 time multiplied
01: 90° phase difference signal, 2 times multiplied
10: 90° phase difference signal, 4-times multiplied
11: Plus and minus pulses

To select the counting direction of EA/EB input, set bit 22 (EDIR) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	n	–	–	0	0	–	–

0: Counting up when the phase of EA signal advances or at the rise of EA
1: Counting up when the phase of EB signal advances or at the rise of EB

To select the PA/PB input, set bits 25-24 (PIM1-0) of the RENV2 register.

[RENV2] (WRITE)

31							24
0	0	0	0	0	–	n	n

00: 90° phase difference signal, 1 time multiplied
01: 90° phase difference signal, 2 times multiplied
10: 90° phase difference signal, 4-times multiplied
11: Plus and minus pulses

To select the counting direction of PA/PB input, set bit 26 (PDIR) of the RENV2 register.

[RENV2] (WRITE)

31							24
0	0	0	0	0	n	–	–

0: Counting up when the phase of PA signal advances or at the rise of PA
1: Counting up when the phase of PB signal advances or at the rise of PB

To check EA/EB or PA/PB input error, read bits 16 (ESEE) and 17 (ESPE) of the REST register.

[REST] (READ)

23							16
0	0	0	0	0	0	n	n

Bit 16 (ESEE) = 1: EA/EB input error
Bit 17 (ESPE) = 1: PA/PB input error

11.10.2 Resetting Counters

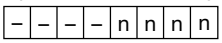
Each counter is reset by any of the following three ways.

(1) Turning the CLR signal from OFF to ON (by setting RENV3 register)
(2) Completing the origin return (by setting RENV3 register)
(3) Writing the command.

Also, as an event interrupt factor, the $\overline{\text{INT}}$ signal can be output at the time the CLR signal is input.

To turn the CLR signal from OFF to ON, set bits 19-16 (CU4C-1C) of the RENV3 register.

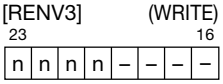
[RENV3] (WRITE)



Bit 16 (CU1C) = 1: Resets counter 1 (command position).
Bit 17 (CU2C) = 1: Resets counter 2 (mechanical position).
Bit 18 (CU3C) = 1: Resets counter 3 (deviation).
Bit 19 (CU4C) = 1: Resets counter 4 (multi-purpose).

To reset counters upon completing the origin return, set bits 23-20 (CU4R-1R) of the RENV3 register.

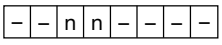
[RENV3] (WRITE)



Bit 20 (CU1R) = 1: Resets counter 1 (command position).
Bit 21 (CU2R) = 1: Resets counter 2 (mechanical position).
Bit 22 (CU3R) = 1: Resets counter 3 (deviation).
Bit 23 (CU4R) = 1: Resets counter 4 (multi-purpose).

To select the type of CLR signal, set bits 23-20 (CLR1-0) of the RENV1 register.

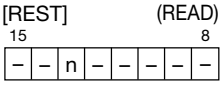
[RENV1] (WRITE)



00: Clears at the falling edge.
01: Clears at the rising edge.
10: Clears at low level.
11: Clears at high level.

To check the CLR signal status, read bit 13 (SLCR) of the RSTS register.

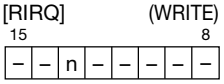
[REST] (READ)



0: CLR signal OFF
1: CLR signal ON

To make the CLR signal an event interrupt factor, set bit 13 (IRCL) of the RIRQ register.

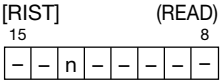
[RIRQ] (WRITE)



1: Outputs the INT signal when the CLR signal resets counters.

To check the event interrupt factor, read bit 13 (ISCL) of the RIST register.

[RIST] (READ)



1: CLR signal which turns on resets counters.

Counter reset command (CUN1R-CUN4R; bit control commands)

[Bit Control Command]

20HEX: Resets the counter 1 (command position) to 0. 20HEX

21HEX: Resets the counter 2 (mechanical position) to 0. 21HEX

22HEX: Resets the counter 3 (deviation) to 0. 22HEX

23HEX: Resets the counter 4 (multi-purpose) to 0. 23HEX

11.10.3 Counter Latch and Counting Condition

With all counters, the counting value can be latched in any of the following five ways by setting the RENV5 (environmental setting 5) register.

(1) LTC signal turns from OFF to ON.
(2) ORG signal turns from OFF to ON.
(3) Comparator 4 condition is satisfied.
(4) Comparator 5 condition is satisfied.
(5) The command is written.

Also, the present speed can be latched in place of the counter 3 (deviation) and the latching condition due to hardware timing [abovementioned (1) to (4)] can be terminated.

The LTC signal input timing can be set by the RENV1 (environmental setting 1) register. The INT signal can be output when the LTC signal or ORG signal as an event interrupt factor lets counters be latched.

To select the factor to latch counters 1 to 4, set bits 13-12 (LTM1-0) of the RENV5 register.

[RENV5] (WRITE)

15							8
–	–	n	n	–	–	–	–

00: LTC signal turning from OFF TO ON
01: ORG signal turning from OFF to ON
10: Comparator 4 condition satisfied
11: Comparator 5 condition satisfied

To latch the present speed in place of the counter 3 (deviation), set bit 14 (LTFD) of the RENV5 register at 1.

[RENV5] (WRITE)

15							8
–	n	–	–	–	–	–	–

To terminate the latching condition caused by hardware timing [abovementioned (1) to (4)], set bit 15 (LTOF) of the RENV5 register at 1.

[RENV5] (WRITE)

15							8
n	–	–	–	–	–	–	–

To select the LTC signal timing, set bit 23 (LTCL) of the RENV1 register.

[RENV1] (WRITE)

23							16
n	–	–	–	–	–	–	–

0: Falling edge
1: Rising edge

To select event interrupt factors, set bits 14 (IRLT) and 15 (IROT) of the RIRQ register.

[RIRQ] (WRITE)

15							8
n	n	–	–	–	–	–	–

Bit 14 (IRLT) = 1: Outputs the $\overline{INT}$ signal when the LTC signal turns on to latch counter values.

Bit 15 (IROT) = 1: Outputs the $\overline{INT}$ signal when the ORG signal turns on to latch counter values.

To check the event interrupt factor, read bits 14 (RIST) and 15 (ISOL) of the RIST register.

[RIST] (READ)

15							8
n	n	–	–	–	–	–	–

Bit 14 (ISLT) = 1: LTC signal latches counter values.

Bit 15 (ISOL) = 1: ORG signal latches counter values.

To check the LTC signal status, read bit 14 (SLTC) of the RSTS register.

[RSTS] (READ)

15							8
–	n	–	–	–	–	–	–

0: LTC signal OFF 1: LTC signal ON

The counter latch command 29HEX (LTCH: bit control command) latches counters 1 to 4.

[Bit Control Command]

29HEX

The counter 1 (command position) stops counting when it is so set by the RMD (operation mode) register and during operation in timer mode. Counters 2, 3 and 4 can be set by the RENV3 (environmental setting 3) register so that they stop counting. Also, by setting the RENV3 register, backlash/slip correction can stop counters from counting. Since the counter 4 can be operated only under the condition the BSY signal is low level, it can be used to control the time from the start by selecting the signal of (reference clock x 1/2) for the input.

To stop the counter 1, set bit 11 (MCCE) of the RMD register.

[RMD] (WRITE)

15							8
–	–	–	–	n	–	–	–

1: Stops the counter 1 (command position) from counting.

To stop counters 2 to 4, set bits 31-29 (CU2H-4H) of the RENV3 register.

[RENV3] (WRITE)

31							24
n	n	n	0	–	–	–	–

Bit 29 (CU2H) = 1: Stops the counter 2 (mechanical position).

Bit 30 (CU3H) = 1: Stops the counter 3 (deviation)

Bit 31 (CU4H) = 1: Stops the counter 4 (multi-purpose).

To select whether backlash/slip correction stops counters from counting or not, set bits 27-24 (CU4B-1B) of the RENV3 register.

[RENV3] (WRITE)

31							24
–	–	–	0	n	n	n	n

Bit 16 (CU1B) = 1: Operates the counter 1 (command position).

Bit 17 (CU2B) = 1: Operates the counter 2 (mechanical position).

Bit 18 (CU3B) = 1: Operates the counter 3 (deviation)

Bit 19 (CU4B) = 1: Operates the counter 4 (multi-purpose)

To select the counting condition of counter 4, set bit 14 (BSYC) of the RENV3 register.

[RENV3] (WRITE)

15							8
–	n	–	–	–	–	–	–

1: The counter 4 operates only under the condition the BSY signal is low level.

11.11 Comparators

11.11.1 Types and Functions of Comparators

The PCL6045 provides five 28-bit comparators for each axis. Comparators 1 to 4 can select the comparing counters from counters 1 to 4. Besides counters 1 to 4, the comparator 5 can select the in-position counter or present speed for comparison. The comparator 5 has a preregister. There are nine types of comparing methods and four types of actions initiated when the comparing condition is satisfied.

Comparator conditions are set by RENV4 (environmental setting 4) and RENV5 (environmental setting 5) registers. These comparators can be used to:

- Output the $\overline{\text{INT}}$ signal, externally output comparison result and start in internal synchronization.
- Stop the chip from generating pulses, immediately or after deceleration.
- Replace the operation data with preregister data (to change the present speed).
- Output soft limit signals.
- Detect the out-of-step condition of stepping motor using the counter 3 (deviation)
- Output the synchronization signal using the counter 4 (multi-purpose).

Comparators can select respective comparing subjects from the table below.

	Comparator 1	Comparator 2	Comparator 3	Comparator 4	Comparator 5
Comparing subject	C1C1-0	C2C1-0	C3C1-0	C4C1-0	C5C2-0
Counter 1	00	00	00	00	000
Counter 2	01	01	01	01	001
Counter 3	10	10	10	10	010
Counter 4	11	11	11	11	011
In-position counter	—	—	—	—	100
Present speed	—	—	—	—	101
Preregister	—	—	—	—	Provided
Major application	+SL	–SL		IDX output	

- SL and –SL stand for soft limit.
- If the counter 3 (deviation) is selected for the comparing counter, the absolute value of the counter is compared with the comparator data. (Range of absolute data is 0 to 32,767)
- Bit map of comparing data setting value is as follows:
  C1C1-0 (bits 1-0 of RENV4) C2C1-0 (bits 9-8 of RENV4)
  C3C1-0 (bits 17-16 of RENV4) C4C1-0 (bits 25-24 of RENV4)
  C5C2-0 (bits 2-0 of RENV5)

Comparators can select respective comparing methods from the table below.

Comparing method	Comparator 1 C1S2-0	Comparator 2 C2S2-0	Comparator 3 C3S2-0	Comparator 4 C4C3-0	Comparator 5 C5S2-0
Comparator = Comparing counter (no relation with counting direction)	001	001	001	0001	001
Comparator = Comparing counter (only at counting up)	010	010	010	0010	010
Comparator = Comparing counter (only at counting down)	011	011	011	0011	011
Comparator > Comparing counter	100	100	100	0100	100
Comparator < Comparing counter	101	101	101	0101	101
Used as soft limit	110	110	—	—	—
IDX (synchronization signal) output (no relation with counting direction)	—	—	—	1000	—
IDX (synchronization signal) output (only at counting up)	—	—	—	1001	—
IDX (synchronization signal) output (only at counting down)	—	—	—	1010	—

- SL and –SL stand for soft limit.
- When used as soft limit, the comparator 1 is for a limit in plus side and the comparator method is (comparator < comparing counter). And the comparator 2 is for a limit in minus side and the comparing method is (comparator > comparing counter). For the comparing counter, select the counter 1 (command position).
- C3S2-0 of comparator 3 is prohibited to set at 110. Other setting values are all for comparing condition not satisfied.
- To output the IDX (synchronized signal) by setting C4S3-0 of comparator 4 at 1000, 1001 or 1010, select the counter 4 (multi-purpose) as the comparing counter. Any other counter cannot be selected. Also, set the comparator at a positive value.
- Bit map of comparing method setting value is as follows:
  C1S2-0 (bits 4-2 of RENV4) C2C2-0 (bits 12-10 of RENV4)
  C3S2-0 (bits 20-18 of RENV4) C4S3-0 (bits 29-26 of RENV4)
  C5S2-0 (bits 5-3 of RENV5)

Comparators can select the action initiated when the condition is satisfied.

Action intiated by condition satisfied	Comparator 1 C1D1-0	Comparator 2 C2D1-0	Comparator 3 C3D1-0	Comparator 4 C4D1-0	Comparator 5 C5D1-0
No action	00	00	00	00	00
Immediate stop	01	01	01	01	01
Stop after decel.	10	10	10	10	10
Change of data to preregister data	11	11	11	11	11

- “No action” is mainly for INT output, external output of comparison result and internal synchronization start.
- “Change of data to preregister data” is main for changing the present speed.
- Bit map of action selecttion is as follows:
  C1D1-0 (bits 6-5 of RENV4) C2D1-0 (bits 14-13 of RENV4)
  C3D1-0 (bits 22-21 of RENV4) C4D1-0 (bits 31-30 of RENV4)
  C5D1-0 (bits 7-6 of RENV5)

For output of the $\overline{INT}$ signal, external output of comparing result and internal synchronization start, set as follows.

To output the $\overline{INT}$ signal when the comparator condition is satisfied, set bit 12-8 (IRC5-1) of the RIRQ register.

[RIRQ] (WRITE)

15							8
–	–	–	n	n	n	n	n

Bit 8 (IRC1) = 1: $\overline{INT}$ signal output when comparator 1 condition is satisfied.
Bit 9 (IRC2) = 1: $\overline{INT}$ signal output when comparator 2 condition is satisfied.
Bit 10 (IRC3) = 1: $\overline{INT}$ signal output when comparator 3 condition is satisfied.
Bit 11 (IRC4) = 1: $\overline{INT}$ signal output when comparator 4 condition is satisfied.
Bit 12 (IRC5) = 1: $\overline{INT}$ signal output when comparator 5 condition is satisfied.

To check the event interrupt factor, read bits 12-8 (ISC1-5) of the RIST register.

[RIST] (READ)

15							8
–	–	–	n	n	n	n	n

Bit 8 (IRC1) = 1: Comparator 1 condition satisfied
Bit 9 (IRC2) = 1: Comparator 2 condition satisfied
Bit 10 (IRC3) = 1: Comparator 3 condition satisfied
Bit 11 (IRC4) = 1: Comparator 4 condition satisfied
Bit 12 (IRC5) = 1: Comparator 5 condition satisfied

To check the comparator condition satisfied condition, read bits 12-8 (SCP1-5) of MSTSW.

[MSTSW] (READ)

15							8
–	–	–	n	n	n	n	n

Bit 8 (SCP1) = 1: Comparator 1 condition satisfied
Bit 9 (SCP2) = 1: Comparator 2 condition satisfied
Bit 10 (SCP3) = 1: Comparator 3 condition satisfied
Bit 11 (SCP4) = 1: Comparator 4 condition satisfied
Bit 12 (SCP5) = 1: Comparator 5 condition satisfied

To select the function of P3/CP1 (+SL) pin, set bits 7-6 (P3M1-0) of the RENV2 register.

[RENV2] (WRITE)

7							0
n	n	–	–	–	–	–	–

00: General-purpose input
01: General-purpose output
10: Output of the CP1 (comparator 1 condition being satisfied) signal in negative logic
11: Output of the CP1 (comparator 1 condition being satisfied) signal in positive logic

To select the function of P4/CP2 (–SL) pin, set bits 9-8 (P4M1-0) of the RENV2 register.

[RENV2] (WRITE)

15							8
–	–	–	–	–	–	n	n

00: General-purpose input
01: General-purpose output
10: Output of the CP2 (comparator 2 condition being satisfied) signal in negative logic
11: Output of the CP2 (comparator 2 condition being satisfied) signal in positive logic

To select the function of P5/CP3 pin, set bits 11-10 (P5M1-0) of the RENV2 register.

[RENV2] (WRITE)

15							8
–	–	–	–	n	n	–	–

00: General-purpose input
01: General-purpose output
10: Output of the CP3 (comparator 3 condition being satisfied) signal in negative logic
11: Output of the CP3 (comparator 3 condition being satisfied) signal in positive logic

To select the function of P6/CP4 pin, set bits 13-12 (P6M1-0) of the RENV2 register.

[RENV2] (WRITE)

15							8
–	–	n	n	–	–	–	–

00: General-purpose input
01: General-purpose output
10: Output of the CP4 (comparator 4 condition being satisfied) signal in negative logic
11: Output of the CP4 (comparator 4 condition being satisfied) signal in positive logic

To select the function of P7/CP5 pin, set bits 15-14 (P7M1-0) of the RENV2 register.

[RENV2] (WRITE)

15							8
n	n	–	–	–	–	–	–

00: General-purpose input
01: General-purpose output
10: Output of the CP5 (comparator 5 condition being satisfied) signal in negative logic
11: Output of the CP5 (comparator 5 condition being satisfied) signal in positive logic

To select output timing of the internal synchronization signal, set bits 19-16 (SYO3-1) or the RENV5 register.

[RENV2] (WRITE)

23							16
–	–	–	–	n	n	n	n

0001: At the time the comparator 1 condition is satisfied
0010: At the time the comparator 2 condition is satisfied
0011: At the time the comparator 3 condition is satisfied
0100: At the time the comparator 4 condition is satisfied
0101: At the time the comparator 5 condition is satisfied
1000: At the start of acceleration
1001: At the end of acceleration
1010: At the start of deceleration
1011: At the end of deceleration
Other: No internal synchronization signal output

11.11.2 Soft Limit Function

Soft limits can be set using comparators 1 and 2. Select the counter 1 (command position) for the counter with which the comparators 1 and 2 compare. With the comparator 1 for the limit of plus side and the comparator 2 for the limit of minus side, stop control is made based on the comparison result and moving direction.

The soft limit function can initiate the following action:

(1) Immediately stop the chip from generating pulses.

(2) Stop the chip from generating pulses after deceleration.

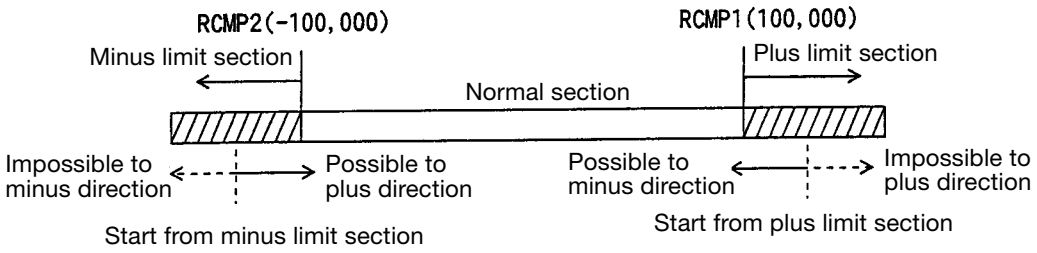
If the start command is written with the soft limit signal turned on, the chip cannot start in the same direction as the soft limit signal, while it can start in the reverse direction to the soft limit signal.

Setting Sample

RENV4 = 00007070HEX: Comparator 1 for the plus soft limit, comparator 2 for the minus soft limit and immediate stop at the time the soft limit signal turns on

RCMP1 = 100,000: Plus soft limit

PCMP2 = –100,000: Minus soft limit



11.11.3 Detection of Out-of-step of Stepping Motor

Using the counter 3 (deviation) and the comparator, the chip detects an out-of-step condition of stepping motor if a deviation between command pulses and feedback pulses from the encoder attached to the stepping motor exceeds the maximum deviation. The action initiated by detection of the out-of-step condition can be selected from those initiated by comparator condition satisfied (see section 11.11.1). The feedback encoder should provide the same resolution as the stepping motor.

The counter 3 can be reset by writing the deviation counter reset command. As the feedback signal input, either the 90° phase difference signals (1, 2 or 4 times multiplied) or two pulses, plus and minus, can be input to EA/$\overline{\text{EB}}$ pins. If EA and EB pins change simultaneously, an error results and the $\overline{\text{INT}}$ signal is output.

Setting Sample

RENV4 = 00360000HEX: Comparator 3 < Counter 3 (deviation) satisfies the condition and initiate immediate stop.
RCMP3 = 32: Maximum deviation is set at 32.
RIRQ = 00000400HEX: $\overline{\text{INT}}$ signal is output when the comparator 3 condition is satisfied.

To select the input of EA/EB pins, set bits 21-20 (EIM1-0) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	–	n	n	0	0	–	–

00: 90° phase difference signal, 1 time multiplied
01: 90° phase difference signal, 2 times multiplied
10: 90° phase difference signal, 4 times multiplied
11: 2 types of pulses, plus and minus

To select the direction of counting EA/EB signals, set bit 22 (EDIR) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	n	–	–	0	0	–	–

0: Counting up when the EA phase is advancing or at the rise of EA signal
1: Counting up when the EB phase is advancing or at the rise of EB signal

To check for EA/EB input error, read bit 16 (ESEE) of the REST register.

[REST] (READ)

15							8
0	0	0	0	0	0	–	n

1: EA/EB input error

To reset the counter 3 (deviation), write the command 22HEX (CUN3R: bit control command).

[Bit Control Command]

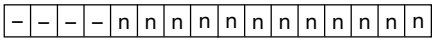
22HEX

11.12 Backlash/Slip Correction

The PCL6045 provides the backlash/slip correction function which enables the chip to output pulses in the preset correction amount at the rate written to the RFA (correction rate) register. The backlash correction is made every time the moving direction changes. The slip correction is made just before generating command pulses irrespective of the moving direction. The correction amount and method are set by the RENV6 (environmental setting 6) register. Even during correction, counters 1 to 4 can be operated by setting the RENV3 (environmental setting 3) register.

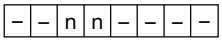
To set the correction amount, use bits 11-0 (BR11-0) of the RENV6 register.
The setting range is 0 to 4,095.

[RENV6] (WRITE)



To select the correction method, set bits 13-12 (ADJ1-0) of the RENV6 register.

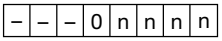
[RENV6] (WRITE)



- 00: No correction
- 01: Backlash correction
- 10: Slip correction

To select effective counters during correction, set bits 27-24 (CU4B-1B) of the RENV3 register.

[RENV3] (WRITE)



Bit 16 (CU1B) = 1: Operates the counter 1 (command position).
Bit 17 (CU2B) = 1: Operates the counter 2 (mechanical position).
Bit 18 (CU3B) = 1: Operates the counter 3 (deviation).
Bit 19 (CU4B) = 1: Operates the counter 4 (multi-purpose).

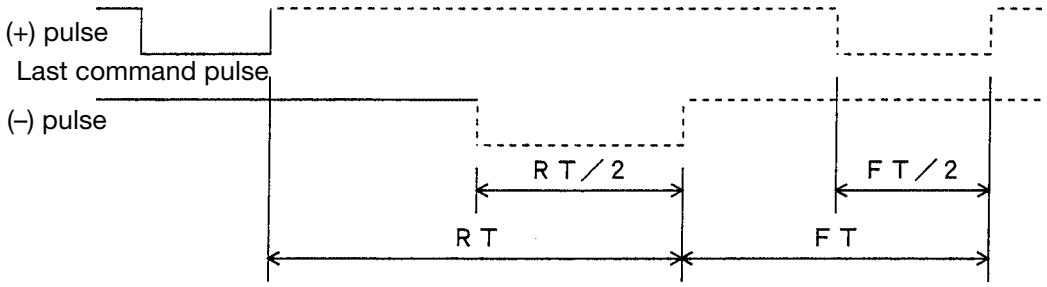
Precaution

For backlash correction, you need to change setting of the in-position mode depending on the moving direction. Set bit 3 (MOD) of the RMD (operation mode) register to the condition of the highest-place bit of RMV (target position) register

For operation in plus direction: MOD = 41_{HEX}
For operation in minus direction: MOD = 49_{HEX}

11.13 Vibration Suppression Function

The PCL6045 provides the function to suppress vibration at the time of stop by adding one pulse each in reverse and forward directions just after outputting all command pulses. Output timings of additional pulses are set by the RENV7 (environmental setting 7) register. The vibration suppression function is valid when the output time in reverse direction (RT) and that in forward direction (FT) are set at other than 0. Dotted lines in the figure below indicate pulses added by the vibration suppression function in the case of operation in plus direction.



To select the time of reverse operation, set bits 15-0 (RT15-0) of the RENV7 register.

[RENV7] (WRITE)

15							8	7							0
n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n

RT setting range: 0 to 65,535
The setting unit is 32 times the reference clock
(approx. 1.6μs with reference clock = 19.6608MHz).
Setting time range: 0 to approx. 0.1 sec

To select the time of forward operation, set bits 31-16 (FT15-0) of the RENV7 register.

[RENV7] (WRITE)

31							24	23							16
n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n

FT setting range: 0 to 65,535
The setting unit is 32 times the reference clock
(approx. 1.6μs with reference clock = 19.6608MHz).
Setting time range: 0 to approx. 0.1 sec

11.14 Synchronized Start

The PCL6045 enables the following operations by setting the RMD (operation mode) register in advance.

- Stop of some axis starts operation.
- Internal synchronization signal starts operation.

The output timing of internal synchronization signal can be selected from nine types by setting the RENV 5 (environmental setting 5) register. Also, by setting the RIRQ (event interrupt factor) register, the INT signal can be output when the internal synchronization signal is output. The event interrupt factor can be checked by reading the RIST register and the operation status can be checked by reading the RSTS (extension status) register.

To select the factor of synchronized start, set bits 19-18 ()MSY1-0) of the RMD register.

[RMD] (WRITE)

23							16
–	–	–	–	n	n	–	–

10: Internal synchronization signal
11: Stop of some axis

To select the axis of which the stop starts operation, set bits 23-20 (MAX3-0) of the RMD register.

[RMD] (WRITE)

23							16
n	n	n	n	–	–	–	–

0001: X axis
0010: Y axis
0100: Z axis
1000: U axis
0011: X and Y axes
0101: X and Z axes
1011: X, Y and U axes
1111: All axes

To select the output timing of synchronization signal, set bits 19-16 (SYO3-0) of the RENV5 register.

[RENV5] (WRITE)

23							16
–	–	–	–	n	n	n	n

0001: Comparator 1 condition satisfied
0010: Comparator 2 condition satisfied
0011: Comparator 3 condition satisfied
0100: Comparator 4 condtion satisfied
0101: Comparator 5 condition satisfied
1000: Start of acceleration
1001: End of acceleration
1010: Start of deceleration
1011: End of deceleration
Other: No internal synchronization signal output

To select the axis of which the internal synchronization signal is used, set bits 21-20 (SYI1-0) of the RENV5 register.

[RENV5] (WRITE)

23							16
–	–	n	n	–	–	–	–

00: X axis
01: Y axis
10: Z axis
11: U axis

To check the operation status, read bits 3-0 (CND) of the RSTS register.

[RSTS] (READ)

7							0
–	–	–	–	n	n	n	n

0011: Waiting for the internal synchronization signal
0100: Waiting for stop of other axis

To select the event interrupt ($\overline{INT}$ output) factor, set bits 12-4 of the RIRQ register.

[RIRQ] (WRITE)

15								8	7						0
–	–	–	n	n	n	n	n	n	n	n	n	–	–	–	–

Bit 4 (IRUS) = 1: Start of acceleration
Bit 5 (IRUE) = 1: End of acceleration
Bit 6 (IRDS) = 1: Start of deceleration
Bit 7 (IRDE) = 1: End of deceleration
Bit 8 (IRC1) = 1: Comparator 1 condition satisfied
Bit 9 (IRC2) = 1: Comparator 2 condition satisfied
Bit 10 (IRC3) = 1: Comparator 3 condition satisfied
Bit 11 (IRC4) = 1: Comparator 4 condition satisfied
Bit 12 (IRC5) = 1: Comparator 5 condition satisfied

To check the event interrupt ($\overline{INT}$ output) factor, read bits 12-4 of the RIST register.

[RIST] (READ)

15								8	7						0
–	–	–	n	n	n	n	n	n	n	n	n	–	–	–	–

Bit 4 (ISUS) = 1: Start of acceleration
Bit 5 (ISUE) = 1: End of acceleration
Bit 6 (ISDS) = 1: Start of deceleration
Bit 7 (ISDE) = 1: End of deceleration
Bit 8 (ISC1) = 1: Comparator 1 condition satisfied
Bit 9 (ISC2) = 1: Comparator 2 condition satisfied
Bit 10 (ISC3) = 1: Comparator 3 condition satisfied
Bit 11 (ISC4) = 1: Comparator 4 condition satisfied
Bit 12 (ISC5) = 1: Comparator 5 condition satisfied

11.14.1 Starting by Stop of Other Axis

With “stop of two or more axes” selected as the starting condition, other axis starts when one of axes selected for stop condition stops after starting if all other axes are in stop condition. Setting sample 1 describes an example of setting “stop of two or more axes is selected for the starting condition. With the setting sample 1, the U axis starts when the X (or Y) axis stops after starting if the Y (or X) axis is in stop condition from the start.

Setting Sample 1

(1) Set bits 19-18 (MSY1-0) of the RMD register of U axis at 11 (to start the U axis when other axes stop.
(2) Set bits 23-20 (MAX3-0) of the RMD register of U axis at 0011 (to select X and Y axes as the axes of which the stop starts the U axis).
(3) Write the start command to the U axis.

Then, start X and Y axes. When both of these axes stop, the U axis starts.

If “stop of other axis” is made the starting condition, the axis which starts based on stop of other axis should be placed in the condition waiting for stop of other axis by writing the start command and then other axis should be started so that its stop starts the other.

For example, write to preregisters of X and Y axes during circular interpolation in progress between X and Y axes, the condition of linear interpolation based on the stop of “all axes” as the condition of the next operation. If other axes (Z and U) have already stopped at the time of completing the circular interpolation between X and Y axes, the linear interpolation between X and Y axes does not start. Because X and Y axes are already in stop condition and do not change from moving to stop at the time they are placed in the condition waiting for “stop of all axes” by the start command for linear interpolation.

Continuous interpolation without changing the interpolation axis can be easily performed by setting preregisters to the next operation conditions (without setting the stop condition). The setting method is described in setting sample 2 below. With this sample, only settings related to the concerned operation are shown and settings of speeds, acceleration rates, etc. are omitted. The reason why to set the $\overline{\text{CSTA}}$ waiting condition (RMD = 0004_0064HEX) is to start the operation after setting all operation conditions.

Setting Sample 2

Setting for continuous interpolation (circular interpolation between X and Y axes to linear interpolation between the same axes) without changing the interpolation axis)

Step	Preregister	X axis	Y axis	Description
1	PRMV	10000	10000	90° circular interpolation between X and Y axes with a radius of 10000
	PRIP	10000	0	
	PRMD	0004_0064HEX	0004_0064HEX	X and Y axes wait for $\overline{\text{CSTA}}$ input
	Write the start command 0351HEX*			Start command for X and Y axes
2	PRMV	10000	5000	Linear interpolation-1 between X and Y axes with ending position (10000, 5000)
	PRMD	0000_0061HEX	0000_0061HEX	
	Write the start command 0351HEX*			Start command for X and Y axes

* Start command for constant-speed operation at FH rate

Turn the $\overline{\text{CSTA}}$ input on after setting as above, continuous interpolation will be made as follows:

(1) 90° circular interpolation between X and Y axes in CW direction with a radius of 10000

(2) Linear interpolation between X and Y axes with the ending position of 10000, 5000

Take care of the steps when performing continuous interpolation by changing the interpolation axis on the way using the preregister function. Setting sample 3 shows the setting method for continuous interpolation by changing the interpolation axis and writing the condition of “stop of other axis” as the starting condition to the preregister.

Setting Sample 3

Setting method for continuous interpolation by changing the interpolation axis on the way (circular interpolation between X and Y axes to linear interpolation between X and Y axes and finally to linear interpolation between X and Z axes)

Step	Preregister	X axis	Y axis	Z axis	Description
1	PRMV	10000	10000	0	90° circular interpolation between X and Y axes with radius 10000
	PRIP	10000	0	0	Z axis: in-positioning with moving amount 0
	PRMD	0004_0064HEX	0004_0064HEX	003C_0041HEX	X and Y axes wait for CSTA input, Z axis waits for stop of X and Y axes.
	Write the start command 0751HEX for constant speed operation at FH rate.				Start command for X, Y and Z axes
2	PRMV	10000	5000	0	X and Y: linear interpolation, Z: in-positioning with moving amount 0
	PRMD	004C_0061HEX	004C_0061HEX	003C_0041HEX	X and Y wait for stop of Z; Z waits for stop of X and Y.
	Write the start command 0751HEX for constant speed operation at FH rate				Start command for X, Y and Z axes
3	PRMV	10000	5000	–5000	Linear interpolation-1 between X and Z
	PRMD	004C_0061HEX	004C_0061HEX	0000_0061HEX	X and Y wait for stop of Z; Z for continuous start
	Write the start command 0551HEX for constant speed operation at FH rate				Start command for X and Z (SPRF of X and Z = 1)

Turn the $\overline{\text{CSTA}}$ input on after setting as above, and continuous operation will be made as follows:

(1) 90° CW circular interpolation between X and Y axes with radius 10000
(2) In-positioning of Z axis (moving amount 0)
(3) Linear interpolation between X and Y axes (10000, 5000)
(4) In-positioning of Z axis (moving amount 0)
(5) Linear interpolation between X and Z axes (10000, –5000)

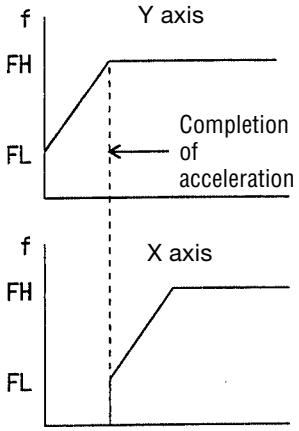
11.14.2 Starting by Internal Synchronization Signal

The RENV5 register allows selection of an output timing of the internal syncyhronizaton signal from nine types. The signal to monitor the internal synchronization signal can be output to an external circuit. Setting sample 1 below is to use the end of acceleration as an internal synchronization signal.

Setting Sample 1

(1) Set bits 19-18 (MSY1-0) of the RMD register of X axis at 10 (to let the internal synchronization start the X axis).
(2) Set bits 21-20 (SYI1-0) of the RMD register of X axis at 01 (to use the internal synchronization signal of Y axis).
(3) Set bits 19-16 (SYO3-0) of the RENV5 register of Y axis at 1001 (to let Y axis output the internal synchronization signal upon completing acceleration).

Write the start command for X and Y axes after setting as above. X axis will start when Y axis completes acceleration.



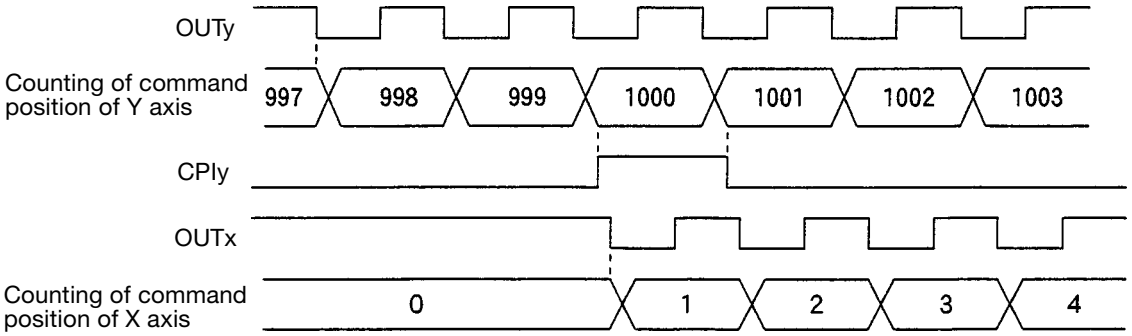
Setting sample 2 is to use the comparator condition satisfied as an internal synchronization signal to start other axis. Take care that the start timing of other axis differs depending on the comparing method of comparator.

Setting Sample 2

To start X axis when Y axis reaches 1000 position by using the counter 1 (command position) and the comparator 1.

(1) Set bits 19-18 (MSY1-0) of the RMD register of X axis at 10.
(To let an internal synchronization signal start X axis)
(2) Set bits 21-20 (SYI1-0) of the RENV5 register of X axis at 01.
(To use the internal synchronization signal of Y axis)
(3) Set bits 19-16 (SY03-0) of the RENV5 register of Y axis at 0001.
(To let Y axis output the internal synchronization signal when the comparator 1 condition is satisfied)
(4) Set bits 1-0 (C1C1-0) of the RENV4 register of Y axis at 00.
(To select the counter 1 as the comparing counter of comparator 1)
(5) Set bits 4-2 (C1S2-0) of the RENV4 register of Y axis at 001.
(To select “comparator 1 = comparing counter” as the comparing method)
(6) Set bits 6-5 (C1D1-0) of the RENV4 register of Y axis at 00.
(To let the comparator 1 condition satisfy initiate no action)
(7) Set the RCMP1 register of Y axis at 1000.
(To set the comparing count value of comparator 1 at 1000.)

(8) Write the start command for X and Y axes.
X axis will start at the following timing.



Precaution

If the moving amount of Y axis is set at 2000 and that of X axis, at 1000 with the sample above, the operation-complete position shifts by one pulse between X and Y axes since X axis = 1 at the time Y axis = 1000. To complete operation of X and Y axes at the same timing, set the RCMP1 value at 1001 or select "comparator 1 < comparing counter" as the comparing condition.

To select the output signal of P0/FUP pin, set bits 1-0 (POM1-0) of the RENV2 register.

[RENV2] (WRITE)

7						1	0
–	–	–	–	–	–	n	n

10: FUP (acceleration under progress) signal

To select the output signal of P1/FDW pin, set bits 3-2 (P1M1-0) of the RENV2 register.

[RENV2] (WRITE)

7							0
–	–	–	–	n	n	–	–

10: FDW (deceleration under progress) signal

To select the output logic of P0 (one-shot)/FUP pin, set bit 16 (P0L) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	–	–	–	0	0	–	n

0: Negative logic
1: Positive logic

To select the output logic of P1 (one-shot)/FDW pin, set bit 17 (P1L) of the RENV2 register.

[RENV2] (WRITE)

23							16
–	–	–	–	0	0	n	–

0: Negative logic
1: Positive logic

To select the function of P3/CP1 (+SL) pin, set bits 7-6 (P3M1-0) of the RENV2 register.

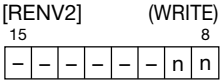
[RENV2] (WRITE)

7							0
n	n	–	–	–	–	–	–

10: Output of CP1 (comparator 1 condition satisfied) signal in negative logic
11: Output of CP1 (comparator 1 condition satisfied) signal in positive logic

To select the function of P4/CP2 (–SL) pin, set bits 9-8 (P4M1-0) of the RENV2 register.

[RENV2] (WRITE)

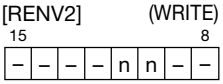


10: Output of CP2 (comparator 2 condition satisfied) signal in negative logic

11: Output of CP2 (comparator 2 condition satisfied) signal in positive logic

To select the function of P5/CP3 pin, set bits 11-10 (P5M1-0) of the RENV2 register.

[RENV2] (WRITE)

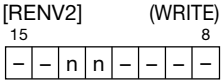


10: Output of CP3 (comparator 3 condition satisfied) signal in negative logic

11: Output of CP3 (comparator 3 condition satisfied) signal in positive logic

To select the function of P6/CP4 pin, set bits 13-12 (P6M1-0) of the RENV2 register.

[RENV2] (WRITE)

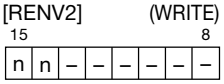


10: Output of CP4 (comparator 4 condition satisfied) signal in negative logic

11: Output of CP4 (comparator 4 condition satisfied) signal in positive logic

To select the function of P7/CP5 pin, set bits 15-14 (P7M1-0) of the RENV2 register.

[RENV2] (WRITE)



10: Output of CP5 (comparator 5 condition satisfied) signal in negative logic

11: Output of CP5 (comparator 5 condition satisfied) signal in positive logic

11.15 Interrupt Signal Output

The PCL6045 can output the interrupt signal ($\overline{INT}$ signal) against 17 types of error factors and 19 types of event factors. Error interrupt factors let the chip output the $\overline{INT}$ signal unconditionally, while event interrupt factors to initiate the $\overline{INT}$ signal are selected by setting the RIRQ register.

The chip keeps outputting the $\overline{INT}$ signal until all interrupt factors are cleared from all axes. Error interrupt factors are cleared when writing the "REST (error factor) register read command." Event interrupt factors are cleared when writing the "RIST (event factor) register read command." To judge the interrupt generating axis and to clear the interrupt factors, read the REST registers of all operating axes and read all contents of RIST registers where event interrupt factors are selected. The interrupt generating status can be checked by reading the main status (MSTSW).

The output of $\overline{INT}$ signal can be masked by setting the INTM bit of RENV1 (environmental setting 1) register at 1. If the output is masked, an interrupt condition satisfied changes the status but does not change the $\overline{INT}$ signal from high to low level. Also, if the output of $\overline{INT}$ signal is unmasked by setting the INTM bit of RENV1 register at 0 under the condition where the interrupt condition is satisfied, the $\overline{INT}$ signal changes to low level. When the $\overline{INT}$ pin is not used, place it in open condition.

If multiple chips are used, $\overline{INT}$ pins cannot be connected with each other in WIRED OR.

To check the interrupt status, read bits 4 (SERR) and 5 (SINT) of the main status (MSTSW).

SERR = 1: Error interrupt (Reading the bit resets the bit at 0.)

SINT = 1: Event interrupt (Reading the bit resets the bit at 0.)

[MSTSW] (READ)

7							0
–	–	n	n	–	0	–	–

To mask the $\overline{INT}$ signal output, set bit 29 (INTM) of the RENV1 register.

1: $\overline{INT}$ signal output is masked.

[RENV1] (WRITE)

31							23
–	–	n	–	–	–	–	–

To read error interrupt factors, write the read command $F2_{HEX}$ (RREST: read command). Data of the REST register (error interrupt factors) will be copied to the buffer.

[Read Command]

$F2_{HEX}$

To read event interrupt factors, write the read command $F3_{HEX}$ (RRIST: read command). Data of the RIST register (event interrupt factors) will be copied to the buffer.

[Read Command]

$F3_{HEX}$

To set event interrupt factors, send the write command AC_{HEX} (WRIRQ; write command). Data of the buffer will be written in the RIRQ register.

[Read Command]

AC_{HEX}

Error Interrupt Factors (Occurrence of an error sets the corresponding bit at 1.)

Error Interrupt Factors	REST Register	
	Bit	Name
Comparator 1 condition is satisfied. (+SL)	0	ESC1
Comparator 2 condition is satisfied. (–SL)	1	ESC2
Comparator 3 condition is satisfied.	2	ESC3
Comparator 4 condition is satisfied.	3	ESC4
Comparator 5 condition is satisfied.	4	ESC5
+EL signal turns on.	5	ESPL
–EL signal turns on.	6	ESM
ALM signal turns on.	7	ESAL
$\overline{\text{CSTP}}$ signal turns on.	8	ESSP
$\overline{\text{CEMG}}$ signal turns on	9	ESEM
SD signal turns on.	10	ESSD
(Always 0)	11	Undefined
Abnormal operation data	12	ESDT
Abnormal stop of an axis during interpolation	13	ESIP
PA/PB input buffer counter overflows.	14	ESPO
In-position counter exceeds the counting range during interpolation.	15	ESAO
EA/EB input error	16	ESEE
PA/PB input error	17	ESPE

Event Interrupt Factors (Select desired event interrupt factors by setting the bits of RIRQ register. Occurrence of a selected event sets the corresponding bit of RIST register at 1.)

Error Interrupt Factors	RIRQ Register		RIST Register	
	Bit	Name	Bit	Name
Automatic stop	0	IREN	0	ISEN
Successive start of next operation	1	IRNX	1	ISNX
Secondary preregisters for operation data write-enabled.	2	IRNM	2	ISNM
Secondary preregister for comparator 5 write-enabled.	3	IRND	3	ISND
Start of acceleration	4	IRUS	4	ISUS
End of acceleration	5	IRUE	5	ISUE
Start of deceleration	6	IRDS	6	ISDS
End of deceleration	7	IRDE	7	ISDE
Comparator 1 condition satisfied	8	IRC1	8	ISC1
Comparator 2 condition satisfied	9	IRC2	9	ISC2
Comparator 3 condition satisfied	10	IRC3	10	ISC3
Comparator 4 condition satisfied	11	IRC4	11	ISC4
Comparator 5 condition satisfied	12	IRC5	12	ISC5
Counters reset by CLR signal	13	IRCL	13	ISCL
LTC input initiates latch of counter value.	14	IRDT	14	ISLT
ORG input initiates latch of counter value.	15	IROL	15	ISOL
SD input turns on.	16	IRSD	16	ISSD
Change of +DR input	17	IRDR	17	ISPD
Change of –DR input			18	ISMD
$\overline{\text{CSTA}}$ signal turns on.	18	IRSA	19	ISSA

12. Characteristics

12.1 Absolute Maximum Ratings

Item		Symbol	Rating
Supply Voltage	(V)	$V_{dd}5$	–0.3 to +7.0
		$V_{dd}3$	–0.3 to +5.0
Input Voltage	(V)	V_{IN}	–0.3 to $V_{dd}5$ + 0.3
Input Current	(mA)	I_{IN}	±10
Storage Temperature	(°C)	T_{stg}	–40 to +125

12.2 Recommended Operating Conditions

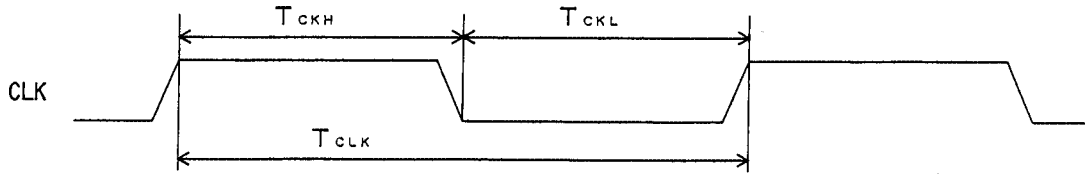
Item		Symbol	Rating
Supply Voltage	(V)	$V_{dd}5$	4.75 to 5.25
		$V_{dd}3$	3.135 to 3.465
Storage Temperature	(°C)	T_J	0 to +70

12.3 DC Characteristics

Item		Symbol	Conditions	Min.	Max.
Static Current Consumption	(µA)	$I_{dd}5$	CLK = 0HZ, no load		32
		$I_{dd}3$			365
Current Consumption	(mA)	$I_{dd}5$	CLK = 20MHz, Output frequency = 6.666667MHz, no load		5
		$I_{dd}3$			240
Output Leakage Current	(µA)	I_{OZ}		–10	10
Input Capacity	(pF)				5.6
Low-level Input Current	(µA)	I_{IL}	Input and I/O pins other than CLK	–200	10
			CLK pin	–10	10
High-level Input Current	(µA)	I_{IH}		–10	10
Low-level Input Voltage	(V)	V_{IL}	Input and I/O pins other than CLK		0.8
			CLK pin		1.0
High-level Input Voltage	(V)	V_{IH}	Input and I/O pins other than CLK	2.0	
			CLK pin	4.0	
Low-level Output Voltage	(V)	V_{OL}	I_{OL} = 1µA		0.05
			I_{OL} = 8mA		0.4
High-level Output Voltage	(V)	V_{OH}	I_{OH} = –1µA	$V_{dd}5$ – 0.05	
			I_{OH} = –8mA	2.4	
Low-level Output Current	(mA)	I_{OL}	V_{OL} = 0.4V		8
High-level Output Current	(mA)	I_{OH}	V_{OH} = 2.4V	–8	
Internal Pull-up Resistor	(kΩ)	R_{UP}		25	500

12.4 AC Characteristics–1 (Reference Clock)

Item		Symbol	Conditions	Min.	Max.
Reference Clock Frequency	(MHz)	f_{CLK}			20
Reference Clock Cycle	(ns)	T_{CLK}		50	
Width of High-level Reference Clock	(ns)	T_{CKH}		20	
Width of Low-level Reference Clock	(ns)	T_{CKL}		20	



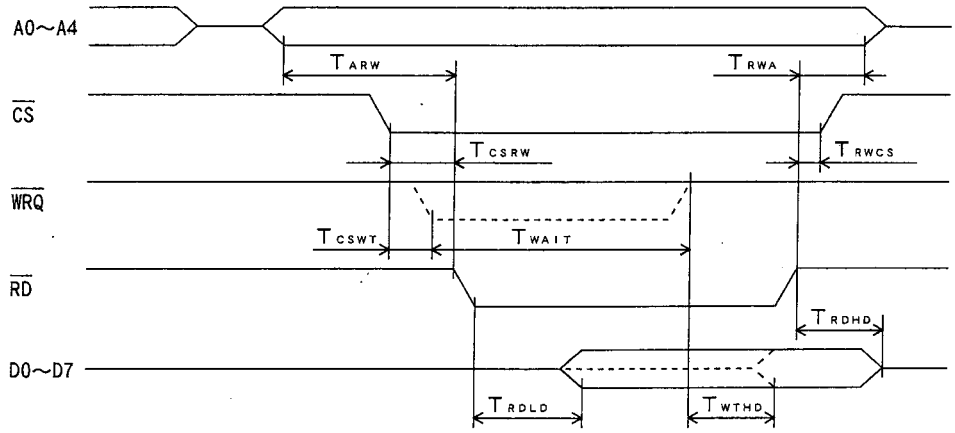
12.5 AC Characteristics–2 (CPU Interface)

12.5.1 CPU Interface–1 (IF1 = H, IF0 = H) Z80

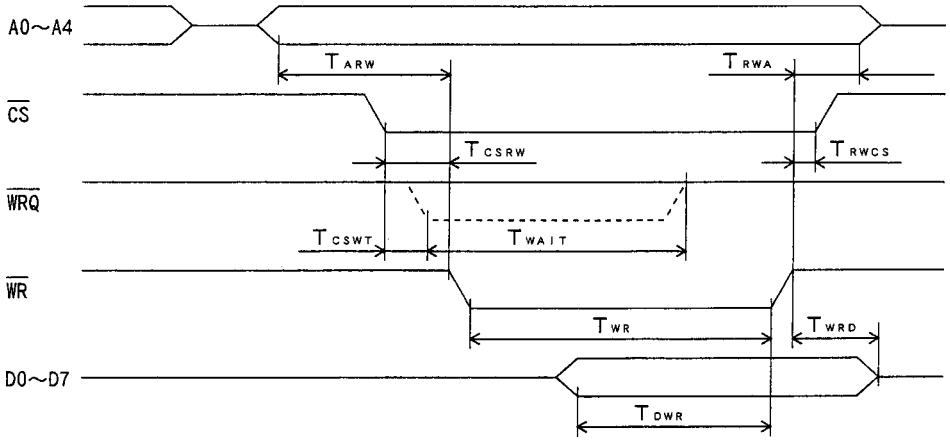
Item	Symbol	Conditions	Min.	Max.
Address Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	T_{ARW}		18	
Address Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	T_{RWA}		0	
$\overline{CS}$ Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	T_{CSRW}		5	
$\overline{CS}$ Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	T_{RWCS}		0	
$\overline{WRQ}$ ON Delay Time to $\overline{CS}$ ↓ (ns)	T_{CSWT}	C_L = 40pF		32
$\overline{WRQ}$ Signal Low-level Time (ns)	T_{WAIT}			$4T_{CLK}+8$
Date Output Delay Time to $\overline{RD}$ ↓ (ns)	T_{RDLD}	C_L = 40pF		43
Data Output Delay Time to $\overline{WRQ}$ ↑ (ns)	T_{WTHD}	C_L = 40pF		26
Data Float Delay Time to $\overline{RD}$ ↑ (ns)	T_{RDHD}	C_L = 40pF		19
$\overline{WR}$ Signal Width (ns)	T_{WR}	Note 1	15	
Data Setup Time to $\overline{WR}$ ↑ (ns)	T_{DWR}		20	
Data Hold Time to $\overline{WR}$ ↑ (ns)	T_{WRD}		0	

Note 1. The time the $\overline{WRQ}$ signal is output is from the time the $\overline{WRQ}$ becomes high level to the time $\overline{WR}$ becomes high level.

Read Cycle



Write Cycle

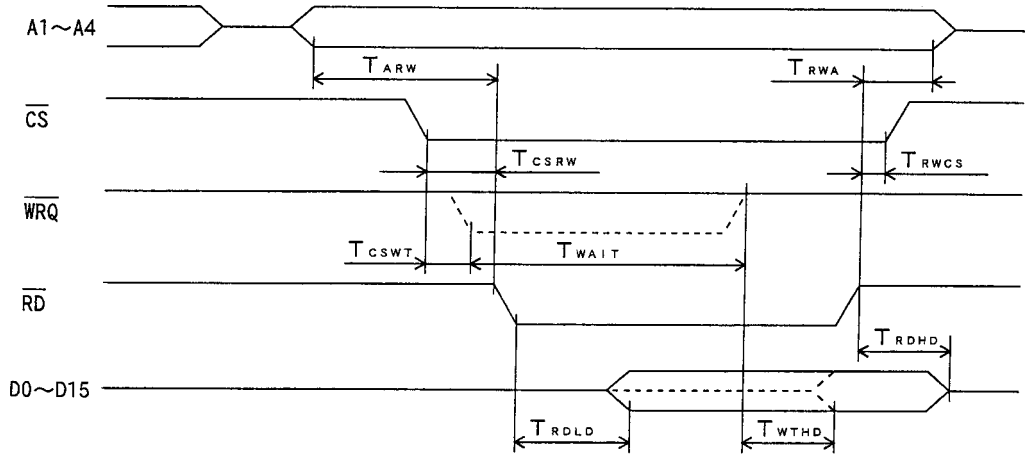


12.5.2 CPU Interface–2 (IF1 = H, IF0 = L) 8086

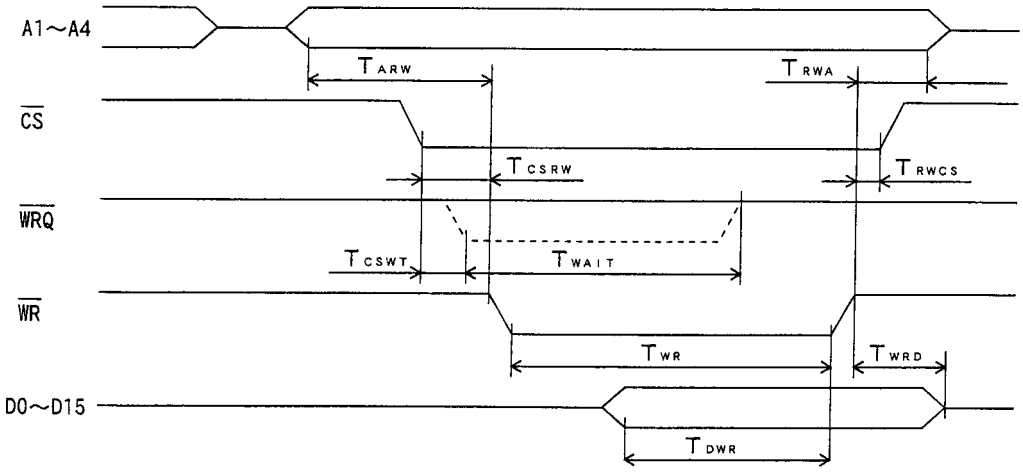
Item	Symbol	Conditions	Min.	Max.
Address Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	TARW		18	
Address Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	TRWA		0	
$\overline{CS}$ Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	TCSRW		5	
$\overline{CS}$ Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	TRWCS		0	
$\overline{WRQ}$ ON Delay Time to $\overline{CS}$ ↓ (ns)	TCSWT	CL = 40pF		32
$\overline{WRQ}$ Signal Low-level Time (ns)	TWAIT			4TCLK +8
Date Output Delay Time to $\overline{RD}$ ↓ (ns)	TRDLD	CL = 40pF		43
Data Output Delay Time to $\overline{WRQ}$ ↑ (ns)	TWTHD	CL = 40pF		26
Data Float Delay Time to $\overline{RD}$ ↑ (ns)	TRDHD	CL = 40pF		19
$\overline{WR}$ Signal Width (ns)	TWR	Note 1	15	
Data Setup Time to $\overline{WR}$ ↑ (ns)	TDWR		20	
Data Hold Time to $\overline{WR}$ ↑ (ns)	TWRD		0	

Note 1. The time the $\overline{WRQ}$ signal is output is from the time the $\overline{WRQ}$ becomes high level to the time $\overline{WR}$ becomes high level.

Read Cycle



Write Cycle

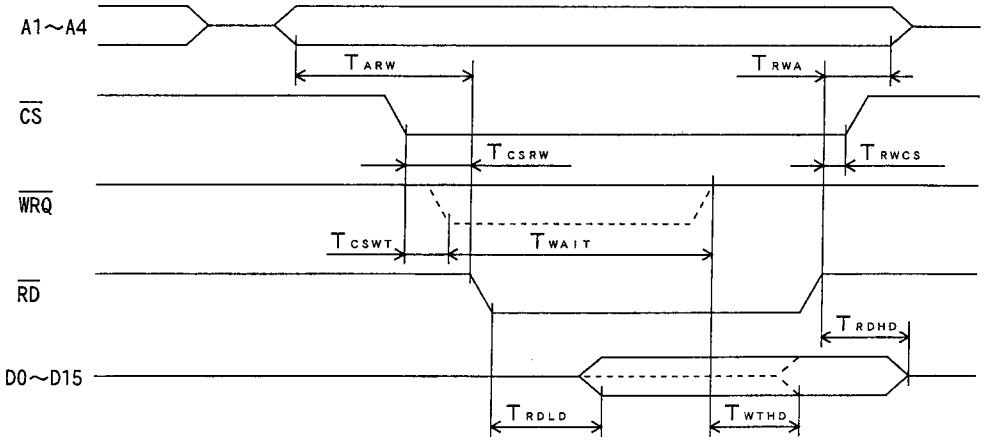


12.5.3 CPU Interface–3 (IF1 = L, IF0 = H) H8

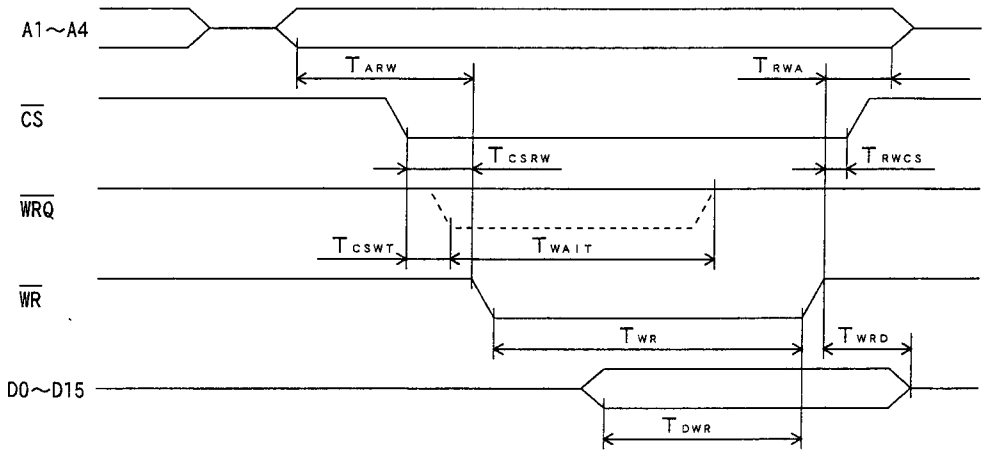
Item	Symbol	Conditions	Min.	Max.
Address Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	TARW		18	
Address Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	TRWA		0	
$\overline{CS}$ Setup Time to $\overline{RD}$, $\overline{WR}$ ↓ (ns)	TCSRW		5	
$\overline{CS}$ Hold Time to $\overline{RD}$, $\overline{WR}$ ↑ (ns)	TRWCS		0	
$\overline{WRQ}$ ON Delay Time to $\overline{CS}$ ↓ (ns)	TCSWT	CL = 40pF		32
$\overline{WRQ}$ Signal Low-level Time (ns)	TWAIT			4TCLK +8
Date Output Delay Time to $\overline{RD}$ ↓ (ns)	TRDLD	CL = 40pF		43
Data Output Delay Time to $\overline{WRQ}$ ↑ (ns)	TWTHD	CL = 40pF		26
Data Float Delay Time to $\overline{RD}$ ↑ (ns)	TRDHD	CL = 40pF		19
$\overline{WR}$ Signal Width (ns)	TWR	Note 1	15	
Data Setup Time to $\overline{WR}$ ↑ (ns)	TDWR		20	
Data Hold Time to $\overline{WR}$ ↑ (ns)	TWRD		0	

Note 1. The time the $\overline{WRQ}$ signal is output is from the time the $\overline{WRQ}$ becomes high level to the time $\overline{WR}$ becomes high level.

Read Cycle



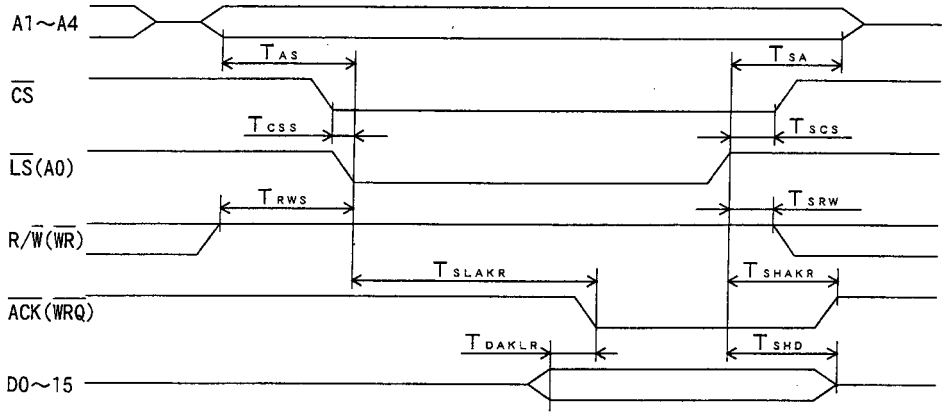
Write Cycle



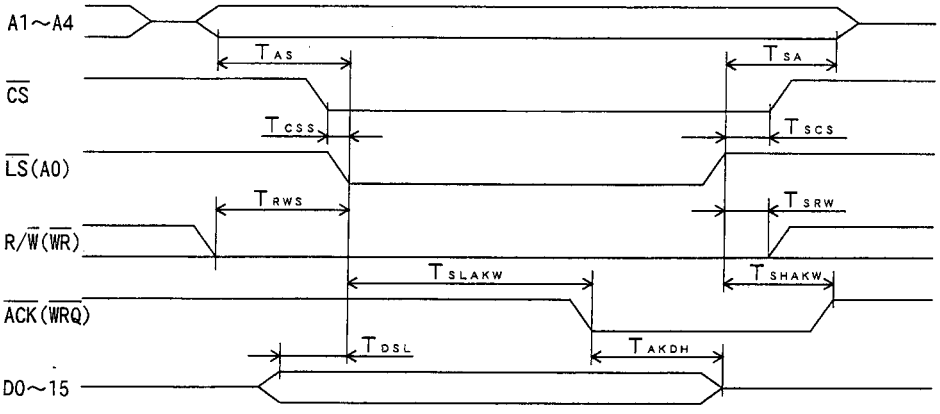
12.5.4 CPU Interface–4 (IF1 = L, IF0 = L) 68000

Item	Symbol	Conditions	Min.	Max.
Address Setup Time to $\overline{LS}\downarrow$ (ns)	T_{AS}		18	
Address Hold Time to $\overline{LS}\uparrow$ (ns)	T_{SA}		0	
$\overline{CS}$ Setup Time to $\overline{LS}\downarrow$ (ns)	T_{CSS}		9	
$\overline{CS}$ Hold Time to $\overline{LS}\uparrow$ (ns)	T_{SCS}		0	
R/$\overline{W}$ Setup Time to $\overline{LS}\downarrow$ (ns)	T_{RWS}		4	
R/$\overline{W}$ Hold Time to $\overline{LS}\uparrow$ (ns)	T_{SRW}		14	
$\overline{ACK}$ ON Delay Time to $\overline{LS}\downarrow$ (ns)	T_{SLAKR}	C_L = 40pF	1T_{CLK}	4T_{CLK} +34
	T_{SLAKW}	C_L = 40pF	1T_{CLK}	4T_{CLK} +34
$\overline{ACK}$ OFF Delay Time to $\overline{LS}\uparrow$ (ns)	T_{SHAKR}	C_L = 40pF		35
	T_{SHAKW}	C_L = 40pF		35
Data Output Preceding time to $\overline{ACL}\downarrow$ (ns)	T_{DAKLR}	C_L = 40pF	1T_{CLK}	
Data Float Delay Time to $\overline{LS}\uparrow$ (ns)	T_{SHD}	C_L = 40pF		29
Data Setup Time to $\overline{LS}\uparrow$ (ns)	T_{DSL}		20	
Data Hold Time to $\overline{ACK}\downarrow$ (ns)	T_{AKDH}		0	

Read Cycle



Write Cycle



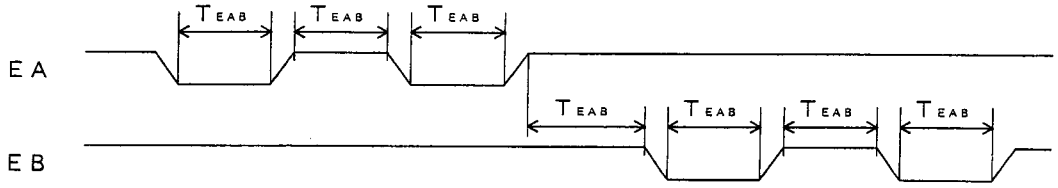
12.6 Operation Timing

Unit: ns

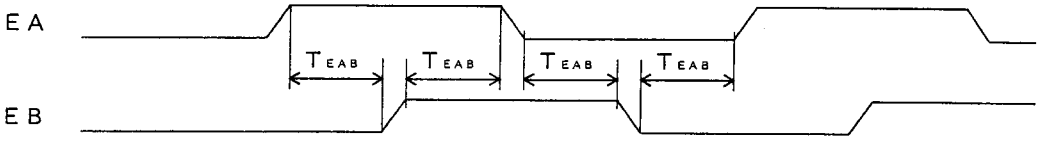
Item		Symbol	Conditions	Min.	Max.
$\overline{\text{RST}}$ Input Signal Width			Note 1	10TCLK	
CLR Input Signal Width				2TCLK	
EA/EB Input Signal Width		TEAB		2TCLK	
EZ Input Signal Width				2TCLK	
PA/PB Input Signal Width		TPAB		2TCLK	
ALM Input Signal Width			Note 2	2TCLK	
INP Input Signal Width			Note 2	2TCLK	
ERC Output Signal Width			Bits 14-12 of RENV1 = 000	254TCLK	255TCLK
			Bits 14-12 of RENV1 = 001	254 x 8TCLK	255 x 8TCLK
			Bits 14-12 of RENV1 = 010	254 x 32TCLK	255 x 32TCLK
			Bits 14-12 of RENV1 = 011	254 x 128TCLK	255 x 128TCLK
			Bits 14-12 of RENV1 = 100	254 x 1024TCLK	255 x 1024TCLK
			Bits 14-12 of RENV1 = 101	254 x 4069TCLK	255 x 4996TCLK
			Bits 14-12 of RENV1 = 110	254 x 8192TCLK	255 x 8192TCLK
			Bits 14-12 of RENV1 = 111	Level output	
+EL/–EL Input Signal Width			Note 2	2TCLK	
SD Input Signal Width			Note 2	2TCLK	
ORG Input Signal Width			Note 2	2TCLK	
+DR/–DR Input Signal Width			Note 3	2TCLK	
$\overline{\text{PE}}$ Input Signal Width			Note 3	2TCLK	
PCS Input Signal Width				2TCLK	
LTC Input Signal Width				2TCLK	
$\overline{\text{CSTA}}$	Output Signal Width			8TCLK	
	Input Signal Width			5TCLK	
$\overline{\text{CSTP}}$	Output Signal Width			8TCLK	
	Input Signal Width			5TCLK	
$\overline{\text{BSY}}$ Signal ON Delay Time		TCMDBSY			5TCLK
		TSTABSY			7TCLK
Start Delay Time		TCMDPLS			15TCLK
		TSTAPLS			17TCLK

Notes:
1. Practically, 10 cycles of CLK signal should be input while the RST pin is low level.
2. If the input filter is made valid by setting bit 26 (FLTR) of the RENV1 register, the minimum time is 80TCLK.
3. If the input filter is made valid by setting bit 27 (DRF) of the RENV1 register, the minimum time is 655,360TCLK.
4. Abovementioned signals are commonly provided to all axes.

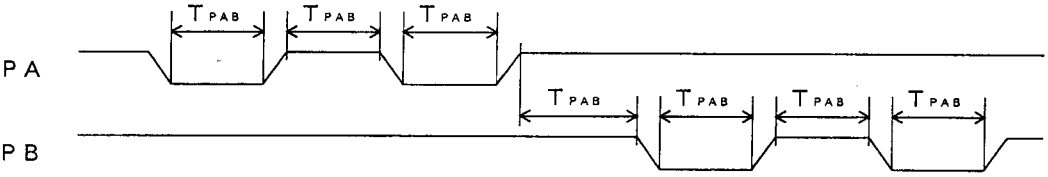
(1) When EA/EB pins are in 2-pulse mode



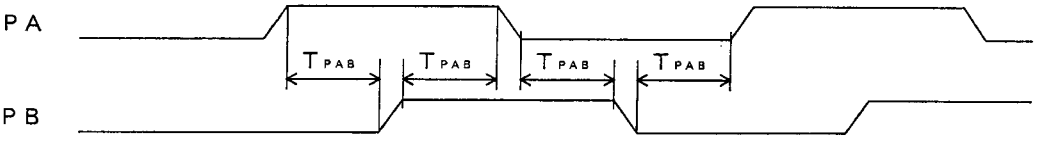
(2) When EA/EB pins are in 90° phase differece mode



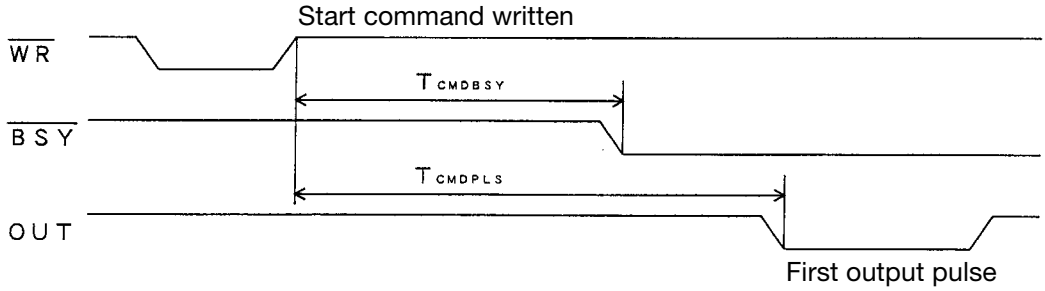
(3) When PA/PB pins are in 2-pulse mode



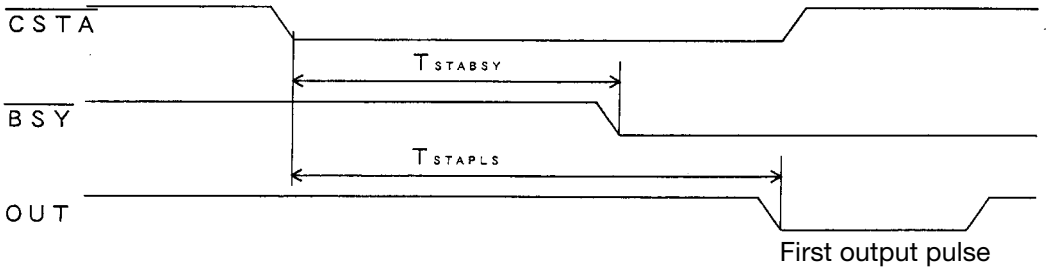
(4) When PA/PB pins are in 90° phase difference mode



(5) Command start timing (I/M = H, B/$\overline{W}$ = H)

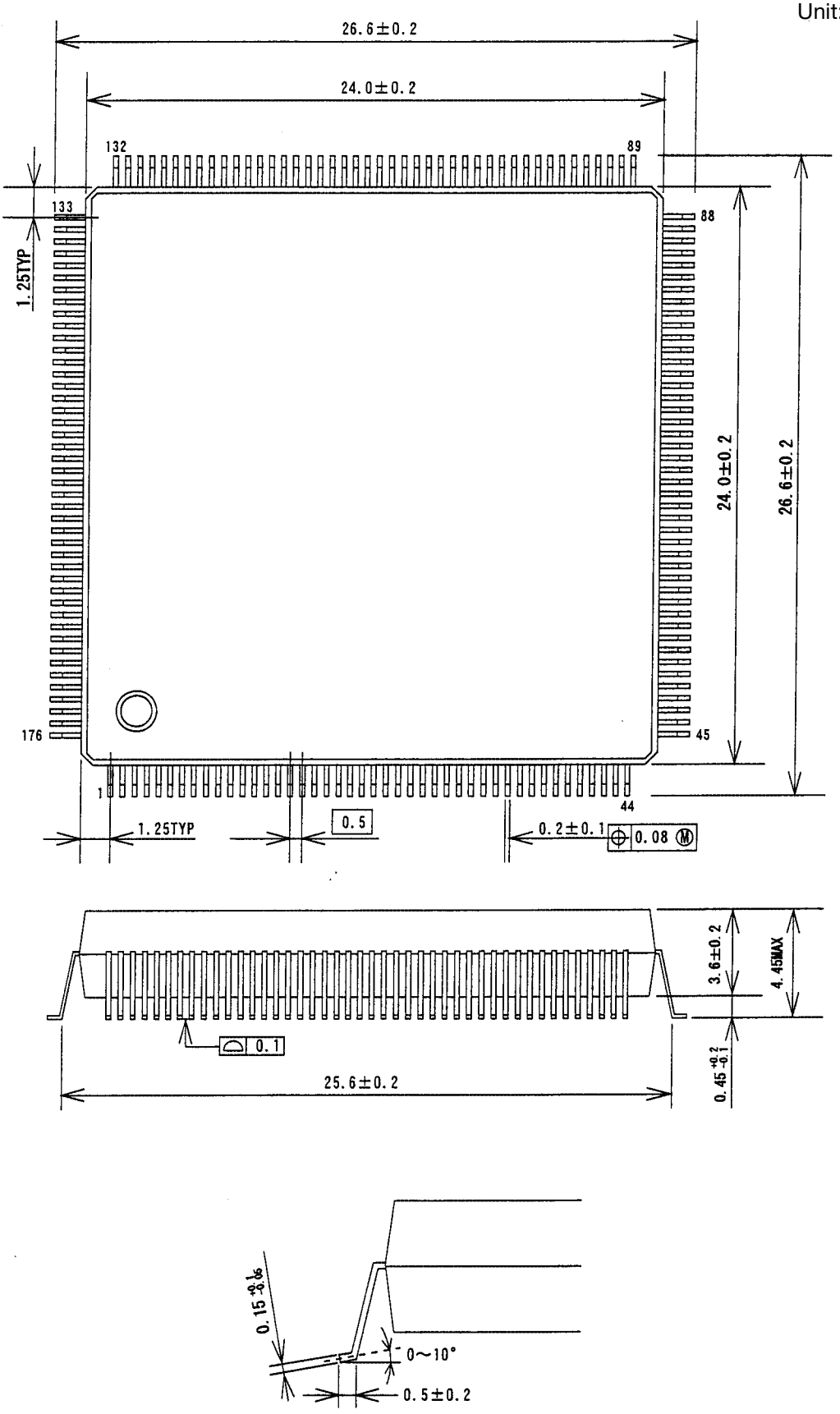


(6) Simultaneous start timing



13. Dimensions

Unit: mm



14. Handling Precautions

14.1 Designing Precautions

(1) In any case the PCL6045 shall not be subjected to a condition exceeding the absolute maximum ratings.
(2) Protect the PCL6045 from receiving any heating effect from environment and keep ambient temperatures as low as possible.
(3) A latch-up condition may cause heat generation and fuming. Take the following precautions.
- Do not make the voltage level of input/output pins higher than +5V and lower than GND.
- Consider the power-up timing.
- Do not apply abnormal noise to the PCL6045.
- Fix the potential of unused input pins at 5V or GND.
- Do not short-circuit the output.
- Protect the PCL6045 against induction and static electricity from a high-voltage generation circuit.

(4) Take care that an excess voltage due to noise, surge and static electricity is not applied to the PCL6045.

14.2 Transportation and Storage Precautions

(1) Handle the package gently. Throwing or dropping it may damage the PCL6045.
(2) Do not store the package where it may be splashed with water or exposed to direct sunlight.
(3) Do not store the package where poisonous or corrosive gases are generated.
(4) Prepare an anti-static container and take care that the PCL6045 may not receive any load.

14.3 Assembling Precautions

(1) Take the following precautions to protect the PCL6045 against damage due to static electricity:
- Ground the instruments and fixtures which are installed at the assembling area.
- Ground the worktable with a conductive mat or the like having resistance. Avoid the metal surface which causes an abrupt electrical discharge with low resistance if an electrified PCL6045 contacts with the surface.
- When picking up the PCL6045 with vacuum, mount a conductive rubber or the like onto the tip of pickup to prevent the PCL6045 from being electrified. Also, use contacts featuring highest possible resistance for connection to lead terminals of PCL6045.

- Tweezers which may contact with pins of PCL6045 should be resistant against static electricity. Avoid metal tweezers if possible. Such tweezers may electrify the PCL6045 through friction and cause electrical discharge.

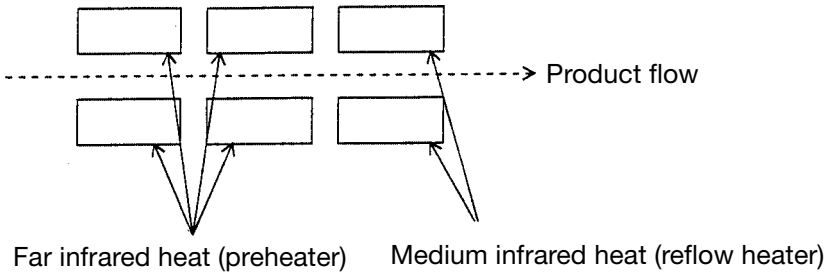
(2) The worker should wear a wrist strap, which should be grounded via 1MΩ resistor.

(3) Use a low-voltage soldering iron and ground it at the tip.

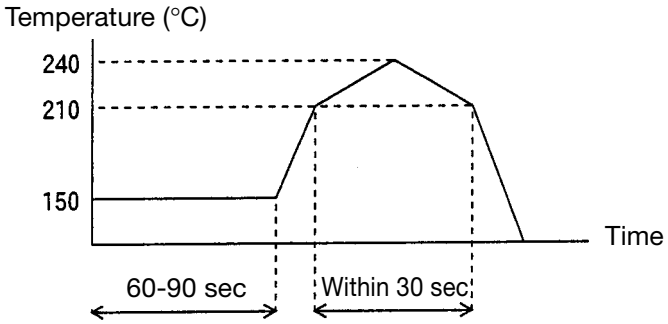
(4) Do not place the PCL6045 or the container near instruments, such as CRT, which generate a high electrical field.

(5) If the fully heating soldering method is used, conduct high-temperature dehumidifying treatment at 125°C for 20 hours.

(6) If soldering is made through an infrared reflow method for reduction of heat stress, the far and medium infrared reflow method is recommended.

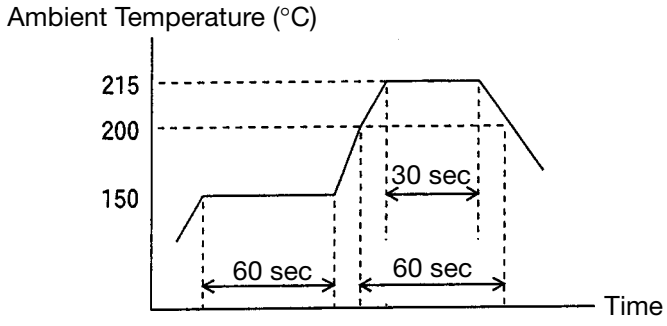


Soldering should be done in such a manner that the time length the package surface and PC board surface are heated to a range of 210°C to 240°C maximum is less than 30 seconds. At the time of reflow, cooling should be done at a rate of lower than 3°C per second.



(7) For the warm-air reflow, use the same procedure as the far infrared method.

(8) For the vapor phase soldering, Florinade FC-70 or the equivalent is recommended as the solution. Time lengths of heating should be within 30 seconds at 215°C and within 60 seconds at 200°C.



(9) In the case of soldering iron, soldering should be done within 10 seconds at maximum 260°C or within 3 seconds at maximum 350°C.

14.4 Other Precautions

(1) If the PCL6045 is intended for use under adverse environmental conditions (humidity, corrosive gases or dirt), take proper measures such as a humidity-resistant coating.

(2) Resin materials used for the package are flame-retardant but not non-inflammable. So, it may be burned or fume. Avoid placing it near an inflammable object.

(3) The PCL6045 is designed for office appliances, communications equipment, measuring instruments and home electric appliances. If you use it for the system of which a trouble or erroneous operation may lead to the dealth or injure the operator, such as nuclear control system, space ship, traffic signal, combustion control system or safety device, take sufficient care.

Appendix

A.1 List of Commands

A.1.1 Operation Commands

COMB0	Mnemonic	Description
05HEX	CMEMG	Emergency stop
06HEX	CMSTA	Output $\overline{\text{CSTA}}$ signal for simultaneous start.
07HEX	CMSTP	Output $\overline{\text{CSTP}}$ signal for simultaneous stop.
40HEX	FCHGL	Immediately change to operation at FL rate.
41HEX	FCHGH	Immediately change to operation at FH rate.
42HEX	FSCHL	Decelerate to FL rate.
43HEX	FSCHH	Accelerate to FH rate.
49HEX	STOP	Stop immediately.
4AHEX	SDSTP	Stop after deceleration.
50HEX	STAFL	Start constant-speed operation at FL rate.
51HEX	STAFH	Start constant-speed operation at FH rate.
52HEX	STAD	Start varied-speed operation 1*1.
53HEX	STUD	Start varied-speed operation 2*2.
54HEX	CNTFL	Output remaining pulses in constant-speed operation at FL rate.
55HEX	CNTFH	Output remaining pulses in constant-speed operation at FH rate.
56HEX	CNTD	Output remaining pulses in varied-speed operation 1*1.
57HEX	CNTUD	Output remaining pulses in varied-speed operation 2*2.

*1. Varied-speed operation 1 is the high-speed operation starting at FH rate with deceleration at the end.
*2. Varied-speed operation 2 is the high-speed operation accelerating from FL to FH rate at the start with deceleration at the end.

A.1.2 General-purpose Port Control Commands

COMB0	Mnemonic	Description
10HEX	P0RST	Set P0 pin at low level.
11HEX	P1RST	Set P1 pin at low level.
12HEX	P2RST	Set P2 pin at low level.
13HEX	P3RST	Set P3 pin at low level.
14HEX	P4RST	Set P4 pin at low level.
15HEX	P5RST	Set P5 pin at low level.
16HEX	P6RST	Set P6 pin at low level.
17HEX	P7RST	Set P7 pn at low level.
18HEX	P0SET	Set P0 pin at high level.
19HEX	P1SET	Set P1 pin at high level.
1AHEX	P2SET	Set P2 pin at high level.
1BHEX	P3SET	Set P3 pin at high level.
1CHEX	P4SET	Set P4 pin at high level.
1DHEX	P5SET	Set P5 pin at high level.
1EHEX	P6SET	Set P6 pin at high level.
1FHEX	P7SET	Set P7 pin at high level.

A.1.3 Control Commands

COMB0	Mnemonic	Description
00HEX	NOP	(Invalid command)
04HEX	SRST	Reset software.
20HEX	CUN1R	Reset counter 1 (command position).
21HEX	CUN2R	Reset counter 2 (mechanical position).
22HEX	CUN3R	Reset counter 3 (deviation).
23HEX	CUN4R	Reset counter 4 (multi-purpose).
24HEX	ERCOUT	Output ERC signal.
25HEX	ERCRST	Reset ERC signal.
26HEX	PRICAN	Cancel operation preregister.
27HEX	PCPCAN	Cancel RCMP5 preregister.
28HEX	STAON	Act for PCS input.
29HEX	LTCH	Act for LTC input.
2AHEX	SPSTA	Initiate the same operation as $\overline{\text{CSTA}}$ input, but for the axis only.
2BHEX	PRISHF	Shift the operation preregister data.
2CHEX	PCPSHF	Shift the RCMP5 preregister data.

A.1.4 Register Control Command

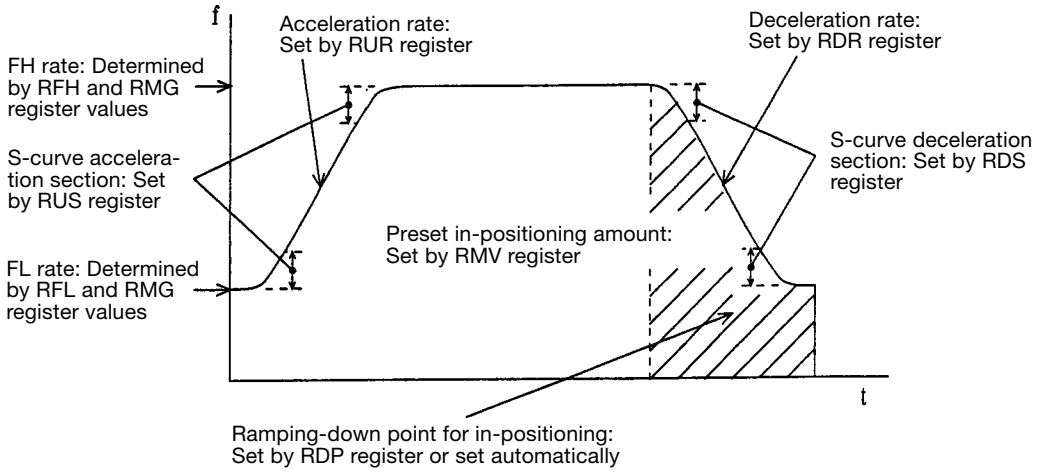
No.	Register	Description	Read Commmand		Write Commmand		2nd Pre-register	Read Commmand		Write Commmand	
			COMB0	Mnemonic	COMB0	Mnemonic		COMB0	Mnemonic	COMB0	Mnemonic
1	RMV	Moving amount, target position	D0HEX	RRMV	90HEX	WRMV	PRMV	C0HEX	RPRMV	80HEX	WPRMV
2	RFL	Initial speed	D1HEX	RFFL	91HEX	WFFL	PRFL	C1HEX	RPRFL	81HEX	WPRFL
3	RFH	Operation speed	D2HEX	RRFH	92HEX	WRFH	PRFH	C2HEX	RPRFH	82HEX	WPRFH
4	RUR	Acceleration rate	D3HEX	RRUR	93HEX	WRUR	PRUR	C3HEX	RPRUR	83HEX	WPRUR
5	RDR	Deceleration rate	D4HEX	RRDR	94HEX	WRDR	PRDR	C4HEX	RPRDR	84HEX	WPRDR
6	RMG	Speed magnification	D5HEX	RRMG	95HEX	WRMG	PRMG	C5HEX	RPRMG	85HEX	WPRMG
7	RDP	Ramping-down point	D6HEX	RRDP	96HEX	WRDP	PRDP	C6HEX	RPRDP	86HEX	WPRDP
8	RMD	Operation mode	D7HEX	RRMD	97HEX	WRMD	PRMD	C7HEX	RPRMD	87HEX	WPRMD
9	RIP	Center of circular interpolation	D8HEX	RRDP	98HEX	WRDP	PRIP	C8HEX	RPRDP	88HEX	WPRIP
10	RUS	S-curve acceleration section	D9HEX	RRUS	99HEX	WRUS	PRUS	C9HEX	RPRUS	89HEX	WPRRS
11	RDS	S-curve deceleration section	DAHEX	RRDS	9AHEX	WRDS	PRDS	CAHEX	RPRDS	8AHEX	WPRDS
12	RFA	Moving amount correct. speed	DBHEX	RRFA	9BHEX	WRFA					
13	RENV1	Environmental setting 1	DCHEX	RRENV1	9CHEX	WRENV1					
14	RENV2	Environmental setting 2	DDHEX	RRENV2	9DHEX	WRENV2					
15	RENV3	Environmental setting 3	DEHEX	RRENV3	9EHEX	WRENV3					
16	RENV4	Environmental setting 4	DFHEX	RRENV4	9FHEX	WRENV4					
17	RENV5	Environmental setting 5	E0HEX	RRENV5	A0HEX	WRENV5					
18	RENV6	Environmental setting 6	E1HEX	RRENV6	A1HEX	WRENV6					
19	RENV7	Environmental setting 7	E2HEX	RRENV7	A2HEX	WRENV7					
20	RCUN1	Counter 1 (command position)	E3HEX	RRCUN1	A3HEX	WRCUN1					
21	RCUN2	Counter 2 (mechanical position)	E4HEX	RRCUN2	A4HEX	WRCUN2					
22	RCUN3	Counter 3 (deviation)	E5HEX	RRCUN3	A5HEX	WRCUN3					
23	RCUN4	Counter 4 (multi-purpose)	E6HEX	RRCUN4	A6HEX	WRCUN4					
24	RCMP1	Comparator 1 data	E7HEX	RRCMP1	A7HEX	WRCMP1					
25	RCMP2	Comparator 2 data	E8HEX	RRCMP2	A8HEX	WRCMP2					
26	RCMP3	Comparator 3 data	E9HEX	RRCMP3	A9HEX	WRCMP3					
27	RCMP4	Comparator 4 data	EAHEX	RRCMP4	AAHEX	WRCMP4					
28	RCMP5	Comparator 5 data	EBHEX	RRCMP5	ABHEX	WRCMP5	PRCP5	CBHEX	RPRCP5	8BHEX	WPRCP5
29	RIRQ	Event interrupt factor setting	ECHEX	RRIRQ	ACHEX	WRIRQ					
30	RLTC1	Counter 1 latch data	EDHEX	RRLTC1							
31	RLTC2	Counter 2 latch data	EEHEX	RRLTC2							
32	RLTD3	Counter 3 latch data	EFHEX	RRLTC3							
33	RLTC4	Counter 4 latch data	F0HEX	RRLTC4							
34	RSTS	Extension status	F1HEX	RRSTS							
35	REST	Error interrupt status	F2HEX	RREST							
36	RIST	Event interrupt status	F3HEX	RRIST							
37	RPLS	In-positioning counter	F4HEX	RRPLS							
38	RSPD	EZ counter, speed monitor	F5HEX	RRSPD							
39	RSDC	Ramping-down point	F6HEX	RRSDC							
40	RIPS	Interpolation status	FFHEX	RRIPS							

A.2 Setting Speed Pattern

Register	Content	Bit length	Setting range	Pre-register
RMV	In-positioning amount	28	–134,217,728 (8000000HEX) to 134,217,727 (7FFFFFFHEX)	PRMV
RFL	Initial (or low) speed	16	1 to 65,535 (0FFFFHEX)	PRFL
RFH	Operation (or high) speed	16	1 to 65,535 (0FFFFHEX)	PRFH
RUR	Acceleration rate	16	1 to 65,535 (0FFFFHEX)	PRUR
RDR	Deceleration rate*	16	0 to 65,535 (0FFFFHEX)	PRDR
RMG	Speed multiplication factor	12	2 to 4,095 (0FFFHEX)	PRMG
RDP	Ramping-down point	24	0 to 16,777,215 (0FFFFFFHEX)	PRDP
RUS	S-curve acceleration range	15	0 to 32,767 (7FFFHEX)	PRUS
RDS	S-curve deceleration range	15	0 to 32,767 (7FFFHEX)	PRDS

* If the RDR register is set at 0, the acceleration rate written to the RUR register is used for deceleration.

Sites to which register data are applied for acceleration and deceleration



A.2.1 RFL: FL Rate Setting Register, 16-bit

This register sets the speed of constant-speed operation at FL rate or the initial speed of varied-speed operation. The setting range is 1 to 65,535 (0FFFFHEX). The practical FL rate is the value obtained through the following equation:

$$\text{FL rate (pps)} = \text{RFL} \times \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

A.2.2 RFH: FH Rate Setting Register, 16-bit

This register sets the speed of constant-speed operation at FH rate or the high speed of varied-speed operation. The setting range is 1 to 65,535 (0FFFF$_{HEX}$). The practical FH rate is the value obtained through the following equation:

$$\text{FH rate (pps)} = \text{RFH} \times \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

A.2.3 RUR: Acceleration Rate Setting Register, 16-bit

This register sets the acceleration rate in varied-speed operation. The setting range is 1 to 65,535 (0FFFF$_{HEX}$). The setting value and acceleration time have the following relations:

In the case of linear acceleration (MSMD of RMD register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RUR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve acceleration with no linear section (MSMD of RMD register = 1 and RUS register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RUR} + 1) \times 8}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve acceleration with linear section (MSMD of RMD register = 1 and RUS register = 0)

$$\text{Acceleration time (s)} = \frac{(\text{RFH} - \text{RFL} + 2 \times \text{RUS}) \times (\text{RUR}) + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

A.2.4 RDR: Deceleration Rate Setting Register, 16-bit

Usually, this register sets the deceleration rate in varied-speed operation in a range of 1 to 65,535 (0FFFF$_{HEX}$). If the ramping-down point is automatically set, the RDR register value is used as deceleration rate. If this RDR register is set at 0, the RUR register value is used for deceleration.

When setting the ramping-down point automatically, set so that:

The deceleration time is equal to, or shorter than, (acceleration time x 2) for the independent operation;

The deceleration time is equal to the acceleration time for the interpolated operation.

If the deceleration time is longer than (acceleration time x 2) in the independent operation or if it is longer than the acceleration time in the interpolated operation, the chip may not decelerate to the FL rate before stop. In such a case, therefore, set MADJ of the RMD register at 1 to turn the FH correction function off and set MSDP of the RMD register at 1 to effect the manual setting of ramping-down point.

The setting value and deceleration time have the following relations:

In the case of linear deceleration (RSMD of RMD register = 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{PDR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve deceleration with no linear section (MSMD of RMD register = 1 and RDS register = 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL}) \times (\text{RDR} + 1) \times 8}{\text{Reference clock frequency (Hz)}}$$

In the case of S-curve deceleration with linear section (MSMD of RMD register = 1 and RDS register > 0)

$$\text{Deceleration time (s)} = \frac{(\text{RFH} - \text{RFL} + 2 \times \text{RDS}) \times (\text{RDR} + 1) \times 4}{\text{Reference clock frequency (Hz)}}$$

A.2.5 RMG: Multiplication Setting Register, 12-bit

This register sets the value by which the RFL and RFH register values are multiplied to provide the practical pulse output rate. The setting range is 2 to 4,095 ($0FFF_{HEX}$). The higher the setting value, the coarser the setting rate; therefore, use the smallest possible multiplication. The setting value has the following relation with the multiplication.

$$\text{Multiplication} = \frac{\text{Reference clock frequency (Hz)}}{(\text{RMG} + 1) \times 65536}$$

Typical Settings of multiplication with reference clock = 19.6608MHz

Setting value	Multiplication	Range of output pulse rate in pps
2999 ($0BB7_{HEX}$)	0.1	0.1 to 6,553.5
1499 ($5DB_{HEX}$)	0.2	0.2 to 13,107.0
599 (257_{HEX})	0.5	0.5 to 32,767.5
299 ($12B_{HEX}$)	1	1 to 65,535
149 (95_{HEX})	2	2 to 131,070
59 ($3B_{HEX}$)	5	5 to 327,675
29 ($1D_{HEX}$)	10	10 to 655,350
14 ($0E_{HEX}$)	20	20 to 1,310,700
5 (5_{HEX})	50	50 to 3,276,750
2 (2_{HEX})	100	100 to 6,553,500

A.2.6 RDP: Ramping-down Point Setting Register, 24-bit

This register sets the value to determine the starting point of deceleration in acceleration/deceleration and in-positioning. Meaning of the value written to the RDP register differs depending on the ramping-down point setting method (MSDP) of the RMD register.

When MSDP of the RMD register is set at 1 (manual setting)

Set the deceleration starting point in the number of pulses in a range of 0 to 16,777,215 (0FFFFFF$_{HEX}$). An optimum value of the ramping-down point is obtained through the following equation.

(1) Linear deceleration (MSMD of RMD register = 0)

$$\text{Optimum value (pulses)} = \frac{(RFH^2 - RFL^2) \times (RDR + 1)}{(RMG + 1) \times 32768}$$

However, if triangular drive is done with the FH correction function OFF (MADJ of RMD register = 1) and with RFH register value not changed, an optimum value is obtained through the following equation. (If idling control is used, substitute the value obtained by subtracting the number of idling pulses from the RMV register value for the RMV in the equation below. The number of idling pulses is 1 to 6 when IDL of RENV5 = 2 to 7.)

$$\text{Optimum value (pulses)} = \frac{RMV \times (RDR + 1)}{PUR + RDR + 2}$$

(2) S-curve deceleration with no linear section (MSMD of RMD register = 1 and RDS register = 0)

$$\text{Optimum value (pulses)} = \frac{(RFH^2 - RFL^2) \times (RDR + 1) \times 2}{(RMG + 1) \times 32768}$$

(3) S-curve deceleration with linear section (MSMD of RMD register = 1 and RDS register > 0)

$$\text{Optimum value (pulses)} = \frac{(RFH + RFL) \times (RFH - RFL + 2 \times RDS) \times (RDR + 1)}{(RMG + 1) \times 32768}$$

Deceleration starts when the in-position counter value becomes equal to, or lower than RDP setting value

.

When MSDP of RMD register is set at 0 (automatic setting)

The RDP register value offsets the automatically set ramping-down point. The setting range is –8,388,608 (800000_{HEX}) to 8,388,607 ($7FFFFFF_{HEX}$). If the offset value is positive, deceleration starts earlier and after deceleration the chip generates pulses at the FL rate. If the offset value is negative, start of deceleration is delayed. If offset is not required, set the register at 0.

If the ramping-down point setting value is smaller than the optimum value, the chip stops generating pulses at a rate higher than the FL rate. On the contrary, if the value is larger than the optimum value, the chip performs constant-speed operation at the FL rate after deceleration.

A.2.7 RUS: S-curve Acceleration Range Setting Register, 15-bit

This register sets the S-curve acceleration section in a range of 1 to 32,767 ($7FFF_{HEX}$). The S-curve acceleration section S_{SU} is obtained through the following equation:

$$S_{SU}\ (pps) = RUS \times \frac{\text{Reference clock frequency (Hz)}}{(RMG + 1) \times 65536}$$

That is, S-curve acceleration is made in the sections from the FL rate to (FL rate + S_{SU}) and from the (FH rate – S_{SU}) to the FH rate. And linear acceleration is applied to the section in between. If the register is set at 0, a value obtained through internal calculation of (RFH – RFL)/2 is substituted, resulting in S-curve acceleration with no linear acceleration section.

A.2.8 RDS: S-curve Deceleration Range Setting Register, 15-bit

This register sets the S-curve deceleration section in a range of 1 to 32,767 ($7FFF_{HEX}$). The S-curve deceleration section S_{SD} is obtained through the following equation:

$$SSD\ (pps) = RDS \times \frac{\text{Reference clock frequency (Hz)}}{(RMG + 1) \times 65536}$$

That is, S-curve acceleration is made in the sections from the FH rate to (FH rate – S_{SD}) and from (FL + S_{SD}) to FL rate. If the register is set at 0, a value obtained through internal calculation of (RFH – RFL)/2 is substituted, resulting in S-curve deceleration with no linear acceleration section.

A.3 List of Labels

Label	Kind	Position	Description
A0	Pin	6	Address bus 0 (LSB)
A1	Pin	7	Address bus 1
A2	Pin	8	Address bus 2
A3	Pin	9	Address bus 3
A4	Pin	10	Address bus 4 (MSB)
ADJ1-0	Register bits	13-12, RENV6	Select moving amount correction method.
ALML	Register bit	9, RENV1	Select ALM signal input logic (0: Negative, 1: Positive)
ALMM	Register bit	8, RENV1	Select ALM signal-initiated action (0: Immediate stop, 1: Stop after deceleration)
ALMu	Pin	134	Driver alarm signal to stop U axis
ALMx	Pin	38	Driver alarm signal to stop X axis
ALMy	Pin	70	Driver alarm signal to stop Y axis
ALMz	Pin	102	Driver alarm signal to stop Z axis
AS15-0	Register bits	15-0, RSPD	Present speed monitor
BR11-0	Register bits	11-0, RENV6	Set backlash/slip correction amount.
BSYC	Register bits	14, RENV3	Operate counter 4 only during operation ($\overline{\text{BSY}}$ = low level).
$\overline{\text{BSYu}}$	Pin	148	Output signal indicating operation in progress in U axis.
$\overline{\text{BSYx}}$	Pin	60	Output signal indicating operation in progress in X axis.
$\overline{\text{BSYy}}$	Pin	81	Output signal indicating operation in progess in Y axis.
$\overline{\text{BSYz}}$	Pin	125	Output signal indicating operation in progress in Z axis.
BUFB0	Byte map	4 with Z80	Read/write from/to input/output buffer (bits 7-0).
BUFB1	Byte map	5 with Z80	Read/write from/to input/output buffer (bits 15-8).
BUFB2	Byte map	6 with Z80	Read/write from/to input/output buffer (bits 23-16).
BUFB3	Byte map	7 with Z80	Read/write from/to input/output buffer (bits 31-24).
BUFW0	Word map	4 with 8086	Read/write from/to input/output buffer (bits 15-0).
BUTW1	Word map	6 with 8086	Read/write from/to input/output buffer (bits 31-16).
C1C1-0	Register bits	1-0, RENV4	Select comparating counter of comparator 1.
C1D1-0	Register bits	6-5, RENV4	Select action initiated when comparator 1 condition is satisfied.
C1S2-0	Register bits	4-2, RENV4	Select comparing method of comparator 1.
C2C1-0	Register bits	9-8, RENV4	Select comparating counter of comparator 2.
C2D1-0	Register bits	14-13, RENV4	Select action initiated when comparator 2 condition is satisfied.
C2S2-0	Register bits	12-10, RENV4	Select comparing method of comparator 2.
C3C1-0	Register bits	17-16, RENV4	Select comparating counter of comparator 3.
C3D1-0	Register bits	22-21, RENV4	Select action initiated when comparator 3 condition is satisfied.
C3S2-0	Register bits	20-18, RENV4	Select comparing method of comparator 3.
C4C1-0	Register bits	25-24, RENV4	Select comparating counter of comparator 4.
C4D1-0	Register bits	31-30, RENV4	Select action initiated when comparator 4 condition is satisfied.
C4S3-0	Register bits	29-26, RENV4	Select comparing method of comparator 4.
C5C2-0	Register bits	2-0, RENV5	Select comparating counter of comparator 5.
C5D1-0	Register bits	7-6, RENV5	Select action initiated when comparator 5 condition is satisfied.
C5S2-0	Register bits	5-3, RENV5	Select comparing method of comparator 5.
$\overline{\text{CEMG}}$	Pin	170	Emergency stop signal
CI21-20	Register bits	9-8, RENV3	Select the input of counter 2 (mechanical position).
CI31-20	Register bits	11-10, RENV3	Select the input of counter 3 (deviation).
CI41-40	Register bits	13-12, RENV3	Select the input of counter 4 (multi-purpose).
CLK	Pin	164	Reference clock (19.6608MHz standard)
CLR1-0	Register bits	21-20, RENV1	Select CLR input mode.
CLRu	Pin	151	Clear counters of U axis.
CLRx	Pin	50	Clear counters of X axis.
CLRy	Pin	86	Clear counters of Y axis.
CLRz	Pin	114	Clear counters of Z axis.
CMEMG	Command	05HEX	Emergency stop
CMSTA	Command	06HEX	Output $\overline{\text{CSTA}}$ (simultaneous start) signal.
CMSTP	Command	07HEX	Output $\overline{\text{CSTP}}$ (simultaneous stop) signal.

Label	Kind	Position	Description
CND3-1	Register bits	3-0, RSTS	Operation status monitor
CNTD	Command	56HEX	Output remaining pulses at FH rate with deceleration at the end.
CMTFH	Command	55HEX	Output remaining pulses at FH rate with no deceleration at the end.
CMTFL	Command	54HEX	Output remaining pulses in FL rate.
CNTUD	Command	57HEX	Output remaining pulses at FH rate with accel. at the start and decel. at the end.
COMB0	Byte map	0 with Z80	Write control command.
COMB1	Byte map	1 with Z80	Designate axis.
COMW	Word map	0 with 8086	Designate axis and write control command.
Counter 1	Circuit		28-bit counter to control command position.
Counter 2	Circuit		28-bit counter to control mechanical position.
Counter 3	Circuit		16-bit counter to count deviation.
Counter 4	Circuit		28-bit universal counter
$\overline{CS}$	Pin	3	Chip select signal
$\overline{CSTA}$	Pin	168	Simultaneous start signal
$\overline{CSTP}$	Pin	169	Simultaneous stop signal
CU1B	Register bit	24, RENV3	Operate counter 2 (mechanical position) even during backlash/slip correction.
CU1C	Register bit	16, RENV3	Let CLR signal reset counter 2 (mechanical position).
CU1R	Register bit	20, RENV3	Lets completion of origin return reset conter 2 (mechanical position).
CU2B	Register bit	25, RENV3	Operate counter 2 (mechanical position) even during backlash/slip correction.
CU2C	Register bit	17, RENV3	Lets CLR signal reset counter 2 (mechanical position).
CU2H	Register bit	29, RENV3	Stop counter 2 (mechanical position) from counting.
CU2R	Register bit	21, RENV3	Let completion of origin return rest counter 3 (deviation).
CU3B	Register bit	26, RENV3	Operate counter 3 (deviation) even during backlash/slip correction.
CU3C	Register bit	18, RENV3	Let CLR signal reset counter 4 (multi-purpose).
CU3H	Register bit	30, RENV3	Stop counter 3 (deviation) from counting.
CU3R	Register bit	22, RENV3	Let completion of origin return reset counter 3 (deviation).
CU4B	Register bit	27, RENV3	Operate counter 4 (multi-purpose) even during backlash/slip correction.
CU4C	Register bit	19, RENV3	Let CLR signal reset counter 4 (multi-purpose).
CU4H	Register bit	31, RENV3	Stop counter 4 (multi-purpose) from counting.
CU4R	Register bit	23, RENV3	Let completion of origin return resets counter 1 (command position).
CUN1R	Command	20HEX	Reset counter 1 (command position).
CUN2R	Command	21HEX	Reset counter 2 (mechanical position).
CUN3R	Command	22HEX	Reset counter 3 (deviation).
CUN4R	Command	23HEX	Reset counter 4 (multi-purpose).
D0	Pin	15	Data bus 0 (LSB)
D1	Pin	16	Data bus 1
D10	Pin	27	Data bus 10
D11	Pin	28	Data bus 11
D12	Pin	29	Data bus 12
D13	Pin	30	Data bus 13
D14	Pin	31	Data bus 14
D15	Pin	32	Data bus 15 (MSB)
D2	Pin	18	Data bus 2
D3	Pin	19	Data bus 3
D4	Pin	20	Data bus 4
D5	Pin	21	Data bus 5
D6	Pin	22	Data bus 6
D7	Pin	23	Data bus 7
D8	Pin	24	Data bus 8
D9	Pin	26	Data bus 9
DIRu	Pin	146	Motor drive direction signal for U axis
DIRx	Pin	58	Motor drive direction signal for X axis
DIRy	Pin	79	Motor drive direction signal for Y axis
DIRz	Pin	123	Motor drive direction signal for Z axis
DRF	Register bit	27, RENV1	Insert +DR/–DR input filter.
DRL	Register bit	25, RENV1	Select +DR/–DR input logic (0; Negative, 1: Positive).

Label	Kind	Position	Description
+DRu	Pin	141	Manual input (+) for U axis
–DRu	Pin	142	Manual input (–) for U axis
+DRx	Pin	46	Manual input (+) for X axis
–DRx	Pin	47	Manual input (–) for X axis
+DRy	Pin	82	Manual input (+) for Y axis
–DRy	Pin	83	Manual input (–) for Y axis
+DRz	Pin	110	Manual input (+) for Z axis
–DRz	Pin	111	Manual input (–) for Z axis
DTMF	Register bit	28, RENV1	Turns direction change timer (0.2ms) off.
EAu	Pin	135	Encoder A phase signal for U axis
EAx	Pin	40	Encoder A phase signal for X axis
EAy	Pin	71	Encoder A phase signal for Y axis
EAz	Pin	103	Encoder A phase signal for Z axis
EBu	Pin	136	Encoder B phase signal for U axis
EBx	Pin	41	Encoder B phase signal for X axis
EBy	Pin	72	Encoder B phase signal for Y axis
EBz	Pin	104	Encoder B phase signal for Z axis
ECZ3-0	Register bits	19-16, RSPD	Allow reading of EZ counter value for origin return.
EDIR	Register bit	22, RENV2	Reverse EA/EB input counting direction.
EIM1-0	Register bits	21-20, RENV2	Select EA/EB input specification.
EIP	Register bit	13, REST	Let stop of an axis during interpolation initiate simultaneous stop.
ELLu	Pin	174	Select end limit signal input logic of U axis.
ELLx	Pin	171	Select end limit signal input logic of X axis.
ELLy	Pin	172	Select end limit signal input logic of Y axis.
ELLz	Pin	173	Select end limit signal input logic of Z axis.
ELM	Register bit	3, RENV1	Select EL signal-initiated action (0: immediate stop, 1: Stop after deceleration).
+ELu	Pin	130	(+) end limit signal of U axis
–ELu	Pin	131	(–) end limit signal of U axis
+ELx	Pin	34	(+) end limit signal of X axis
–ELx	Pin	35	(–) end limit signal of X axis
+ELy	Pin	66	(+) end limit signal of Y axis
–ELy	Pin	67	(–) end limit signal of Y axis
+ELz	Pin	97	(+) end limit signal of Z axis
–ELz	Pin	98	(–) end limit signal of Z axis
EPW2-0	Register bits	14-12, RENV1	Select pulsewidth of ERC output signal.
ERCL	Register bit	15, RENV1	Select ERC signal output logic (0: Negative, 1: Positive).
ERCOUT	Command	24HEX	Output ERC signal.
ERCRST	Command	25HEX	Reset ERC signal which is set for level output.
ERCu	Pin	147	Clear driver's deviation of U axis.
ERCx	Pin	59	Clear driver's deviation of X axis.
ERCy	Pin	80	Clear driver's deviation of Y axis.
ERCz	Pin	124	Clear driver's deviation of Z axis.
EROE	Register bit	10, RENV1	Automatic output of ERC signal
EROR	Register bit	11, RENV1	Automatic output of ERC signal upon completion of origin return
ESAL	Register bit	7, REST	ALM signal stops operation.
ESAO	Register bit	15, REST	In-position counter overflows.
ESC1	Register bit	0, REST	Stop due to comparator 1 condition satsified (+SL)
ESC2	Register bit	1, REST	Stop due to comparator 2 condition satisfied (–SL)
ESC3	Register bit	2, REST	Stop due to comparator 3 condition satisfied (out-of-step detected)
ESC4	Register bit	3, REST	Stop due to comparator 4 condition satisfied
ESC5	Register bit	4, REST	Stop due to comparator 5 condition satisfied
ESDT	Register bit	12, REST	Stop due to abnormal operation data
ESEE	Register bit	16, REST	Occurrence of EA/EB input error
ESEM	Register bit	9, REST	Stop due to $\overline{\text{CEMG}}$ input signal
ESML	Register bit	6, REST	Stop due to –EL input ON
ESOL	Register bit	11, REST	Suspension of moving amount limit in origin return or origin escape.

Label	Kind	Position	Description
ESPE	Register bit	17, REST	Occurrence of PA/PB input error
ESPL	Register bit	5, REST	Stop due to +EL input ON
ESPO	Register bit	14, REST	PA/PB input buffer counter overflows.
ESSD	Register bit	10, REST	Stop after deceleration due to SD input ON.
ESSP	Register bit	8, REST	Stop due to $\overline{\text{CSTP}}$ input ON.
EZL	Register bit	23, RENV2	Select EZ signal input logic (0: Falling edge, 1: Rising edge).
EZu	Pin	137	Encoder Z-phase signal of U axis
EZx	Pin	42	Encoder Z-phase signal of X axis
EZy	Pin	73	Encoder Z-phase signal of Y axis
EZz	Pin	106	Encoder Z-phase signal of Z axis
ETW1-0	Register bit	17-16, RENV1	Set ERC signal OFF timer.
EZD3-0	Register bit	7, 4, RENV3	Set EZ counter for origin return.
FCHGH	Command	41HEX	Immeidately change to FH rate.
FCHGL	Command	40HEX	Immediately change to FL rate.
FLTR	Register bit	26, RENV1	Insert input filter.
FSCHH	Command	43HEX	Change to FH rate by acceleration.
FSCHL	Command	42HEX	Change to FL rate by deceleration.
FT15-0	Register bit	31-16, RENV7	Set FT time for vibration suppression.
IDC2-0	Register bits	22-20, RSPD	Monitor the number of idling pulses (0 to 7).
IDL2-0	Register bits	10-8, RENV5	Set the number of idling pulses (0 to 7).
IF0	Pin	1	Select CPU interface mode 0.
IF1	Pin	2	Select CPU interface mode 1.
IFB	Pin	14	CPU interface busy
INPL	Register bit	22, RENV1	Select INP signal input logic (0: Negative, 1: Positive).
INPu	Pin	150	In-position signal input of U axis
INPx	Pin	49	In-position signal input of X axis
INPy	Pin	85	In-position signal input of Y axis
INPz	Pin	113	In-position signal input of Z axis
$\overline{\text{INT}}$	Pin	11	Interrupt request signal
INTM	Register bit	29, RENV1	Mask $\overline{\text{INT}}$ output pin.
IOP7-0	Sub status bit	7-0, sstsw	Read P7-P0 pin status.
IOPB	Byte map	2 with Z80	Read universal input/output ports.
IPCC	Register bit	19, RIPS	CCW circular interpolation in progress
IPCW	Register bit	18, RIPS	CW circular interpolation in progress
IPE	Register bit	17, RIPS	Linear interpolation in progress with moving amount set by main axis
IPEu	Register bit	7, RIPS	Linear interpolation with U axis as main axis to designate moving amount
IPEx	Register bit	4, RRIPS	Linear interpolation with X axis as main axis to designate moving amount
IPEy	Register bit	5, RIPS	Linear interpolation with Y axis as main axis to designate moving amount
IPEz	Register bit	6, RIPS	Linear interpolation with Z axis as main axis to designate moving amount
IPFu	Register bit	15, RIPS	U axis designates the rate of composite speed constant operation.
IPFx	Register bit	12, RIPS	X axis designates the rate of composite speed constant operation.
IPFy	Register bit	13, RIPS	Y axis designates the rate of composite speed constant operation.
IPFz	Register bit	14, RIPS	Z axis designates the rate of composite speed constant operation.
IPL	Register bit	16, RIPS	Normal linear interpolation in progress
IPLu	Register bit	3, RIPS	U axis is in normal linear interpolation mode.
IPLx	Register bit	0, RIPS	X axis is in normal linear interpolation mode.
IPLy	Register bit	1, RIPS	Y axis is in normal linear interpolation mode.
IPLz	Register bit	2, RIPS	Z axis is in normal linear interpolation mode.
IPSu	Register bit	11, RIPS	U axis is in normal circular interpolation mode.
IPSx	Register bit	8, RIPS	X axis is in normal circular interpolation mode.
IPSy	Register bit	9, RIPS	Y axis is in normal circular interpolation mode.
IPSz	Register bit	10, RIPS	Z axis is in normal circular interpolation mode.
IRC1	Register bit	8, RIPS	INT signal valid when comparator 1 condition is satisfied.
IRC2	Register bit	9, RIPS	INT signal valid when comparator 2 condition is satisfied.
IRC3	Register bit	10, RIPS	INT signal valid when comparator 3 condition is satisfied.

Label	Kind	Position	Description
IRC4	Register bit	11, RIRQ	INT signal valid when comparator 4 condition is satisfied.
IRC5	Register bit	12, RIRQ	INT signal valid when comparator 5 condition is satisfied.
IRCL	Register bit	13, RIRQ	INT signal valid when CLR signal is input and counters are reset.
IRDE	Register bit	7, RIRQ	INT signal valid upon completing deceleration.
IRDR	Register bit	17, RIRQ	INT signal valid when +DR or –DR input changes.
IRDS	Register bit	6, RIRQ	INT signal valid at the start of deceleration.
IREN	Register bit	0, RIRQ	INT signal valid at normal stop.
IRLT	Register bit	14, RIRQ	INT signal valid when LTC signal latches counter.
IRND	Register bit	3, RIRQ	INT signal valid when 2nd preregister for comparator 5 is write-enabled.
IRNM	Register bit	2,RIRQ	INT signal valid when 2nd preregister for operation is write-enabled.
IRNX	Register bit	1, RIRQ	INT signal valid when the next operation is done successively.
IROL	Register bit	15, RIRQ	INT signal valid when ORG input turns on and latches counter value.
IRSA	Register bit	18, RIQ	INT signal valid when $\overline{\text{CSTA}}$ input turns on.
IRSD	Register bit	16, RIRQ	INT signal valid when SD input turns on.
IRUE	Register bit	5, RIRQ	INT signal valid upon completing acceleration.
IRUS	Register bit	4, RIRQ	INT signal valid at the start of acceleration.
ISC1	Register bit	8, RIST	Comparator 1 condition satisfied.
ISC2	Register bit	9, RIST	Comparator 2 condition satisfied.
ISC3	Register bit	10, RIST	Comparator 3 condition satisfied.
ISC4	Register bit	11, RIST	Comparator 4 condition satisfied.
ISC5	Register bit	12, RIST	Comparator 5 condition satisfied.
ISCL	Register bit	13, RIST	When CLR signal turns on and resets counters.
ISDE	Register bit	7, RIST	At the end of deceleration
ISDS	Register bit	6, RIST	At the start of deceleration
ISEN	Register bit	0, RIST	At automatic stop
ISLT	Register bit	14, RIST	When LTC signal turns on and latches counter value.
ISMD	Register bit	18, RIST	–DR signal turns on.
ISND	Register bit	3, RIST	2nd preregister for comparator 5 is write-enabled.
ISNM	Register bit	2, RIST	2nd preregister for operation is write-enabled.
ISNX	Register bit	1, RIST	When the next operation is successively started.
ISOL	Register bit	15, RIST	ORG signal turns on and latches counter value.
ISPD	Register bit	17, RIST	+DR signal turns on.
ISSA	Register bit	19, RIST	CSTA signal turns on.
ISSD	Register bit	16, RIST	SD input turns on.
ISUE	Register bit	5, RIST	At the end of acceleration
ISUS	Register bit	4 RIST	At the start of acceleration
LTCH	Command	29HEX	Serves for LTC input (counter latch).
LTCL	Register bit	23, RENV1	Set operating edge of LTC signal (0: Falling edge, 1: Rising edge).
LTCu	Pin	152	Latch input of U axis
LTCx	Pin	51	Latch input of X axis
LTCy	Pin	87	Latch input of Y axis
LTCz	Pin	115	Latch input of Z axis
LTFD	Register bit	14, RENV5	Latch present speed in place of counter 3.
LTM1-0	Register bits	13-12, RENV5	Set latch timing of counters 1 to 4.
LTOF	Register bit	15, RENV5	Suspend latch by hardware timing.
MADJ	Register bit	26, RMD	FH correction function OFF
MAX3-0	Register bits	23-20, RMD	Select the stop control axis for simultaneous start.
MCCE	Register bit	11, RMD	Stop counter 1 (command position).
METM	Register bit	12, RMD	Operation-complete timing (0: Completion of cycle, 1: completion of pulse)
MINP	Register bit	9, RMD	INP input ON completes operation.
MIPF	Register bit	15, 4MD	Composite speed constant at the time of interpolation
MOD	Register bits	6-0, RMD	Set operation mode.
MPCI	Register bit	14, RMD	Start in-positioning control by PCI input.
MSDE	Register bit	8, RMD	SD signal initiates stop after deceleration.
MSDP	Register bit	13, RMD	Manual setting of ramping-down point

Label	Kind	Position	Description
MSMD	Register bit	10, RMD	S-curve acceleration/deceleration (linear acceleration/deceleration with 0)
MSN1-0	Register bits	17-16, RMD	Sequence number for operation block management
MSPE	Register bit	24, RMD	$\overline{\text{CSTP}}$ input valid
MSPO	Register bit	25, RMD	Output $\overline{\text{CSTP}}$ (simultaneous stop) signal at abnormal stop.
MSTSB0	Byte map	0 with Z80	Read main status (bits 7-0).
MSTSB1	Byte map	1 with Z80	Read main status (bits 15-8).
MSTSW	Word map	0 with 8086	Read main status (bits 15-0
MSY1-0	Register bits	19-18, RMD	Set simultaneous start condition.
NOP	Command	00_{HEX}	(Invalid command)
ORGL	Register bit	7, RENV1	Select ORG sgnal input logic (0: negative, 1: positive).
ORGu	Pin	133	U axis origin signal
ORGx	Pin	37	X axis origin signal
ORGy	Pin	69	Y axis origin signal
ORGz	Pin	101	Z axis origin signal
ORM3-0	Register bits	3-0, RENV3	Select origin return method.
OTP7-0	G.-prp. port	7-0, OTPW	General-purpose ports
OTPB	Byte map	2 with Z80	Change the status of general-purpose output port (valid only for output-designated bits).
OTPW	Word map	2 with 8086	Change the status of general-purpose output port (valid only for output-designated bits).
OUTu	Pin	145	Output command pulses to drive U axis motor.
OUTx	Pin	57	Output command pulses to drive X axis motor.
OUTy	Pin	78	Output command pulses to drive Y axis motor.
OUTz	Pin	122	Output command pulses to drive Z axis motor.
P0L	Register bit	16, RENV2	Select P0 pin output logic (0: negative, 1: positive).
P0u/FUPu	Pin	153	U axis, general-purpose port 0/monitor acceleration status.
P0x/FUPx	Pin	52	X axis, general-purpose port 0/monitor acceleration status.
P0y/FUPy	Pin	89	Y axis, general-purpose port 0/monitor acceleration status.
P0z/FUPz	Pin	116	Z axis, general-purpose port 0/monitor acceleration status.
P1u/FDWu	Pin	154	U axis, general-purpose port 1/monitor deceleration status.
P1x/FDWx	Pin	53	X axis, general-purpose port 1/monitor deceleration status.
P1y/FDWy	Pin	90	Y axis, general-purpose port 1/monitor deceleration status.
P1z/FDWz	Pin	117	Z axis, general-purpose port 1/monitor deceleration status.
P2u/MVCu	Pin	155	U axis, general-purpose port 2/monitor constant-speed operation status.
P2x/MVCx	Pin	54	X axis, general-purpose port 2/monitor constant-speed operation status.
P2y/MVCy	Pin	91	Y axis, general-purpose port 2/monitor constant-speed operation status.
P2z/MVCz	Pin	118	Z axis, general-purpose port 2/monitor constant-speed operation status.
P3u/CP1u(+SLu)	Pin	156	U axis, general-purpose port 3/output comparator 1 (plus soft limit) signal.
P3x/CP1x(+SLx)	Pin	55	X axis, general-purpose port 3/output comparator 1 (plus soft limit) signal.
P3y/CP1y(+SLy)	Pin	92	Y axis, general-purpose port 3/output comparator 1 (plus soft limit) signal.
P3z/CP1z(+SLz)	Pin	119	Z axis, general-purpose port 3/output comparator 1 (plus soft limit) signal.
P4u/CP2u(–SLu)	Pin	157	U axis, general-purpose port 4/output comparator 2 (minus soft limit) signal.
P4x/CP2x(–SLx)	Pin	62	X axis, general-purpose port 4/output comparator 2 (minus soft limit) signal.
P4y/CP2y(–SLy)	Pin	93	Y axis, general-purpose port 4/output comparator 2 (minus soft limit) signal.
P4z/CP2z(–SLz)	Pin	120	Z axis, general-purpose port 4/output comparator 2 (minus soft limit) signal.
P5u/CP3u	Pin	158	U axis, general-purpose port 5/output comparator 3 signal.
P5x/CP3x	Pin	63	X axis, general-purpose port 5/output comparator 3 signal.
P5y/CP3y	Pin	94	Y axis, general-purpose port 5/output comparator 3 signal.
P5z/CP3z	Pin	126	Z axis, general-purpose port 5/output comparator 3 signal.
P6u/CP4u/IDXu	Pin	159	U axis, general-purpose port 6/output comparator 4 signal/output sync. signal.
P6x/CP4x/IDXx	Pin	64	X axis, general-purpose port 6/output comparator 4 signal/output sync. signal.
P6y/CP4y/IDXy	Pin	95	Y axis, general-purpose port 6/output comparator 4 signal/output sync. signal.
P6z/CP4z/IDXz	Pin	128	Z axis, general-purpose port 6/output comparator 4 signal/output sync. signal.
P7u/CP5u	Pin	160	U axis, general-purpose port 7/output comparator 5 signal.
P7x/CP5x	Pin	65	X axis, general-purpose port 7/output comparator 5 signal.
P7y/CP5y	Pin	96	Y axis, general-purpose port 7/output comparator 5 signal.

Label	Kind	Position	Description
P7z/CP5z	Pin	129	Z axis, general-purpose port 7/output comparator 5 signal.
P0M1-0	Register bits	1-0, RENV2	Select P0/FUP pin function.
P0RST	Command	10HEX	Set general-purpose output port P0 at low level.
P0SET	Command	18HEX	Set general-purpose output port P0 at high level.
P1L	Register bit	17, RENV2	Select P1 pin output logic (0: negative, 1: positive).
P1M1-0	Register bits	3-2, RENV2	Select P1/FDW pin function.
P1RST	Command	11HEX	Set general-purpose output port P1 at low level.
P1SET	Command	19HEX	Set general-purpose output port P1 at high level.
P2M1-0	Register bits	5-4, RENV2	Select P2/MVC pin function.
P2RST	Command	12HEX	Set general-purpose output port P2 at low level.
P2SET	Command	1AHEX	Set general-purpose output port P2 at high level.
P3M1-0	Register bits	7-6, RENV2	Select P3/CP1 (+SL) pin function.
P3RST	Command	13HEX	Set general-purpose output port P3 at low level.
P3SET	Command	1BHEX	Set general-purpose output port P3 at high level.
P4M1-0	Register bits	9-8, RENV2	Select P4/CP2 (–SL) pin function.
P4RST	Command	14HEX	Set general-purpose output port P4 at low level.
P4SET	Command	1CHEX	Set general-purpose output port P4 at high level.
P5M1-0	Register bits	11-10, RENV2	Select P5/CP3 pin function.
P5RST	Command	15HEX	Set general-purpose output port P5 at low level.
P5SET	Command	1DHEX	Set general-purpose output port P5 at high level.
P6M1-0	Register bits	13-12, RENV2	Select P6/CP4 pin function.
P6RST	Command	16HEX	Set general-purpose output port P6 at low level.
P6SET	Command	1EHEX	Set general-purpose output port P6 at high level.
P7M1-0	Register bits	15-14, RENV2	Select P7/CP5 pin function.
P7RST	Command	17HEX	Set general-purpose output port P7 at low level.
P7SET	Command	1FHEX	Set general-purpose output port P7 at high level.
PAu	Pin	138	U axis, manual pulser A-phase input
PAx	Pin	43	X axis, manual pulser A-phase input
PAy	Pin	74	Y axis, manual pulser A-phase input
PAz	Pin	107	Z axis, manual pulser A-phase input
PBu	Pin	139	U axis, manual pulser B-phase input
PBx	Pin	44	X axis, manual pulser B-phase input
PBy	Pin	75	Y axis, manual pulser B-phase input
PBz	Pin	108	Z axis, manual pulser B-phase input
PCPCAN	Command	27HEX	Cancel preregister PRCP5 for PCMP5.
PCSL	Register bit	24, RENV1	Select PCSn signal input logic (0: negative, 1: positive).
PCSu	Pin	143	Start in-position control on U axis.
PCSx	Pin	48	Start in-position control on X axis.
PCSy	Pin	84	Start in-position control on Y axis.
PCSz	Pin	112	Start in-position control on Z axis.
PDIR	Register bit	26, RENV2	Reverse PA/PB input counting direction.
PEu	Pin	140	Make PA, PB, +DR and –DR valid on U axis.
PEx	Pin	45	Make PA, PB, +DR and –DR valid on X axis.
PEy	Pin	76	Make PA, PB, +DR and –DR valid on Y axis.
PEz	Pin	109	Make PA, PB, +DR and –DR valid on Z axis.
PIM1-0	Register bits	25-24, RENV2	Select PA/PB input function.
PMD2-0	Register bits	2-0, RENV1	Select output pulse mode.
PRICAN	Command	26HEX	Cancel operation preregister.
RCMP1	Register		Data subjected to comparison by comparator 1
RCMP2	Register		Data subjected to comparison by comparator 2
RCMP3	Register		Data subjected to comparison by comparator 3
RCMP4	Register		Data subjected to comparison by comparator 4
RCMP5	Register		Data subjected to comparison by comparator 5
RCUN1	Register		Counter 1 (command position)
RCUN2	Register		Counter 2 (mechanical position)
RCUN3	Register		Counter 3 (deviation)

Label	Kind	Position	Description
RCUN4	Register		Counter 4 (multi-purpose)
RD	Pin	4	Read signal
RDP	Register		Ramping-down point
RDR	Register		Deceleration rate
RDS	Register		S-curve section in deceleration
RENV1	Register		Environmental setting register 1 (I/O pin function)
RENV2	Register		Environmental setting register 2 (general-purpose port function)
RENV3	Register		Environmental setting register 3 (origin return and counter function)
RENV4	Register		Environmental setting register 4 (comparators 1-4 function)
RENV5	Register		Environmental setting register 5 (comparator 5 function)
RENV6	Register		Environmental setting register 6 (moving amount correction)
RENV7	Register		Environmental setting register 7 (vibration suppression function)
REST	Register		Error interrupt status
RFA	Register		Moving amount correction speed
RFH	Register		Operation speed
RFL	Register		Initial speed
RIP	Register		Center position of circular interpolation, moving amount of main axis in linear interpolation between multiple axes
RIPS	Command	FF_{HEX}	Copy RIPS register data to buffer.
RIRQ	Register		Set event interrupt factor.
RIST	Register		Event interrupt status
RLTC1	Register		Latch data of counter 1 (command position)
RLTC2	Register		Latch data of counter 2 (mechanical position)
RLTC3	Register		Latch data of counter 3 (deviation)
RLTC4	Register		Latch data of counter 4 (multi-purpose)
RMD	Register		Operation mode
RMG	Register		Speed multiplication
RMV	Register		Moving amount, target position
RPLS	Register		Number of remaining pulses for movement
RPRCP5	Command	CB_{HEX}	Copy PRCP5 data to buffer.
RPRDP	Command	$C6_{HEX}$	Copy PRDP data to buffer.
RPRDR	Command	$C4_{HEX}$	Copy PRDR data to buffer.
RPRDS	Command	CA_{HEX}	Copy PRDS data to buffer.
RPRFH	Command	$C2_{HEX}$	Copy PRFH data to buffer.
RPRFL	Command	$C1_{HEX}$	Copy PRFL data to buffer.
RPRIP	Command	$C8_{HEX}$	Copy PRIP data to buffer.
RPRMD	Command	$C7_{HEX}$	Copy PRMD data to buffer.
RPRMG	Command	$C5_{HEX}$	Copy PRMG data to buffer.
RPRMV	Command	$C0_{HEX}$	Copy PRMV data to buffer.
RPRUR	Command	$C3_{HEX}$	Copy PRUR data to buffer.
RPRUS	Command	$C9_{HEX}$	Copy PRUS data to buffer.
RRCMP1	Command	$E7_{HEX}$	Copy RCMP1 register data to buffer.
RRCMP2	Command	$E8_{HEX}$	Copy RCMP2 register data to buffer.
RRCMP3	Command	$E9_{HEX}$	Copy RCMP3 register data to buffer.
RRCMP4	Command	EA_{HEX}	Copy RCMP4 register data to buffer.
RRCMP5	Command	EB_{HEX}	Copy RCMP5 register data to buffer.
RRCUN1	Command	$E3_{HEX}$	Copy RCUN1 register data to buffer.
RRCUN2	Command	$E4_{HEX}$	Copy RCUN2 register data to buffer.
RRCUN3	Command	$E5_{HEX}$	Copy RCUN3 register data to buffer.
RRCUN4	Command	$E6_{HEX}$	Copy RCUN4 register data to buffer.
RRDP	Command	$D6_{HEX}$	Copy RDP register data to buffer.
RRDR	Command	$D4_{HEX}$	Copy RDR register data to buffer.
RRDS	Command	DA_{HEX}	Copy RDS register data to buffer.
RRENV1	Command	DC_{HEX}	Copy RENV1 register data to buffer.
RRENV2	Command	DD_{HEX}	Copy RENV2 register data to buffer.
RRENV3	Command	DE_{HEX}	Copy RENV3 register data to buffer.
RRENV4	Command	DF_{HEX}	Copy RENV4 register data to buffer.

Label	Kind	Position	Description
RRENV5	Command	E0HEX	Copy RENV5 register data to buffer.
RRENV6	Command	E1HEX	Copy RENV6 register data to buffer.
RRENV7	Command	E2HEX	Copy RENV7 register data to buffer.
RREST	Command	F2HEX	Copy REST register data to buffer.
RRFA	Command	DBHEX	Copy RFA register data to buffer.
RRFH	Command	D2HEX	Copy RFH register data to buffer.
RRFL	Command	D1HEX	Copy RFL register data to buffer.
RRIP	Command	D8HEX	Copy RIP register data to buffer.
RRIRQ	Command	ECHEX	Copy RIRQ register data to buffer.
RRIST	Command	E3HEX	Copy RIST register data to buffer.
RRLTC1	Command	EDHEX	Copy RLTC1 register data to buffer.
RRLTC2	Command	EEHEX	Copy RLTC2 register data to buffer.
RRLTC3	Command	EFHEX	Copy RLTC3 register data to buffer.
RRLTC4	Command	F0HEX	Copy RLTC4 register data to buffer.
RRMD	Command	D7HEX	Copy RMD register data to buffer.
RRMG	Command	D5HEX	Copy RMG register data to buffer.
RRMV	Command	D0HEX	Copy RMV register data to buffer.
RRPLS	Command	F4HEX	Copy RPLS register data to buffer.
RRSDC	Command	F6HEX	Copy RSDC register data to buffer.
RRSPD	Command	F5HEX	Copy RSPD register data to buffer.
RRSTS	Command	F1HEX	Copy RSTS register data to buffer.
RRUR	Command	D3HEX	Copy RUR register data to buffer.
RRUS	Command	D9HEX	Copy RUS register data to buffer.
RRDC	Register		Automatically calculated ramping-down point
RSPD	Register		EZ counter, present speed monitor
$\overline{\text{RST}}$	Pin	175	Reset signal
RSTS	Register		Extension status
RT15-0	Register bits	15-0, RENV7	Set RT time for vibration suppression function.
RUR	Register		Acceleration rate
RUS	Register		S-curve section in acceleration
SALM	Sub status bit	11, SSTSW	1 with ALM input ON
SCLR	Register bit	13, RSTS	Indicate CLR input is ON.
SCP1	Main status bit	8, MSTSW	1 when COMP1 condition is satisfied
SCP2	Main status bit	9, MSTSW	1 when COMP2 condition is satisfied
SCP3	Main status bit	10, MSTSW	1 when COMP3 condition is satisfied
SCP4	Main status bit	11, MSTSW	1 when COMP4 condition is satisfied
SCP5	Main status bit	12, MSTSW	1 when COMP5 condition is satisfied
SDIN	Register bit	15, RSTS	Indicate SD input is ON.
SDIR	Register bit	4, RSTS	Monitor operation direction (0: plus direction, 1: minus direction).
SDL	Register bit	6, RENV1	Select SD signal input logic (0: negative, 1: positive).
SDLT	Register bit	5, RENV1	Turn SD input latch function ON/OFF (0: ON, 1: OFF).
SDM	Register bit	4, RENV1	Select SD signal-initiated action (0: deceleration only, 1: stop after deceleration).
SDM1-0	Register bits	21-20, RIPS	Present quadrant of circulator interpolation
SDRM	Register bit	12, RSTS	Indicate –DR input is ON.
SDRP	Register bit	11, RSTS	Indicate +DR input is ON.
SDSTP	Command	4AHEX	Stop after deceleration
SDu	Pin	132	Ramping-down signal on U axis
SDx	Pin	36	Ramping-down signal on X axis
SDy	Pin	68	Ramping-down signal on Y axis
SDz	Pin	99	Ramping-down signal on Z axis
SED1-0	Register bits	23-22, RIPS	Last quadrant of circular interpolation
SELu	Pin	11, COMW	Select U axis.
SELx	Pin	8, COMW	Select X axis.
SELy	Pin	9, COMW	Select Y axis.
SELz	Pin	10, COMW	Select Z axis.
SEMG	Register bits	7, RSTS	Indicate $\overline{\text{CEMG}}$ input in ON.

Label	Kind	Position	Description
SEND	Main status bit	2, MSTSW	0 when started and 1 when stopped automatically
SERC	Register bit	9, RSTS	Indicate ERC output is ON.
SERR	Main status bit	3, MSTSW	1 when error interrupt occurs
SEZ	Register bit	10, RSTS	Indicate EZ input is ON.
SFC	Sub status bit	10, SSTSW	1 during constant-speed operation in progress
SFD	Sub status bit	9, SSTSW	1 during deceleration in progress
SFU	Sub status bit	8, SSTSW	1 during acceleration in progress
SINP	Register bit	16, RSTS	Indicate INP input is ON.
SINT	Main status bit	4, MSTSW	1 when event interrupt occurs
SLTC	Register bit	14, RSTS	Indicate LTC input is ON.
SMEL	Sub statis bit	13, SSTSW	1 when –EL input is ON
SMOV	Main status bit	1, MSTSW	1 during motor operation
SORG	Sub status bit	14, SSTSW	1 when ORG input is ON.
SPCS	Register bit	8, RSTS	Indicate PCS input is ON.
SPDF	Main status bit	15, MSTSW	1 when preregister for comparator 5 is full
SPEL	Sub status bit	12, SSTSW	1 when +EL input is ON
SPRF	Main status bit	14, MSTSW	1 when preregisters for the next $\overline{\text{operation}}$ are full
SPSTA	Command	2A$_{HEX}$	Same processing as initiated by CSTA signal ON, but for that axis only
SRCH	Register bit	2, RENV3	Origin search
SRST	Command	04$_{HEX}$	Software reset
SRUN	Main status bit	0, MSTSW	1 when started
SSC1-0	Mainstatus bits	7-6, MSTSW	Sequence code
SSCM	Main status bit	0, MSTSW	Start command already written
SSD	Sub status bit	15, SSTSW	1 when $\overline{\text{SD}}$ input is ON (latch signal)
SSTA	Register bit	5, RSTS	Indicate $\overline{\text{CSTA}}$ input is ON.
SSTP	Register bit	6, RSTS	Indicate CSTP input is ON.
SSTSB	Byte map	3 with Z80	Read sub status.
SSTSW	Word map	2 with 8086	Read sub status and general-purpose I/O port status.
STAD	Command	52$_{HEX}$	Start varied-speed operation-1 (FH rate – deceleration before stop)
SAFH	Command	51$_{HEX}$	Start constant-speed operation at FH rate.
STAFL	Command	50$_{HEX}$	Start constant-speed operation at FL rate.
STAM	Register bit	18, RENV1	Select $\overline{\text{CSTA}}$ signal mode (0: level trigger, 1: edge trigger).
STAON	Command	28$_{HEX}$	Act for PCS input.
STAUD	Command	53$_{HEX}$	Start varied-speed operation-2 (acceleration – FH rate – deceleration before stop)
STOP	Command	49$_{HEX}$	Stop immediately.
STPM	Register bit	19, RENV1	Select $\overline{\text{CSTP}}$-initiated stop mode (0: immediate stop, 1: stop after deceleration).
SYI1-0	Register bits	21-20, RENV5	Select the axis to input internal synchronization signal.
SYO3-0	Register bits	19-16, RENV5	Select the timing to output internal synchronization signal.
WPRCP5	Command	8B$_{HEX}$	Write data from buffer to PRCP5.
WPRDP	Command	86$_{HEX}$	Write data from buffer to PRDP.
WPRDR	Command	84$_{HEX}$	Write data from buffer to PRDR.
WPRDS	Command	8A$_{HEX}$	Write data from buffer to PRDS.
WPRFH	Command	82$_{HEX}$	Write data from buffer to PRHF.
WPRFL	Command	81$_{HEX}$	Write data from buffer to PRFL.
WPRIP	Command	88$_{HEX}$	Write data from buffer to PRIP.
WPRMD	Command	87$_{HEX}$	Write data from buffer to PRMD.
WPRMG	Command	85$_{HEX}$	Write data from buffer to PRMG.
WPRMV	Command	80$_{HEX}$	Write data from buffer to PRMV.
WPRUR	Command	83$_{HEX}$	Write data from buffer to PRUR.
WPRUS	Command	89$_{HEX}$	Write data from buffer to PRUS.
$\overline{\text{WR}}$	Pin	5	Write signal
WRCMP1	Command	A7$_{HEX}$	Write data from buffer to RCMP1 register.
WRCMP2	Command	A8$_{HEX}$	Write data from buffer to RCMP2 register.
WRCMP3	Command	A9$_{HEX}$	Write data from buffer to RCMP3 register.
WRCMP4	Command	AA$_{HEX}$	Write data from buffer to RCMP4 register.
WRCMP5	Command	AB$_{HEX}$	Write data from buffer to RCMP5 register.

Label	Kind	Position	Description
WRCUN1	Command	$A3_{HEX}$	Write data from buffer to RCUN1 register.
WRCUN2	Command	$A4_{HEX}$	Write data from buffer to RCUN2 register.
WRCUN3	Command	$A5_{HEX}$	Write data from buffer to RCUN3 register.
WRCUN4	Command	$A6_{HEX}$	Write data from buffer to RCUN4 register.
WRDP	Command	96_{HEX}	Write data from buffer to RDP register.
WRDR	Command	94_{HEX}	Write data from buffer to RDR register.
WRDS	Command	$9A_{HEX}$	Write data from buffer to RDS register.
WRENV1	Command	$9C_{HEX}$	Write data from buffer to RENV1 register.
WRENV2	Command	$9D_{HEX}$	Write data from buffer to RENV2 register.
WREND3	Command	$9E_{HEX}$	Write data from buffer to RENV3 register.
WRENV4	Command	$9F_{HEX}$	Write data from buffer to RENV4 register.
WRENV5	Command	$A0_{HEX}$	Write data from buffer to RENV5 register.
WRENV6	Command	$A1_{HEX}$	Write data from buffer to RENV6 register.
WRENV7	Command	$A2_{HEX}$	Write data from buffer to RENV7 register.
WRFA	Command	$9B_{HEX}$	Write data from buffer to RFA register.
WRFH	Command	92_{HEX}	Write data from buffer to RFH register.
WRFL	Command	91_{HEX}	Write data from buffer to RFL register.
WRIP	Command	98_{HEX}	Write data from buffer to RIP register.
WRIRQ	Command	AC_{HEX}	Write data from buffer to RIRQ register.
WRMD	Command	97_{HEX}	Write data from buffer to RMD register.
WRMG	Command	95_{HEX}	Write data from buffer to RMG register.
WRMV	Command	90_{HEX}	Write data from buffer to RMV register.
$\overline{WRQ}$	Pin	13	Wait request signal
WRUR	Command	93_{HEX}	Write data from buffer to RUR register.
WRUS	Command	99_{HEX}	Write data from buffer to RUS register.

NPM NIPPON PULSE MOTOR CO., LTD.
No. 16-13, 2-chome, Hongo, Bunkyo-ku, Tokyo 113-0033, Japan
Phone: 81-3-3813-8841 Fax: 81-3-3813-2940
E-mail: int-l@npm.co.jp URL: http://www.pulsemotor.com