OV7640/OV7141 VGA CameraChip™ Implementation Guide

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Revision Number	Revision
1.0	Initial release
1.1	Added hex address references and disclaimer page.
1.2	Added minimum and maximum values for registers responsible for maximum output window size

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1 Introduction

This general application note is provided as a brief overview of the settings required for programming the OV7640/OV7141 CAMERACHIP™. The Implementation Guide supplies the design engineer with quick-start tips for successful design solutions.

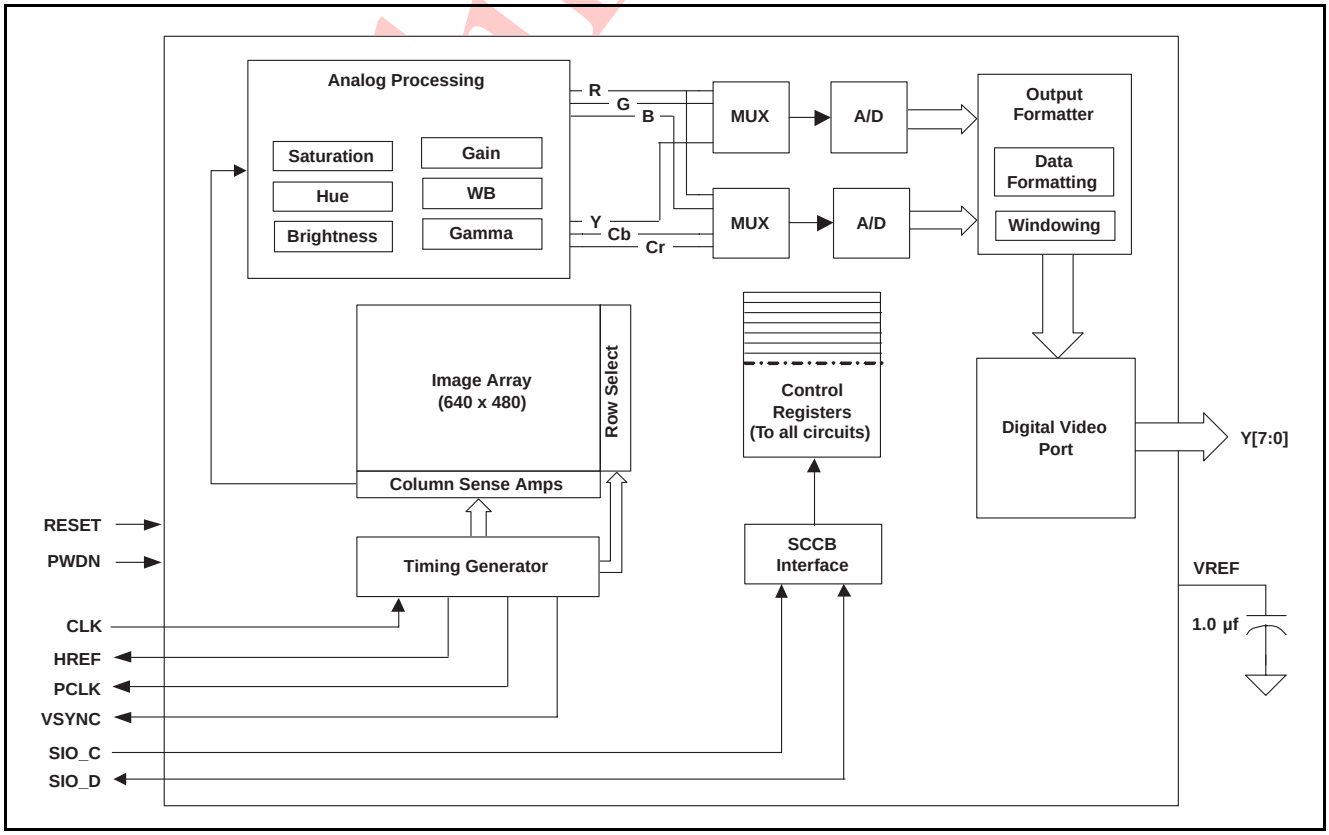
The *OV7640/OV7141 Datasheet* provides complete information on the features, pin descriptions, and registers of the OV7640/OV7141. The Implementation Guide is intended to complement the *OV7640/OV7141 Datasheet* with considerations for PCB layout, register configurations, and timing parameters for rapid product design and deployment.

1.1 Function Description

Figure 1-1 shows the functional block diagram of the OV7640/OV7141 image sensor. The OV7640/OV7141 includes:

- Image Sensor Array (640 x 480 resolution)
- Timing Generator
- Analog Processing Block
- A/D Converters
- Output Formatter
- Digital Video Port
- SCCB Interface

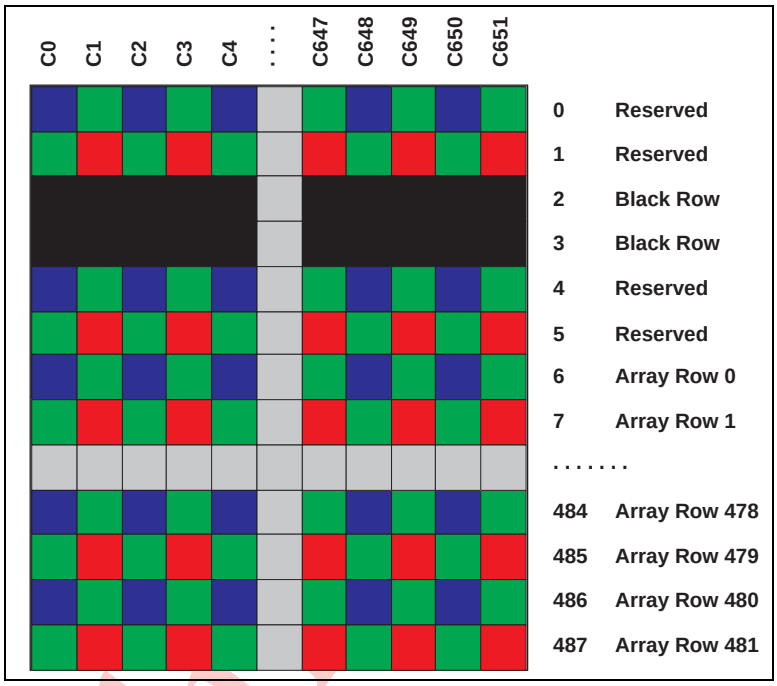
Figure 1-1 OV7640/OV7141 Functional Block Diagram



2 Image Sensor Array

The OV7640/OV7141 family of CAMERACHIPS has an active image array size of 640 columns by 480 rows (307,200 pixels). However, the full array contains 652 columns and 488 rows with the extra 6 rows used for black-level calibration (Optical Black) and color interpolation information (see Figure 2-1). However, the maximum output valid image window size is 652 columns by 482 rows.

Figure 2-1 Pixel Array



As shown in Figure 2-1, the pixel cells themselves are identical, but have RGB color filters arranged in a line-alternating BG/GR ***Bayer Pattern*** (not present on the OV7140). The final Y[7:0] image uses this filter pattern to interpolate each pixel's BG or GR color from the light striking the cell directly, as well as from the light striking the surrounding cells.

Note that the actual output of the array is either 'Raw RGB', in which the Bayer Filter pattern is shifted out row-by-row, or 'RGB', in which row pairs are shifted out for interpolation in the Analog Processing Block (APB) (Actual RGB → YUV/YCbCr conversion is handled by the APB's Color Matrix).

With the OV7140 selected, B&W array scanning is treated as 'Raw RGB' (but with no color filters). In addition, when the output is set to the YUV format, the 'Y' channel (Luminance) will be correctly formatted to output 8-bit B&W. See Table 2-1.

Table 2-1. OV7640/OV7141 Output Formats

Device	Format	Output	Register
OV7141	B&W	8 bits (Y Channel)	COMH[6] (0x28)
OV7640	Raw RGB	8 bits (Bayer Filter Color)	COMA[3] (0x12), COMH[7] (0x28)
	RGB, YUV, YCbCr	8 bits, 4:2:2 (Interpolated Color)	COMH[6] (0x28)

2.1 VGA Format

The OV7640/OV7141 CAMERACHIP VGA configuration assumes device operation at 30 fps using a 24 MHz crystal and configured such that all auto functions are disabled. Adjust registers GAIN (0x00), BLUE (0x01), RED (0x02), and AECH (0x10) for gain, white balance, and exposure. Adjust the following registers for their control functions, as noted in Table 2-2.

Table 2-2. VGA Register Settings

Register	Address	Value	Description
COMA	0x12	0x80	Reset register
COMB	0x13	0x00	Disable auto function
CLKRC	0x11	0x00	30 fps VGA
ADRC	0x69	0x04	Adjust A/D range

2.2 QVGA Format

The OV7640/OV7141 CAMERACHIP QVGA configuration assumes device operation at 30 fps or 60 fps using a 24 MHz crystal and configured such that all auto functions are disabled. Adjust registers GAIN (0x00), BLUE (0x01), RED (0x02), and AECH (0x10) for gain, white balance, and exposure. Adjust the following registers for their control functions, as noted in Table 2-3.

Table 2-3. QVGA Register Settings

Register	Address	Value	Description
COMA	0x12	0x80	Reset register
COMB	0x13	0x00	Disable auto function
CLKRC	0x11	0x00	60 fps QVGA
COMC	0x14	0x20	QVGA format
ADRC	0x69	0x04	Adjust A/D range
COMH	0x28	0x00	Interlace mode for QVGA

Note: Refer to Appendix A, "Reference SCCB Settings for factory-recommended SCCB settings.

3 Timing Generator

In general, the timing generator controls the following functions:

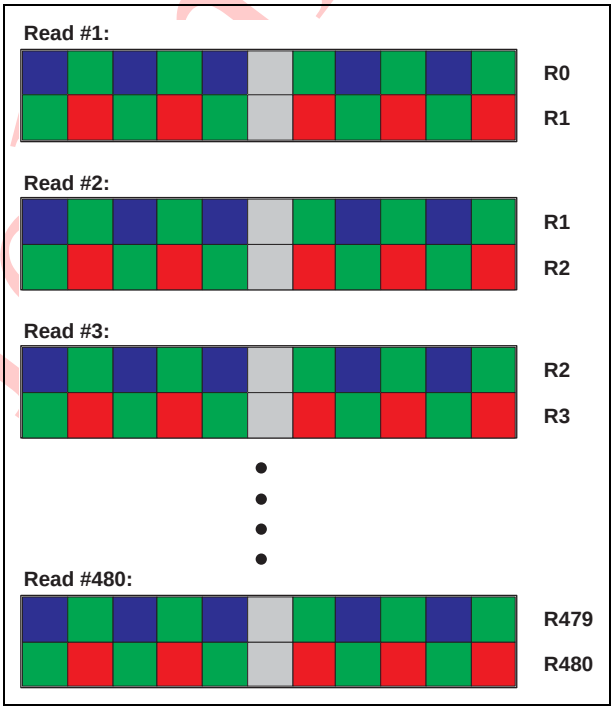
- Array Control and Frame Generation (VGA and QVGA outputs)
- Internal timing signal generation and distribution
- Frame Rate Timing
- Exposure Control
- External timing outputs (VSYNC, HREF and PCLK)

3.1 Array Control and Frame Generation

3.1.1 Frame Generation (VGA)

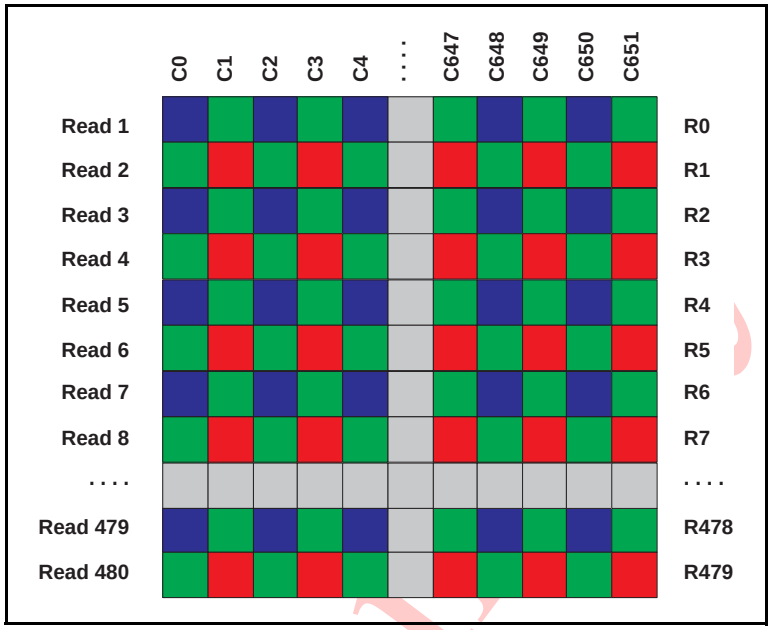
VGA frame generation (see Figure 3-1) uses Progressive scanning of the array in which rows are sequentially read and transferred out to the APB. However, the APB actually receives two rows simultaneously, the current row and the current 'last row' (stored in a 'Last Row' register, not shown). This means that the APB receives pairs of adjacent rows, (R_A/R_{A+1}), (R_{A+1}/R_{A+2}), (R_{A+2}/R_{A+3}), (R_{A+3}/R_{A+4}), etc. (every row is received by the APB twice) for accurate color interpolation.

Figure 3-1 VGA Frame Generation



Note that the ‘Raw RGB’ output (see Figure 3-2) preserves the Bayer Filter pattern, so odd rows follow the R0 pattern (GB) and even rows follow the R1 pattern (GR).

Figure 3-2 VGA Raw RGB Output



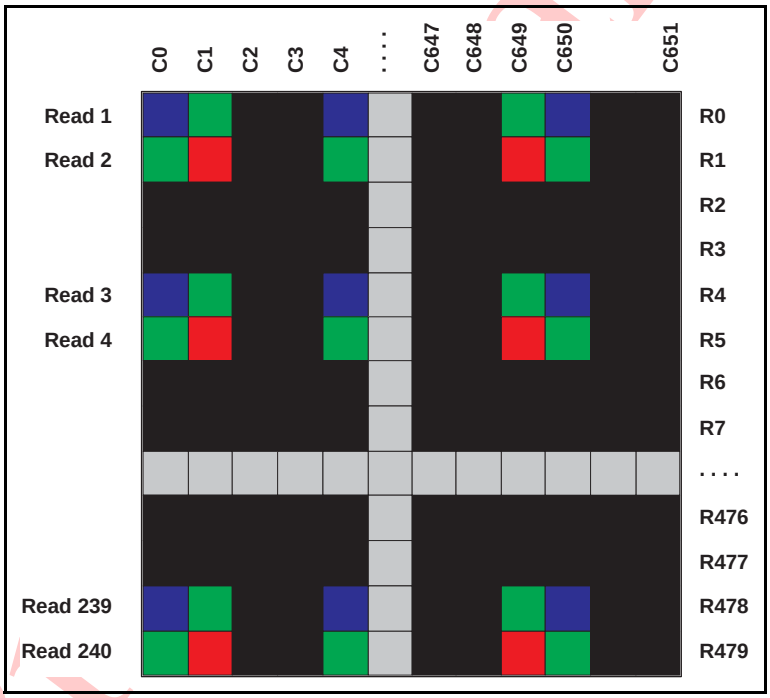
3.1.2 Frame Generation - QVGA (Sub-Sampling)

Although the default VGA resolution for the OV7640/OV7141 device is 640 x 480 pixels, the CAMERACHIP can be programmed to output in QVGA (Quarter VGA, 320 x 240 pixels) resolution for applications where higher resolution image capture is not required. There are two sub-sampling methods which can be chosen, 'Raw RGB' or RGB (which can be converted to YUV or YCbCr in the APB).

3.1.2.1 QVGA – Raw RGB Output

The sub-sampled frame skips every other two rows (R0/R1, R4/R5, R8/R9, …) and every other two columns (C0/C1, C4/C5, C8/C9, …) as shown in Figure 3-3. This method is used for Raw RGB only since YUV and RGB uses the method described in Section 3.1.2.2 which produces better quality.

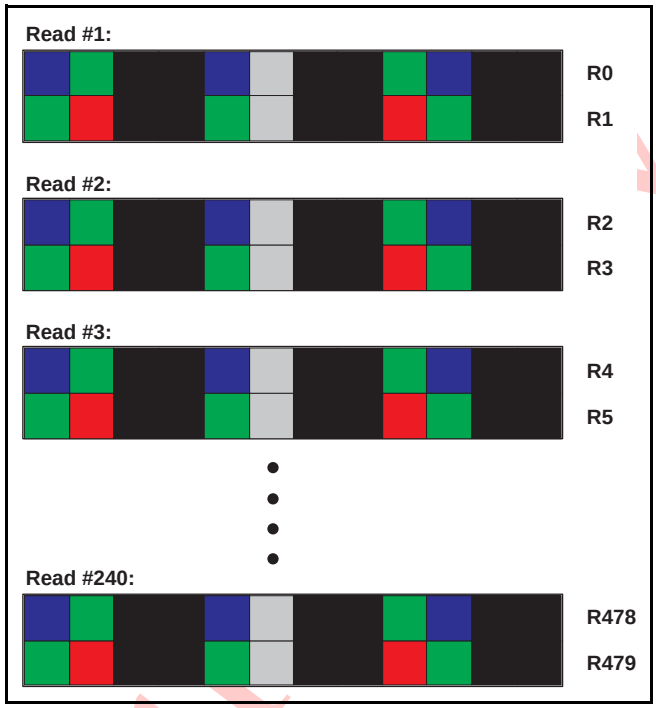
Figure 3-3 Progressive Scan



3.1.2.2 QVGA – RGB/YUV/YCbCr Output

This output uses row pairs which only contain each row once, and skips every other two columns as shown in Figure 3-4. This method uses half of the VGA pixels to generate QVGA format, producing better quality as a result.

Figure 3-4 Interlaced Scan



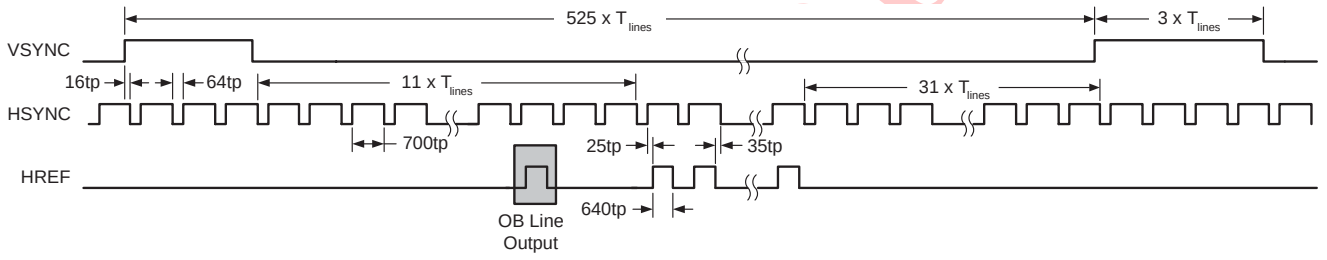
3.2 Sync Signal Selection

OV7640/OV7141 CAMERACHIP supplies two output sync signals: VSYNC and HREF. The vertical sync (VSYNC) signal is output on pin 9. The horizontal reference signal (HREF) is output on pin 10. The HSYNC signal is available on pin 10 when register COML[5] (0x71) value is set to "1".

The VSYNC and HSYNC signals are continuous. The HREF signal is only valid when there is output data. If there is no output data, the HREF signal will remain at either high or low, depending on the polarity selection. The VSYNC/HSYNC polarity selection is controlled by register CLKRC[7:6] (0x11).

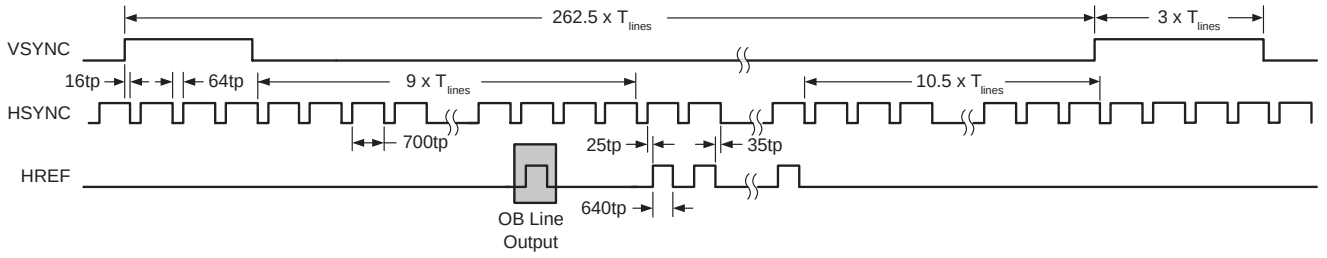
Figure 3-5 shows the timing chart of the three sync signals for VGA and QVGA implementation.

Figure 3-5 Sync Timing Diagram



NOTES: YUV/RGB: Tp = 2 x Tpclk
Raw data: Tp = Tpclk
QVGA Raw data output frame timing is the same as VGA YUV/RGB format but Tp = Tpclk/2 and data will be valid 2 lines for every 4 lines

VGA YUV/RGB Frame Timing



NOTE: YUV/RGB: Tp = Tpclk

QVGA YUV/RGB Frame Timing

3.3 Frame Rate Timing

The OV7640/OV7141 offers two methods of frame rate adjustment:

- Clock Prescalar (Timing Generator)
- Dummy Pixel Row Adjustment (Output Formatter)

3.3.1 Clock Prescalar (Timing Generator)

By changing the system clock divide ratio using the CLKRC[5:0] (0x11) register, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 ... 1/64 of the input clock rate. The internal clock frequency, $f_{INT\ CLK}$, can be expressed as follows:

$f_{INT\ CLK} = f_{CLK} \div (CLKRC[5:0]\ (0x11) + 1)$
$t_{INT\ CLK} = t_{CLK} \times (CLKRC[5:0]\ (0x11) + 1)$

Table 3-1. PCLK Output Frequency

Resolution	Format	f_{PCLK}
VGA	RGB/YUV/CbCr	$f_{INT\ CLK}$
	Raw RGB	$f_{INT\ CLK} \div 2$
QVGA	RGB/YUV/CbCr	$f_{INT\ CLK} \div 2$
	Raw RGB	$f_{INT\ CLK} \div 4$

3.3.2 Dummy Pixel Row Adjustment (Output Formatter)

By inserting dummy pixels in each row's output or by inserting dummy lines in each frame output, the frame rate can be changed while leaving the pixel rate unchanged (see Section 7.2.2).

3.4 Exposure Control

The OV7640/OV7141 CAMERACHIP supports both automatic and manual exposure control modes. The exposure time is defined as the interval from the cell precharge to the end of the photo-induced current measurement and can be controlled manually or by using the AEC function. This exposure control uses a 'rolling' shutter as exposure time is set on a row-by-row basis rather than on a frame-by-frame basis.

Exposure Time interval is defined as follows:

$t_{EXPOSURE} = 2 \times (764 \times t_{INT\ CLK}) \times AEC[9:0]$ where AEC[9:0] is defined as:

AEC[9:0] = MSB + LSB = AECH[7:0] (0x10) + COMO[1:0] (0x76)

Each bit in AEC[9:0] = t_{ROW} interval = $2 \times (764 \times t_{INT\ CLK})$

Note that both the AEC and AGC functions are interactive so registers and functions may be common to both. Also, in general, the AEC is the primary control and will be adjusted before the AGC (the AGC acts to adjust and center the AEC).

The algorithm used for the electronic exposure control is based on brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the AEC white/black ratio may be adjusted to suit the needs of the application.

The minimum exposure time is controlled by SCCB register bit FACT[0] (0x1F). When FACT[0] (0x1F) is low, the minimum time for exposure is 1 line. When FACT[0] (0x1F) is high, the minimum exposure time is about 80 pixels. The AEC time count when exposure time is under one line is stored in AECL1[7:0] (0x7C).

3.4.1 Digital Exposure Control

- Each frame has digitally-generated averages (YUV or RGB) which are used to set the Control Zone limits.
- Exposure Time, Control Zone Limits, and Channel Average registers are updated automatically.
- In this mode, the user must select the AEC method using register bit FRARH[0] (0x2A) and enable the digital averaging function using register bit COME[6] (0x20).

3.4.2 Analog Exposure Control

- Based on their analog levels, each frame is evaluated for "bright" and "dark" pixels outside of the 'stable region' which are used to set the upper and lower Control Zone limits.
- Exposure Time is updated automatically.
- In this mode, the user must select the correct feedback channel for the selected output.

3.4.3 Exposure Control Methods

Table 3-2 lists the registers used for Exposure Control.

Table 3-2. Exposure Control Registers

Function	Register	Address
AEC Method Select	FRARH[0]	0x2A
Analog AEC – Feedback Channel Select	SPCC[7]	0x61
Digital Averaging Enable	COME[6]	0x20
Digital Y/G Channel Average	AVGY[7:0]	0x7E
Digital R/V Channel Average	AVGR[7:0]	0x7F
Digital B/U Channel Average	AVGB[7:0]	0x80

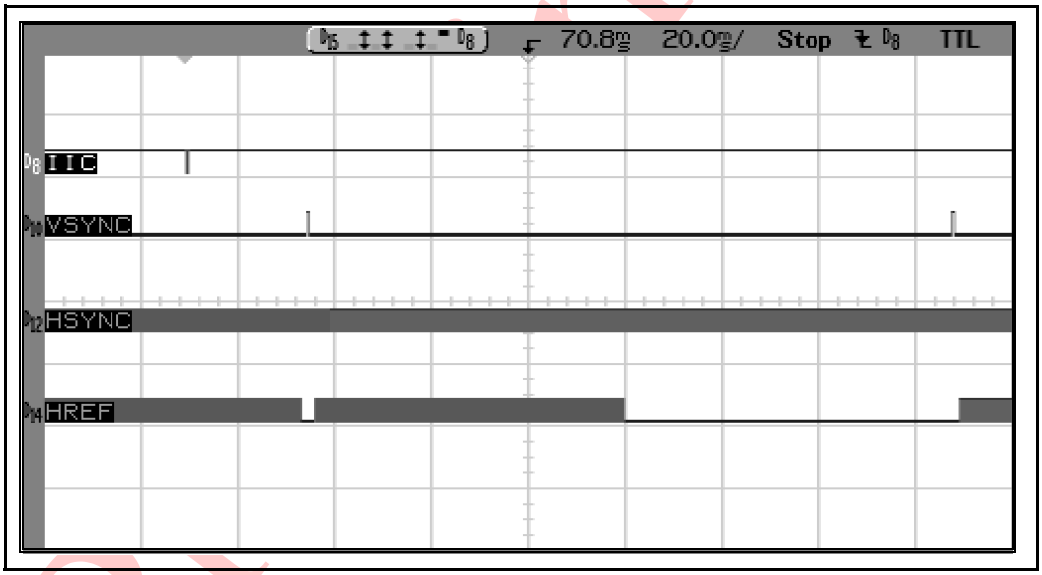
3.4.3.1 Manual Exposure Control Mode

The manual exposure control mode allows for the companion backend system ASIC to control the OV7640/OV7141 image exposure. The companion back-end chip may write exposure values to CAMERACHIP register AECH (0x10) and COMO[1:0] (0x76) according to its corresponding Auto-Exposure Control (AEC) algorithm.

The minimum allowable exposure value is 1 line. Exposure modes of less than 1 line may be used in special cases but may suffer from a little more noise. The LSB signifies the 1 line exposure time. The exposure value data is 10-bits in length, AECH[7:0] (0x10), COMO[1:0] (0x76).

The maximum exposure increase steps are 20 lines for VGA mode and 9 lines for QVGA mode. Exceeding these values will result in the appearance of an over-exposure frame. Setting the register COMN[3] (0x75) to a value of "1" will eliminate this over-exposure frame by eliminating the HREF signal output. This provision also allows for the companion backend system ASIC to use the VSYNC as a frame data reset to eliminate the undesired frame by register COMK[2] (0x70). Refer to Figure 3-6 for details.

Figure 3-6 Manual Exposure Frame Drop Timing Diagram



Rolling Horizontal Band Elimination in Manual Mode

The OV7640/OV7141 supports a rolling shutter exposure mode and requires special exposure values when used in 50/60 Hz florescent lighting conditions to eliminate rolling horizontal band. The minimum exposure value is 1/120 second for 60 Hz and 1/100 second for 50 Hz lighting conditions. The following steps outline how to calculate the proper exposure value at 50 Hz/60 Hz light conditions:

1. Calculate the CAMERACHIP Minimum Exposure Line (MEL):
   Line period is Tline = K × Tpclk = K/fpclk, while K is PCLK number in one line, Tpclk is PCLK period (sec) and fpclk is PCLK frequency (Hz). Tpclk = 1/fpclk
   For 60 Hz lighting: MEL = (1/120)/Tline = 1/(120 × K × Tpclk) = fpclk/(120 × K)
   For 50 Hz lighting: MEL = (1/100)/Tline = 1/(100 × K × Tpclk) = fpclk/(100 × K)

2. Set the CAMERACHIP Available Exposure Line (AEL):
   Suppose N is integer, N = 1,2,3…
   Available exposure line are: AEL = N × MEL. While AEL ≤ 525 (VGA) and 262.5 (QVGA)
3. Convert AEL to binary, and then send 2 LSBs hex number to register COMO (0x76) and 8 MSBs hex number to register AECH (0x10).

Maximum Exposure Line Limitation

OV7640/OV7141 maximum exposure line value are:

- VGA - 525 lines
  Register setting: 0x20D = {AECH[7:0] (0x10), COMO[1:0] (0x76)}, meaning AECH (0x10) = 0x83, COMO[1:0] (0x76) = 0x01
- QVGA - 262.5 lines
  Register setting: 0x106 = {AECH[7:0] (0x10), COMO[1:0] (0x76)}, meaning AECH (0x10) = 0x41, COMO[1:0] (0x76) = 0x02

3.4.3.2 Automatic Exposure Control Mode (AEC)

The AEC function allows for the CAMERACHIP to adjust the exposure without external command or control. The registers AECH (0x10) and COMO[1:0] (0x76) are adjusted by the CAMERACHIP internal controls and cannot be overwritten by an external device.

Auto-Exposure Control Enable Bit

To enable the AEC function, set register COMB[0] (0x13) to "1". The AEC controls brightness using registers AEW (0x24) and AEB (0x25). The register AEW (0x24) value indicates the high threshold value and register AEB (0x25) indicates the low threshold value. When the target image luminance average value (YAVG) is within the specified range of values, the AEC is not required and is therefore disabled. When YAVG, is greater than the value in register AEW (0x24), the AEC will decrease the image exposure. When YAVG is less than the value in register AEB (0x25), the AEC will increase the image exposure. Accordingly, the value in register AEW (0x24) should be greater than the value in register AEB (0x25). The difference between the AEW (0x24) and AEB (0x25) register values controls the image stability and brightness. The recommended values for register AEW (0x24) and AEB (0x25) are: AEW (0x24) = 0x90; AEB (0x25) = 0x80.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers AEW (0x24) and AEB (0x25). AEC set to normal mode will allow for single-step increase or decrease in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increase or decrease in the image exposure to maintain the specified range. A value of "0" in register COMD[2] (0x15) will result in normal speed operation and a "1" will result in fast speed operation.

Register AEGR (0x77) controls the fast AEC range. If the target image YAVG is greater than AEGR[7:4] (0x77) × 16, AEC will decrease by 2. If YAVG is less than AEGR[3:0] (0x77) × 16, AEC will increase by 2.

Rolling Horizontal Band Elimination in Auto Mode

OV7640/OV7141 also provides rolling horizontal band eliminate function in auto exposure mode. Default function is designed to work with a 24 MHz system clock. To enable this function, set register COMJ[2] (0x2D).

Note that when OV7640/OV7141 uses another frequency system clock, the line period should be adjusted by adding some dummy pixels (by setting register FRARH (0x2A) and FRARL (0x2B) to meet the horizontal band eliminate condition.

For example: when the system clock is 27 MHz, dummy pixels will be 764 × (27/24 -1) = 96 = 0x60. So set register FRARH[7] (0x2A) to "1" and FRARL (0x2B) to 0x60.

AEC Convergence Limits

Table 3-2 lists the registers used for setting AEC convergence limits.

Table 3-3. AEC Convergence Limits

Function	Register	Address
Control Zone – Upper Limit MSB	AEGR[7:4]	0x77
Control Zone – Lower Limit MSB	AEGR[3:0]	0x77
Stable Operating Region – Upper Limit	AEW[7:0]	0x24
Stable Operating Region – Lower Limit	AEB[7:0]	0x25
Step Size Limit	COMD[3]	0x15

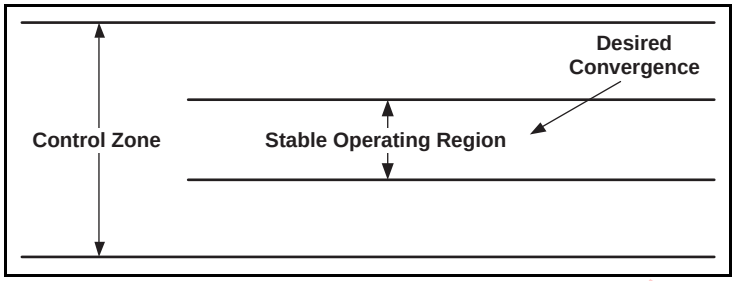
As shown in Figure 3-7, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer Control Zone, which defines the convergence step size change as follows:

- Outside Control Zone
  Step Size: 2 × (AEC[9:0])
  t_{STEP}: t_{ROW} × (2 × AEC[9:0])
- Inside Control Zone
  Step Size: 2 × (AEC[9:0]) ÷ 16
  t_{STEP}: t_{ROW} × (AEC[9:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

The Step Limit register acts to create a "middle ground" by limiting the maximum step size to 32 rows (delay time = t_{ROW} × 32).

Figure 3-7 Desired Convergence



Control Zone Upper Limit: AEGR[7:4] (0x77) (MSB) + 0000 (LSB)
Control Zone Lower Limit: AEGR[3:0] (0x77) (MSB) + 0000 (LSB)
Stable Operating Region Upper Limit: AEW[7:0] (0x24)
Stable Operating Region Lower Limit: AEB[7:0] (0x25)

AEC Options

Table 3-4 shows lists the registers used for various AEC options.

Table 3-4. AEC Options

Function	Register	Address
Center-Based Reference Area Enable	FRARH[1]	0x2A
Partial Row Exposure Enable	FACT[0]	0x1F
Partial Row Exposure – Bits Sampled	AECL1[7:0]	0x7C
Flicker Filter Enable	COMJ[2]	0x2D

Center-Based Reference Area Enable

Enabling this option changes the AEC/AGC exposure reference from the whole image to the center of the array (one quarter of the whole image is counted).

Partial Row Exposure

This allows exposure time < 1 row for very bright ambient lighting (both manual and AEC modes).

Flicker Filter

A banding filter to filter out banding caused by 50/60 Hz fluorescent lighting.

3.5 Strobe Flash Control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV7640/OV7141 supports rolling shutter exposure mode.

To avoid the need for a mechanical shutter, the OV7640/OV7141 should be set to rolling shutter mode. When the rolling shutter mode is enabled and the image requires strobe flash illumination, the strobe timing must be limited. Timing diagrams for strobe flash timing are shown in Figure 3-8 and Figure 3-9.

Figure 3-8 VGA Strobe Flash Timing Diagram

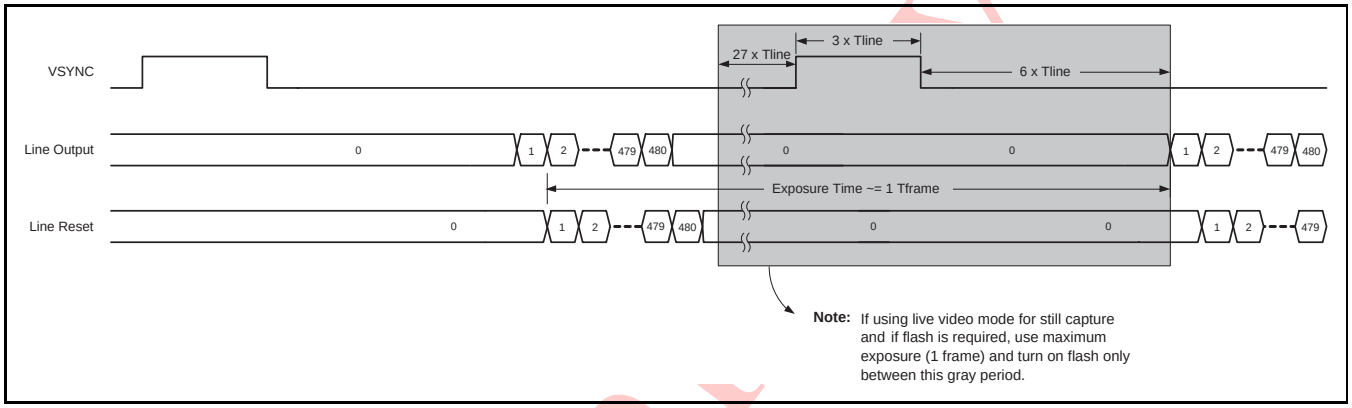
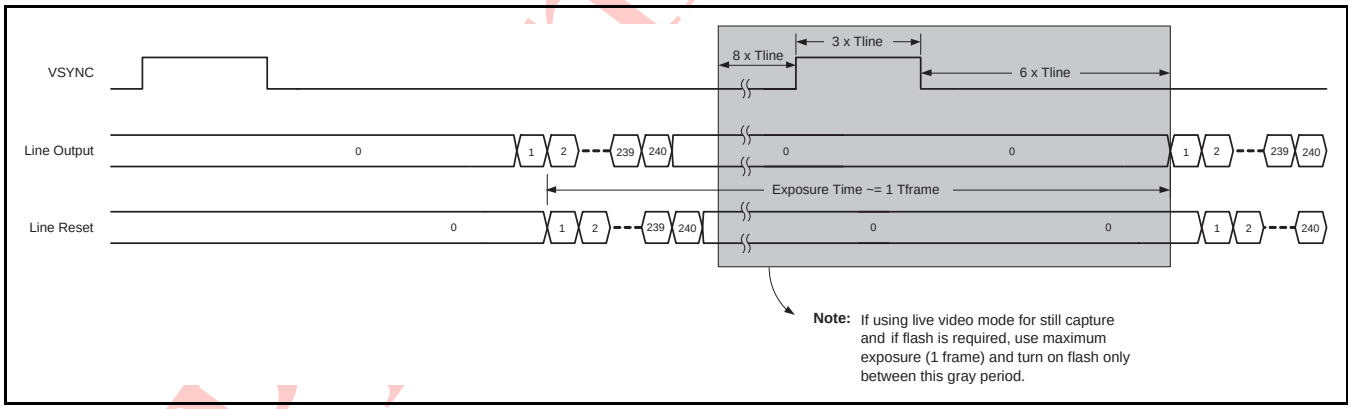


Figure 3-9 QVGA Strobe Flash Timing Diagram



3.6 RGB Raw Data Output Sequence

Review the *OV7640/OV7141 Datasheet* for complete details regarding the RGB raw data output. Register COMD[6] (0x15) determines whether the data is valid based on either the rising or falling edge of PCLK, depending on the PCLK polarity selection. The data receiver should latch upon indication of valid data in time with the rising/falling edge of PCLK. Setting register COMD[6] (0x15) to "1" indicates data is valid on the rising edge of PCLK. Setting register COMD[6] (0x15) to "0" indicates data is valid on the falling edge of PCLK. Depending on this polarity selection, if the HREF signal is high, the data is valid. If the HREF signal is low, the data is not valid.

When using the HSYNC signal, adjust registers COML (0x71), HSDYR (0x72), and HSDYF (0x73) to adjust the HSYNC signal rising and falling edges to obtain valid data. To obtain the HSYNC and HREF width, set registers HSTART (0x17), HSTOP (0x18), HSDYR (0x72), and HSDYF (0x73) to HSYNCR/HSYNCF[9:0], respectively. To use the default HREF settings, refer to Appendix A, “Reference SCCB Settings for programming registers COML (0x71), HSDYR (0x72), and HSDYF (0x73).

4 Analog Processing Block

This block performs all analog image functions including Automatic Gain Control (AGC), Automatic White Balance (AWB), and other image manipulation functions

4.1 Gain Control

The OV7640/OV7141 CAMERACHIP provides support for both AGC and manual gain control modes.

4.1.1 Manual Gain Control

The manual gain control mode allows for the companion backend system ASIC to control the OV7640/OV7141 gain value. The companion backend chip may write gain control values to the CAMERACHIP RGB raw data register GAIN (0x00) according to its corresponding AGC algorithm. The complete definition for this register is available in Appendix A, “Reference SCCB Settings. An example of the total gain to control bit correlation is shown in Table 4-1.

Table 4-1. Total Gain to Control Bit Correlation

Register GAIN (0x00)	Gain	dB
000000	1	0
000001	1 + 1/16	.375
000010	1 + 2/16	.75
000011	1 + 3/16	1.125
000100	1 + 4/16	1.5
000101	1 + 5/16	1.875
000110	1 + 6/16	2.25
000111	1 + 7/16	2.625
001000	1 + 8/16	3
001001	1 + 9/16	3.375
001010	1 + 10/16	3.75
001011	1 + 11/16	4.125
001100	1 + 12/16	4.5
001101	1 + 13/16	4.875
001110	1 + 14/16	5.25
001111	1 + 15/16	5.625
010000	2 × (1 + 0/16)	6
110000	4 × (1 + 0/16)	12
111111	4 × (1 + 15/16)	~18

Note: To achieve the best image quality, using a 1x gain at most for the highest S/N ratio is recommended. When operating in low-light condition, use the strobe flash. The information contained in Table 4-1 is based on a 1x gain.

4.1.2 Automatic Gain Control (AGC)

The AGC function allows the CAMERACHIP to adjust image brightness and target level gain without external command or control. Register setting COMB[1] (0x13) enables AGC. The target level control registers are AEW (0x24) and AEB (0x25). Refer to Section 3.4.3.2 for additional details regarding the target level controls. When operating in fast AEC/AGC mode, use register AEGR[7:0] (0x77) to set the conditions for fast AGC. Table 4-2 shows the general controls for the AGC.

Table 4-2. AGC General Controls

Function	Register	Address
AGC Enable	COMB[1]	0x13
Gain Setting	GAIN[5:0]	0x00
1.5x Multiplier (Pre-amplifier) Enable	SPCB[7]	0x60
Maximum Gain Select	COMM[6:5]	0x74
Feedback Channel Select[a]	SPCC[7]	0x61

a. The user must select the correct feedback channel for the output selected (set in the AEC section)

The analog pixel data first arrives at the AGC amplifier which can be automatically controlled by the AGC circuit or manually programmed by the user (see Table 4-3). In both cases, the gain control is active but when AGC = OFF, the gain setting is generated by the user and not updated by the AGC circuit.

Table 4-3. AGC Enable Bit

COMB[1] (0x13)	AGC Status	GAIN[5:0] (0x00)
1	ON	Controlled by AGC
0	OFF	Controlled by user

The two-stage gain circuit consists of an optional 1.5x (3 dB) multiplier (pre-amplifier) followed by the AGC-controlled amplifier. The maximum gain possible (21 dB) is determined by the maximum gain selected multiplied by the 1.5x pre-gain multiplier (if enabled).

The AGC operation is identical to the AEC (see Section 3.4.3.2). Table 4-4 lists the registers used to set the AGC convergence limits.

Table 4-4. AGC Convergence Limits

Function	Register	Address
Control Zone – Upper Limit MSB	AEGR[7:4]	0x77
Control Zone – Lower Limit MSB	AEGR[3:0]	0x77
Stable Operating Region – Upper Limit	AEW[7:0]	0x24
Stable Operating Region – Lower Limit	AEB[7:0]	0x25
Step Size Limit	COMD[3]	0x15

4.1.2.1 Center-Based Reference Area Enable

Enabling this option changes the AEC/AGC exposure reference from the whole image to the center of the array (set in the AEC section - see Section 3.4.3.2). The Center-based Reference Area Enabled is set at register FRARH[1] (0x2A).

4.2 White Balance Control

The OV7640/OV7141 CAMERACHIP supports auto/manual white balance control. After the initial pixel level adjustment, the Red and Blue channel gains are optimized to the Green channel luminance to set the white balance. This white balance is either automatically-controlled by the AWB circuit or manually-controlled by the user. The following describes these AWB modes:

- Full user control – RED/BLUE channels are set manually
- Full AWB control – RED/BLUE are channels are under AWB control
- Full AWB control – RED/BLUE are channels are under AWB control but initial values are set by the user for faster performance

These AWB modes can be controlled by the registers shown in Table 4-5.

Table 4-5. AWB Operating Modes

AWB Enable (COMA[2] 0x12)	Manual Enable (COME[2] 0x20)	AWB Status	RED[7:0] (0x02) / BLUE[7:0] (0x01) Control
0	X	OFF	By User
1	0	ON	By AWB
1	1	ON	By AWB (initial value set by user)

4.2.1 Automatic White Balance Control

In general, the white balance is done in two steps, by adjusting the Red/Blue gain to match the Green channel luminance and by controlling the AWB response time.

The Red/Blue gain is first set to a fixed 'pre-AWB' gain level and then sent to the two (Red and Blue) AWB-controlled amplifiers (see Table 4-6).

Table 4-6. AWB Red/Blue Balance Control

Function	Register	Address
Red Channel Preamplifier Gain Setting	CWF[7:4]	0x05
Blue Channel Preamplifier Gain Setting	CWF[3:0]	0x05
Red Channel Gain Setting	RED[7:0]	0x02
Blue Channel Gain Setting	BLUE[7:0]	0x01

The response time for these two amplifiers are then set by selecting the amplifier response step size for the application, which can be 64 steps for the fastest response (4 bits/step), 256 steps for the slowest response (1 bit/step), or 128 steps (2 bits/step) as a trade-off of stability versus speed. The AWB response time (step select) is set by register COMD[5:4] (0x15).

The AWB mode can be set to fast or slow modes:

- Fast mode – updates every frame
- Slow mode – updates every 16 or 64 frames (Slow mode select)

During power-up, Fast mode is automatically enabled until the device stabilizes, at which point, slow mode is enabled. Slow mode is controlled by register COME[1] (0x20) (slow mode enable) and register COMK[1] (0x70) (slow mode select).

As with the AEC and AGC, the AWB control zone is set to recognize an AWB 'out-of-bounds' condition. Because these two options have different widths (approximately 10% and 20% around a 50% level), the system will have different thresholds for detecting an out-of-white condition. However, in either case, when an out-of-bounds condition is detected, the white balance will be precisely reset. Use register COMC[7] (0x14) to set the control zone parameter.

4.2.2 Manual White Balance

In manual mode, the companion backend chip can control OV7640 internal Red and Blue register values to achieve white balance. These registers are BLUE (0x01) and RED (0x02) and are defined as follows:

- Blue Gain: BLUE[7:0] (0x01)
- Red Gain: RED[7:0] (0x02)

Blue/Red Gain Range: 0.2 ~ 5x

Values in register BLUE[7] (0x01) and RED[7] (0x02) indicate a sign bit. If the value is "1", the gain is greater than 1x increase. If the value is "0", the gain is less than 1x increase. Also, red and blue have a pre-gain at register CWF[7:0] (0x05).

5 Image Controls

The settings for brightness, hue, and sharpness control can be controlled by the following registers:

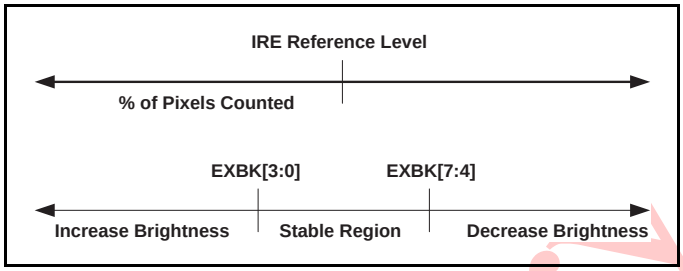
- Brightness: BRT (0x06)
- Hue: HUE (0x04)
- Sharpness: COMF[7:4] (0x26)

5.1 Auto Brightness Control

The Auto Brightness Control (ABC) function is only compatible with a YUV/YCbCr output format. If the OV7640 is configured for RGB or Raw RGB data outputs, the Auto Brightness MUST be disabled and the RGB Brightness enabled (brightness control will work but only in manual mode).

The ABC mode is similar to the AGC method as the percentage of pixels falling below the IRE reference level (%P_L) are counted, the adjust criteria is evaluated and the Brightness setting register is adjusted accordingly (see Figure 5-1).

Figure 5-1 Brightness Setting Adjustment



The Reference Level Select (default = 0 IRE) can change the output brightness "offset", allowing the user to set the brightness level as the application requires.

The range of adjustment around the IRE level can also be changed by enabling the ½ step, ½ range option, which keeps the full 256 bit range but cuts each bit to ½ of its value, effectively halving the final brightness range of the IRE level.

ABC general controls are shown in Table 5-1.

Table 5-1. ABC General Controls

Function	Register	Address
Auto Brightness Enable	COMJ[4]	0x2D
RGB Brightness Enable	SPCC[3]	0x61
Reference Level Select	SPCC[1:0]	0x61
Control Zone – Upper Limit	EXBK[7:0]	0x2C
Control Zone – Lower Limit	EXBK[3:0]	0x2C
Brightness Setting	BRT[7:0]	0x06
½ Step, ½ Range Enable	SPCC[2]	0x61

ABC Fast/Slow mode is in Fast mode by default. Register COML[7] (0x71) enables the ABC slow mode.

- Fast Mode – updates every frame
- Slow Mode – updates every 16 frames

5.2 Color Matrix

The color matrix is used to eliminate the cross talk induced by the micro-lens and color filter process. It also compensates for lighting and temperature effects. The companion backend system ASIC must receive the Bayer RGB raw data pattern, implement the color matrix correction, and then complete the color processing. The calibrated G1, B1, R1 data is a result of the equation: c1=(G*x)+(B*y)+(R*z), where c1 is the calibrated color and x, y, and z are the adjustment values for the corresponding raw color. Refer to Table 5-2 for recommended color matrix settings. The user can change these values based previous experience.

Table 5-2. Recommended Color Matrix Values

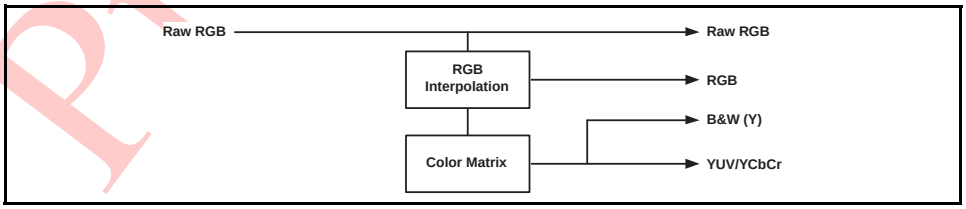
Calibrated $R^1G^1B^1$	Bayer Raw RGB Value		
	R	G	B
R^1 =	1.315	-0.165	-0.150
G^1 =	-0.090	1.205	-0.115
B^1 =	0.021	-1.013	1.992

The color matrix generates YUV and YCbCr outputs from the RGB input as well as color filter crosstalk compensation (compensates for color filter crosstalk in adjacent pixels). Table 5-3 shows the registers used to control the color matrix output.

Table 5-3. Color Matrix Control

Function	Register	Address
RGB Crosstalk Compensation Disable	COMG[4]	0x27
RGB Crosstalk Compensation – R channel	RMCO[7:0]	0x6C
RGB Crosstalk Compensation – G channel	GMCO[7:0]	0x6D
RGB Crosstalk Compensation – B channel	BMCO[7:0]	0x6E

Figure 5-2 Color Matrix Output



The YUV color matrix is used for YUV/YCbCr output. Register YMXB[7:6] (0x67) controls the coefficient of the matrix. Refer to the YMXB (0x67) register description for further details.

- YUV Derivation from RGB: Y: 0.59G + 0.31R + 0.11B
  U: B – Y
  V: R – Y
- YCbCr Derivation from RGB:Y: 0.59G + 0.31R + 0.11B
  Cr: 0.713 (R – Y)
  Cb: 0.563 (B – Y)
- B&W Derivation from RGB: Y Channel

5.2.1 Image Quality Functions

The color channels are then processed for image formatting and quality using the controls shown in Table 5-4 and Table 5-5.

Table 5-4. Image Formatting Controls

Channel	Function	Register	Address
YUV and YCbCr	Hue Enable	HUE[5]	0x04
	Hue Setting	HUE[4:0]	0x04
	Saturation	SAT[7:4]	0x03
RGB	Gamma Enable (also available for YUV/YCbCr)	COMC[2]	0x14

Table 5-5. Image Quality Controls

Function	Register	Address
Band Filter Enable	COMJ[2]	0x2D
Automatic Band Filter Enable	COMN[2]	0x75
Band Filter Clock Select	COMB[6]	0x13
UV Channel '3 Pixel' Averaging Enable	YMXB[4]	0x67
Edge Enhancement Enable	COME[4]	0x20
Edge Enhancement Sensitivity Setting	COMF[7:6]	0x26
Edge Enhancement Strength Setting	COMF[5:4]	0x26
Edge Enhancement ½x Strength Enable	COMK[5]	0x70
Edge Enhancement 2x Strength Enable	COMK[2]	0x70
Even/Odd Noise Compensation Sign	EOC[4]	0x6F
Even/Odd Noise Compensation Setting	EOC[3:0]	0x6F

5.2.1.1 Band Filter

This enables a different exposure algorithm to cut 60 Hz fluorescent-induced light banding.

Automatic Band Filter (ABF) Enable

The exposure time will be set to a minimum of 1/120 second (with longer exposures in multiples of 1/120) but under bright ambient lighting, the filter will automatically be disabled allowing correct exposure (if the lighting decreases, the ABF will be re-enabled).

5.2.1.2 UV Channel '3 Pixel' Averaging

For YUV/YCbCr only, this function is used for noise reduction (default is 'single pixel' averaging).

5.2.1.3 Edge Enhancement (Sharpness)

This function increases the contrast between adjacent pixels. Note that this function is not functional in the OV7640 when in Raw RGB mode.

5.2.1.4 Even/Odd Noise Compensation

Compensates for any DC noise induced by odd column/even column reading.

6 A/D Converters

After the Analog Processing Block, the color channel data signal is fed to two 8-bit Analog-to-Digital (A/D) converters via two multiplexers, one for the Y/G channel and the other shared by the CbCr/BR channels. These A/D converters operate at speeds up to 12 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Optical Black Calibration – Digital Black-Level Calibration (BLC)
- U/V Channel Delay (Optional)
- Additional A/D Range Controls

6.1 Optical Black Calibration

The OV7640/OV7141 CAMERACHIP uses a true optical black (OB) pixel for black level calibration (BLC). BLC compensates for dark current induced temperature and exposure changes. This function is enabled/disabled by register COMF[1] (0x26). When this register is set to "1", calibration is achieved using 2-line true OB pixel averaging. If this register is set to "0", the internal standard value is used for calibration.

This function adds two extra lines of data to the output (total 482 lines for VGA and 242 lines for QVGA mode). If register COMF[0] (0x26) is set to "0", there is no OB pixel line data output (total of 480 lines for VGA and 240 lines for QVGA mode). Refer to Figure 3-5 for details.

Table 6-1. BLC Control Registers

Function	Register	Address
Black-Level Calibration Enable	COMF[1]	0x26
Manual Black-Level Calibration Enable	COMG[2]	0x27
Black-Level Setting – Y/G Channel	YOFF[7:0]	0x21
Black-Level Setting – U/B Channel	UOFF[7:0]	0x22
Black-Level Setting – V/R Channel	VOFF[7:0]	0x2E
Manual Black-Level Manual Offset Enable	COMG[3]	0x27
Manual Y/G Black-Level Offset	YBAS[7:0]	0x78
Manual U/B Black-Level Offset	UBAS[7:0]	0x79
Manual V/R Black-Level Offset	VBAS[7:0]	0x7A

6.1.1 Black-Level Calibration Enable

This function enables all automatic and manual BLC modes.

6.1.2 Manual Black-Level Calibration Enable

The default is Automatic Black-Level Calibration (ABLC). Entering a ’1’ in the COMG[2] (0x27) register bit allows the user to manually enter the black-level settings in the YOFF (0x21), UOFF (0x22), and VOFF (0x2E) registers. If ABLC is enabled, these registers are internally updated by the ABLC function.

6.1.3 Manual Black-Level Manual Offset

If enabled, this function allows the user to use registers YBAS (0x78), UBAS (0x79), and VBAS (0x7A) to insert a manual black-level offset (black-level visual adjust).

Note that the YOFF (0x21), UOFF (0x22), and VOFF (0x2E) registers use bit[7] as the sign bit and bits [6:0] as the value bits.

6.2 U/V Channel Delay

This function is used in the Y-channel Edge Enhancement actions to delay the UV channels = Y channel. Register FRARH[4] (0x2A) is used to enable the UV Channel ’2 Pixel’ Delay. Also, there are two additional register bits at BPBLC[2:1] (0x65) to control UV delay.

6.3 Additional A/D Range Controls

In general, the combination of the A/D Range Multiplier and the A/D Range Control (see Table 6-2) sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Table 6-2. A/D Range Controls

Function	Register	Address
A/D Range Multiplier	ADRC[3]	0x69
A/D Range Control	ADRC[2:0]	0x69

7 Output Formatter

This block controls all output and data formatting required prior to sending the image out on Y[7:0]. Table 7-1 lists the control registers for the Output Formatting functions.

Table 7-1. Output Formatting General Controls

Function	Register	Address
Mirror Image Enable	COMA[6]	0x12
Vertical Flip Enable	COMN[7]	0x75
RGB:565/555 Mode Enable	FACT[4]	0x1F
RGB:565 Output Format Select	FACT[2]	0x1F
RGB:555 Output Format Select	FACT[2]	0x1F

RGB:565 and RGB:555 are alternate output formats where each color is represented by different Y[7:0] bit widths (see Table 7-2).

Table 7-2. RGB:555 and RGB:565 Output Format Controls

Format	Y[7:0]		
	Red	Green	Blue
RGB:565	RRRR Rxxx	GGGG GGxx	BBBB Bxxx
RGB:555	RRRR Rxxx	GGGG Gxxx	BBBB Bxxx

This format uses an odd/even byte pair to express the color for each pixel:

- RGB:565

Bytes	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Even	R7	R6	R5	R4	R3	G7	G6	G5
Odd	G4	G3	G2	B7	B6	B5	B4	B3

- RGB:555

Bytes	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Even	00	R7	R6	R5	R4	R3	G7	G6
Odd	G5	G4	G3	B7	B6	B5	B4	B3

7.1 Windowing

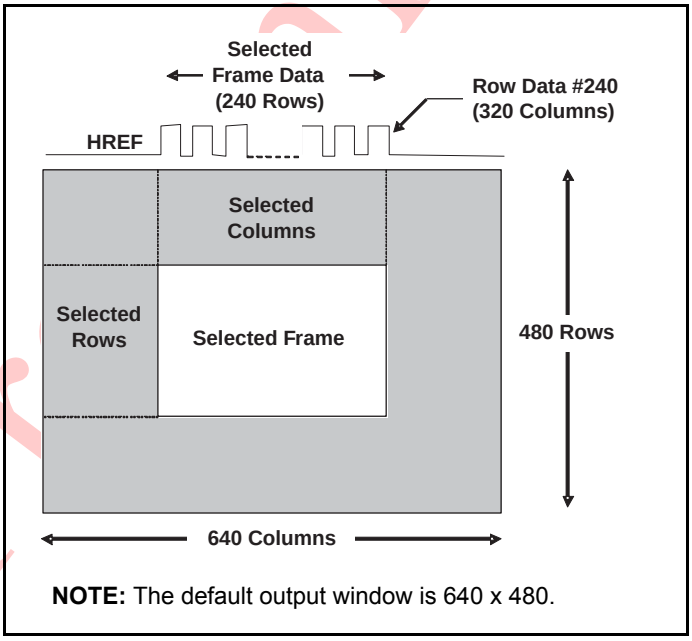
The OV7640/OV7141 CameraChip windowing feature allows the users to define the active pixels used in the final image (frame) as required for low-resolution applications. In other words, the final image can range from 2x2 pixels to the maximum 640x480 pixels, with users selecting the Start/Stop Row/Column addresses (modifying window size and/or position does not change the frame or data rate). When windowing is enabled, the HREF signal is asserted to be consistent with the programmed 'active' horizontal and vertical region. Table 7-3 lists the control registers

Table 7-3. Windowing Control Registers

Function	Register	Address
Horizontal Frame (HREF Column) Start	HSTART[7:0]	0x17
Horizontal Frame (HREF Column) Stop	HSTOP[7:0]	0x18
Vertical Frame (Row) Start	VSTRT[7:0]	0x19
Vertical Frame (Row) Stop	VSTOP[7:0]	0x1A

Figure 7-1 shows an example of a windowed 320x240 frame.

Figure 7-1 Example of Windowing



NOTE: The default output window is 640 x 480.

7.2 Data Formatting

Table 7-4 lists the registers used for Data Formatting.

Table 7-4. Data Formatting

Function	Register	Address
HSYNC/VSYNC Polarity	CLKRC[7:6]	0x11
HREF Polarity	COMC[3]	0x14
YUV Formatting	COMA[4]	0x12
UV Sequence Exchange	COMD[0]	0x15
Output Data MSB/LSB Swap Enable	COMF[2]	0x26
Output Flag Bit Disable	COMD[7]	0x15
Y[7:0] - PCLK Reference Edge	COMD[6]	0x15
ITU-656 Format Enable	COMB[4]	0x13
Output Full Range Enable	COMG[1]	0x27
Frame Rate Adjust Enable (by inserting dummy pixels)	FRARH[7]	0x2A
Frame Rate Adjust Setting MSB (by inserting dummy pixels)	FRARH[6:5]	0x2A
Frame Rate Adjust Setting LSB (by inserting dummy pixels)	FRARL[7:0]	0x2B
Frame Rate Adjust Setting (by inserting dummy lines)	ADDH[7:0], ADDL[7:0]	0x1E, 0x16
Auto Frame Rate Adjust Enable (by inserting dummy lines)	FRARH[2]	0x2A
Auto Frame Rate Adjust Range	COMM[6:5]	0x74
Pixel Delay Select	PSHFT[7:0]	0x1B
Output HSYNC on HREF Pin Enable	COML[5]	0x71
PCLK Output Gated by HREF Enable	COML[6]	0x71
HSYNC Rising Edge Delay MSB	COML[3:2]	0x71
HSYNC Rising Edge Delay LSB	HSDYR[7:0]	0x72
HSYNC Falling Edge Delay MSB	COML[1:0]	0x71
HSYNC Falling Edge Delay LSB	HSDYF[7:0]	0x73
VSYNC Drop Option	COMP[2]	0x7D

7.2.1 ITU-656 Format Enable

Instead of using HREF to define each row, the ITU-656 standard inserts a 4-byte header before and after the row data.

Header Footer: [FF] [00] [00] [Sync Byte]

7.2.2 Frame Rate Adjust

The OV7640/OV7141 offers three methods of frame rate adjustment using the clock prescaler (see Section 3.3.1), by inserting 'dummy' pixels in each row's output, and by inserting dummy lines in each frame output. By inserting these dummy pixels (using FRA[9:0]), the frame rate can be changed while leaving the pixel unchanged.

FRA[9:0] = MSB + LSB = FRARH[6:5] (0x2A) + FRARL[7:0] (0x2B)

- Range: 0.12% to 112%
- Each bit changes the frame rate by 0.12%

By inserting dummy lines at frame output, the user can get the same data rate and the same data read out time at one frame.

Also, in low light (night mode) conditions, the user can turn on auto frame adjust to decrease the random noise and increase the sensitivity. In this mode, FRARH[2] (0x2A) is high. COMM[6:5] (0x74) is used as the frame adjust range and maximum AGC is always at 2. See Table 7-5 for details.

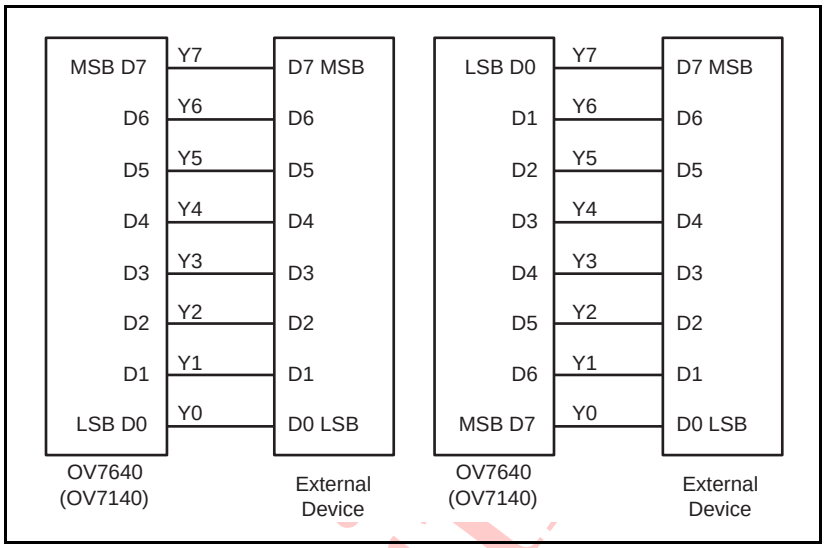
Table 7-5. Auto Frame Rate Adjust Range

COMM[6:5] (0x74)	Maximum Frame Rate Adjust
00	1
01	1/2
10	1
11	1/8

7.2.3 Output Data MSB/LSB Swap Enable

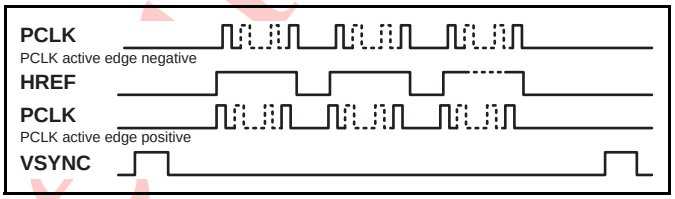
See Figure 7-2 for details when MSB/LSB output data swap is enabled.

Figure 7-2 MSB/LSB Output Data Swap



7.2.4 Y[7:0] - PCLK Reference Edge

To conserve the user's memory space, the PCLK output can be gated by HREF, which defines the active video period.



8 Digital Video Port

The two bits shown in Table 8-1 are used to increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's Y[7:0] loading.

Table 8-1. Output Drive Current

Function	Register	Address
Y[7:0] 2x I_{OL}/I_{OH} Enable	COME[0]	0x20
Y[7:0] 2x I_{OL}/I_{OH} Enable	COMK[6]	0x70

9 SCCB Interface

The *OmniVision Serial Camera Control Bus (SCCB) Functional Specification* is available at http://www.ovt.com. The Functional Specification provides complete information for using the SCCB to control the features of an OmniVision CAMERACHIP. Appendix A, "Reference SCCB Settings contains all register settings and values. However, a quick guide to some of the register settings is provided herein for reference. Also, some reserved registers are detailed in this document.

The OV7640/OV7141 CAMERACHIP uses the SCCB protocol to control the features noted in this document via the companion backend system ASIC. The device slave addresses of the OV7640/OV7141 CAMERACHIP are: 0x42 for write and 0x43 for read. The first command in the SCCB transmission must be a register reset, as most registers will rely on the default value setting.

9.1 Control Functions

Table 9-3 lists the SCCB control functions.

Table 9-1. SCCB Control Functions

Function	Register	Address
Register Reset	COMA[7]	0x12
Standby Mode Enable	COMO[5]	0x76
Tri-state Enable – Y[7:0]	COMB[2]	0x13

9.1.1 Register Reset

All registers can be reset to their default values by using the RESET pin (RESET to VDD_IO) or by using the SCCB interface (see register COMA[7] (0x12)).

9.1.2 Standby Mode Enable

The OV7640/OV7141 CAMERACHIP can be placed in Standby mode by using the PWDN pin (PWDN to VDD_IO) or by using the SCCB interface (see register COMO[5] (0x76)). Note that using the PWDN pin results in lower Standby current (see Electrical Characteristics in the *OV7640/OV7141 Datasheet*).

9.1.2.1 Standby Mode Using the PWDN Pin

Internal device clock is halted and all internal counters are reset to their default values and all SCCB registers remain unchanged.

9.1.2.2 Standby Mode Using the SCCB Interface

Suspends internal circuit activity but does not halt the device clock.

9.1.3 Tri-state Enable

This bit control will immediately tri-state the data outputs. However, all internal signals will continue to be generated and transfer to the output as if it were active. It is the user's responsibility to ensure that the tri-state command is used after all functions have completed their operation.

If the device is put into Standby mode, all outputs, including data and clock, are automatically tri-stated.

9.2 SCCB Low Power Control

The Low Power controls shown in Table 9-2 lower the array, Analog Processing Block (APB), and A/D converter current for low-power operation. However, lowering these current sources will result in a lower signal integration time so the frame rate may need to be decreased in order to preserve the image quality ($f_{INT\ CLK}$).

The array output buffer isolates the array from the AFB – the drive current multiplier bits (SPCC[6:5], 0x61) act to decrease this current.

Table 9-2. SCCB Low Power Control Registers

Function	Register	Address
Array Read Bias "½ Current" Enable	SPCA[3]	0x2F
Array Output Buffer Drive Current Multiplier	SPCC[6:5]	0x61
APB "½ Current" Enable	SPCB[6]	0x60
A/D "½ Current" Enable	ARL[4]	0x68

9.3 Register Set

Table 9-3 provides a list and description of the Device Control registers contained in the OV7640/OV7141. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses for the OV7640/OV7141 are 0x42 for write and 0x43 for read.

For factory-recommended settings, refer to Appendix A, "Reference SCCB Settings.

Note: All registers shown as reserved have no function.

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: [00] to [3F] The basic formula is as follows: Gain = (bit[5]+1) × (bit[4]+1) × (1+bit[3]/2+bit[2]/4+bit[1]/8+bit[0]/16) AGC Enabled: Updated automatically AGC Disabled: User manually stores and updates value
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF] The basic formula is as follows: Blue Gain = 1/3+bit[7]/1.5+bit[6]×47/120+bit[5]×5/24+bit[4]×13/120+bit[3]×7/120+bit[2]×3.8/120+bit[1]/60+bit[0]×1.1/120 AWB Enabled: Updated automatically AWB Disabled: User manually stores and updates value ***Note:*** *This function is not available on the B&W OV7141.*
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF] The basic formula is as follows: Red Gain = 1/3+bit[7]/1.5+bit[6]×47/120+bit[5]×5/24+bit[4]×13/120+bit[3]×7/120+bit[2]×3.8/120+bit[1]/60+bit[0]×1.1/120 AWB Enabled: Updated automatically AWB Disabled: User manually stores and updates value ***Note:*** *This function is not available on the B&W OV7141.*
03	SAT	84	RW	Image Format – Color saturation value Bit[7:4]: Saturation value • Range: [0] to [F] Bit[3:0]: Reserved ***Note:*** *This function is not available on the B&W OV7141.*

Table 9-3. SCCB Register List

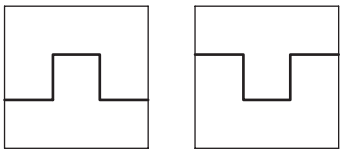
Address (Hex)	Register Name	Default (Hex)	R/W	Description
04	HUE	34	RW	Image Format – Color hue control Bit[7:6]: Reserved Bit[5]: Hue Enable Bit[4:0]: Hue setting • Range: -30° to 30° ***Note:*** *This function is not available on the B&W OV7141.*
05	CWF	3E	RW	AWB – Red/Blue Pre-Amplifier gain setting Bit[7:4]: Red channel pre-amplifier gain setting • Range: [0] to [F] (equal to 0.8 to 1.55 linear change) Bit[3:0]: Blue channel pre-amplifier gain setting • Range: [0] to [F] (equal to 1 to 1.75 linear change) ***Note:*** *This function is not available on the B&W OV7141.*
06	BRT	80	RW	ABC – Brightness setting • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PID	76	R	Product ID number (Read only)
0B	VER	48	R	Product version number (Read only)
0C-0F	RSVD	XX	–	Reserved
10	AECH	41	RW	AEC – Exposure control time (MSB) AEC[9:0] = MSB + LSB = AECH[7:0] + COMO[1:0] AEC Enabled: AEC[9:0] is updated automatically AEC Disabled: User manually stores and updates value
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7:6]: Data Format – HSYNC/VSYNC Polarity_ 00: HSYNC = NEG VSYNC = POS 01: HSYNC = NEG VSYNC = NEG 10: HSYNC = POS VSYNC = POS 11: HSYNC = POS VSYNC = POS  POS NEG Bit[5:0]: Internal Clock Pre-Scalar • Range: [0] to [3F] $f_{INT\ CLK} = f_{CLK} \div (CLKRC[5:0] + 1)$ $t_{INT\ CLK} = t_{CLK} \times (CLKRC[5:0] + 1)$

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COMA	14	RW	Common Control A Bit[7]: SCCB – Register Reset 0: No change 1: Reset all registers to default values Bit[6]: Output Format – Mirror Image Enable Bit[5]: Reserved Bit[4]: Data Format – YUV formatting (when register COMD[0] = 0) 0: Y U Y V Y U Y V 1: U Y V Y U Y V Y (when register COMD[0] = 1) 0: Y V Y U Y V Y U 1: V Y U Y V Y U Y Bit[3]: Output Format – Output Channel Select A 0: YUV/YCbCr 1: RGB/Raw RGB Bit[2]: AWB – Enable Bit[1]: Reserved Bit[0]: ADBLC option 0: ADBLC - only calibrate ADC offset 1: ADBLC - calibrate all channel offset ***Note:*** *This function is not available on the B&W OV7141.*
13	COMB	A3	RW	Common Control B Bit[7]: Reserved Bit[6]: ABF – Band Filter Clock Select (for best performance, choose the option ≈ f_{CLK}) 0: f_{CLK} = 24Mhz 1: f_{CLK} = 12MHz Bit[5]: Reserved Bit[4]: Data Format – ITU-656 Format Enable Bit[3]: Reserved Bit[2]: SCCB – Tri-State Enable – Y[7:0] Bit[1]: AGC – Enable Bit[0]: AEC – Enable

Table 9-3. SCCB Register List

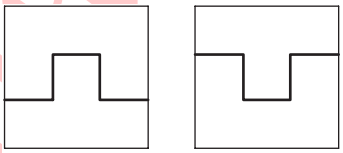
Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COMC	04	RW	Common Control C Bit[7]: AWB – Control Zone Select 0: 10% region (More accurate, less stable) 1: 20% region (More stable, less accurate) ***Note:*** *Bit[7] is not programmable on the B&W OV7141.* Bit[6]: Reserved Bit[5]: Output Format – Resolution 0: VGA (640 x 480) 1: QVGA (320 x 240) Bit[4]: Reserved Bit[3]: Data Format – HREF Polarity 0: HREF Positive 1: HREF Negative  POS NEG Bit[2]: Image Format – RGB Gamma Enable Bit[1:0]: Reserved
15	COMD	00	RW	Common Control D Bit[7]: Data Format – Output Flag Bit Disable 0: Frame = 254 data bits (00/FF = Reserved flag bits) 1: Frame = 256 data bits Bit[6]: Data Format – Y[7:0]-PCLK Reference Edge 0: Y[7:0] data out on PCLK falling edge 1: Y[7:0] data out on PCLK rising edge Bit[5:4]: AWB – Step Select (Affects AWB stability and speed) 00: 1 bit/step (256 steps) 01: 4 bits/step (64 steps) 10: 2 bits/step (128 steps) 11: 4 bits/step (64 steps) ***Note:*** *Bit[5:4] is not programmable on the B&W OV7141.* Bit[3]: AEC – Step Size Limit 0: 32 rows (32 × t_{ROW}) 1: Unlimited step size Bit[2]: Fast speed AEC/AGC Bit[1]: Reserved Bit[0]: Data Format – UV Sequence Exchange (when register COMA[4] = 0) 0: Y U Y V Y U Y V 1: Y V Y U Y V Y U (when register COMA[4] = 1 0: U Y V Y U Y V Y 1: V Y U Y V Y U Y ***Note:*** *Bit[0] is not programmable on the B&W OV7141.*

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
16	ADDL	00	RW	Dummy lines LSB (for frame rate adjust setting)
17	HSTART	1A	RW	Output Format – Horizontal Frame (HREF Column) Start VGA: Each bit = 4 pixels (columns) QVGA: Each bit = 2 pixels (columns) • Default Start Column: 8 ***Note:*** *For maximum output window size of 652x482, minimum value of this register is 0x18.*
18	HSTOP	BA	RW	Output Format – Horizontal Frame (HREF Column) Stop VGA: Each bit = 4 pixels (columns) QVGA: Each bit = 2 pixels (columns) • Default Stop Column: 648 • Maximum Value: 662 ***Note:*** *For maximum output window size of 652x482, maximum value of this register is 0xBB.*
19	VSTRT	03	RW	Output Format – Vertical Frame (Row) Start VGA: Each bit = 2 row scan (Progressive Scan) QVGA: Each bit = 1 row scan ***Note:*** *For maximum output window size of 652x482, minimum value of this register is 0x02.*
1A	VSTOP	F3	RW	Output Format – Vertical Frame (Row) Stop VGA: Each bit = 2 row scan (Progressive Scan) QVGA: Each bit = 1 row scan ***Note:*** *For maximum output window size of 652x482, maximum value of this register is 0xF3.*
1B	PSHFT	00	RW	Data Format – Pixel Delay Select (Delays timing of the Y[7:0] data relative to HREF in pixel units) • Range: [00] (No delay) to [FF] (256 pixel delay)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	ADDH	00	RW	Dummy lines MSB (for frame rate adjust setting)

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	FACT	01	RW	Output Format – Format Control Bit[7:5]: Reserved Bit[4]: RGB:565/555 Enable Control 0: Disabled 1: Enabled ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3]: Reserved Bit[2]: RGB:565/555 Mode Select 0: RGB:565 output format 1: RGB:555 output format ***Note:*** *Bit[2] is not programmable on the B&W OV7141.* Bit[1]: Reserved Bit[0]: AEC – Partial Row Exposure Time Enable (Optional) 0: Minimum exposure = 1 row 1: Minimum exposure time < 1 row, 64 pixels
20	COME	C0	RW	Common Control E Bit[7]: Reserved Bit[6]: AEC – Digital Averaging Enable Bit[5]: Reserved Bit[4]: Image Quality – Edge Enhancement Enable Bit[3]: Reserved Bit[2]: AWB – Auto Mode 'Manual Adjust' Enable (to manually enter data to RED[7:0] and BLUE[7:0]) Bit[1]: AWB – Slow Mode Enable 0: Fast Mode – Update every frame 1: Slow Mode – Update every 16 or 64 frames ***Note:*** *Bit[1] is not programmable on the B&W OV7141.* Bit[0]: Y[7:0] 2X I_{OL} / I_{OH} Enable
21	YOFF	80	RW	BLC – Black-Level Setting – Y/G Channel Bit[7]: Offset Adjust Sign Bit[6:0]: Offset Adjust Value • Range: -127 to +127 Manual BLC Enabled: User manually stores and updates value Manual BLC Disabled: Updated automatically
22	UOFF	80	RW	BLC – Black-Level Setting – U/B Channel Bit[7]: Offset Adjust Sign Bit[6:0]: Offset Adjust Value • Range: -127 to +127 Manual BLC Enabled: User manually stores and updates value Manual BLC Disabled: Updated automatically ***Note:*** *This function is not available on the B&W OV7141.*
23	CLKC	DE	RW	Output Format – QVGA Sampling Bit[7:1]: Reserved Bit[0]: Output Format – QVGA Output Select 0: RGB/YUV/YCbCr 1: Raw RGB
24	AEW	10	RW	AGC/AEC – Stable Operating Region – Upper Limit

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
25	AEB	8A	RW	AGC/AEC – Stable Operating Region – Lower Limit
26	COMF	A2	RW	Common Control F Bit[7:6]: Image Quality – Edge Enhancement Sensitivity Setting • Range: [00] (Maximum) to [11] (Minimum) Bit[5:4]: Image Quality – Edge Enhancement Strength Setting • Range: [00] (Minimum) to [11] (Maximum) Bit[3]: Reserved Bit[2]: Data Format – Output Data MSB/LSB Swap Enable (LSB → MSB (Y[7]) and MSB → LSB (Y[0]) Bit[1]: Black-Level Calibration (BLC) Enable Bit[0]: Optical Black Output Enable
27	COMG	E2	RW	Common Control G Bit[7:5]: Reserved Bit[4]: Color Matrix – RGB Crosstalk Compensation Disable (Used to increase each color filter's efficiency) ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3]: BLC – Manual Black-Level Manual Offset Enable Bit[2]: BLC – Manual Black-Level Calibration Enable 0: Automatic calibration using internal update(s) 1: Manual calibration using user's offset value(s) Bit[1]: Data Format – Output Full Range Enable 0: Output Range = [10] to [F0] (224 bits) 1: Output Range = [01] to [FE] (254/256 bits) Bit[0]: Reserved
28	COMH	20	RW	Common Control H Bit[7]: Output Format – RGB Output Select 0: RGB 1: Raw RGB ***Note:*** *Bit[7] is NOT programmable when COMA[3] = 0.* Bit[6]: Device Select 0: OV7640 1: OV7141 Bit[5]: Output Format – Scan Select 0: Interlaced 1: Progressive Bit[4:0]: Reserved
29	COMI	00	RW	Common Control I Bit[7:2]: Reserved Bit[1:0]: Device Version (Read-only)

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	FRARH	00	RW	Output Format – Frame Rate Adjust High Bit[7]: Data Format – Frame Rate Adjust Enable Bit[6:5]: Data Format – Frame Rate Adjust Setting MSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0] Bit[4]: A/D – UV Channel '2 Pixel Delay' Enable ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3]: Reserved Bit[2]: Night mode – Enable automatic frame rate adjust Bit[1]: AGC/AEC – Center-Based Reference Area Enable Bit[0]: AEC – AEC Method Select 0: Analog: Uses frame percentage of 'out-of-bound' bits 1: Digital: Uses frame average
2B	FRARL	00	RW	Data Format – Frame Rate Adjust Setting LSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0]
2C	EXBK	88	RW	ABC – Control Zone Limits Bit[7:4]: Control Zone – Upper Limit (EXBK[7:4] + EXBK[3:0]) • Range 0.06% ~ 3.85% Bit[3:0]: Control Zone – Lower Limit • Range 0.06% ~ 3.85%
2D	COMJ	81	RW	Common Control J Bit[7:5]: Reserved Bit[4]: ABC – Auto-Brightness Enable Bit[3]: Reserved Bit[2]: AEC – Band Filter Enable Bit[1:0]: Reserved
2E	VOFF	2C	RW	BLC – Black-Level Setting – V/R Channel Bit[7]: Offset Adjust Sign Bit[6:0]: Offset Adjust Value • Range: -127 to +127 Manual BLC Enabled: User manually stores and updates value Manual BLC Disabled: Updated automatically ***Note:*** *This function is not available on the B&W OV7141.*
2F	SPCA	31	RW	Signal Process Control A Bit[7:4]: Array reference control Bit[3]: Low-Power – Sensor "½ Current Read" Enable Bit[2:0]: Array reset voltage control
30	AREF1	00	RW	Array Reference Control 1 Bit[7]: Short voltage selection (user changes are not recommended) Bit[6]: Bit line current half Bit[5:4]: Array current control (user changes are not recommended) Bit[3]: Bypass blooming circuits Bit[2:0]: Blooming circuits voltage reference

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
31	AREF2	C4	RW	Array Reference Control 2 Bit[7]: Bit line current double Bit[6:4]: Reserved Bit[3]: Charge voltage to VDD Bit[2:0]: Reserved
32	AREF3	C0	RW	Reserved
33	AREF4	16	RW	Array Reference Control 4 All control bits are internal use only (user changes are not recommended)
34-5F	RSVD	XX	–	Reserved
60	SPCB	06	RW	Signal Process Control B Bit[7]: AGC – 1.5x Multiplier (Pre-amplifier) Enable Bit[6]: Low-Power – Analog Processor “½ Current Option” Enable Bit[5]: G channel – instead of average, use switch for RGB or color channel Bit[4]: G channel – instead of average, use switch for Y channel Bit[3:0]: Reserved
61	SPCC	80	RW	Signal Process Control C Bit[7]: AGC/AEC – AGC/Analog AEC – Feedback Channel Select 0: RGB, Raw RGB: Feedback using RGB channels 1: YUV/YCbCr: Feedback using Y channel Bit[6:5]: Low-Power – Array Output Buffer Drive Current Multiplier 00: 1 (Maximum drive current into APB) 01: ½ 10: ½ 11: ¼ (Minimum drive current into APB) Bit[4]: Reserved Bit[3]: ABC – RGB Brightness Enable ***Note:*** *Bit[3] is not programmable on the B&W OV7141.* Bit[2]: ABC – ‘½ Step and ½ Range’ Function Enable (Changes range to 128 bits with “1/2 step” intervals) Bit[1:0]: ABC – Reference Level Select 00: 0 IRE 01: 6 IRE 10: 10 IRE 11: 20 IRE
62	RGAM	88	RW	RGB or Color Channel Gamma Control (user changes are not recommended)
63	GAM	11	RW	Gamma Control for Y and RGB/Color Channel
64	YGAM	89	RW	Y Channel Gamma Control (user changes are not recommended) Bit[7:1]: Reserved Bit[0]: Gamma ON/OFF for Y channel

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
65	BPBLC	02	RW	Different BLC Pass Bit[7]: First stage BLC bypass Bit[6]: Second stage BLC bypass Bit[5]: Auto zero RGB bypass Bit[4]: UV BLC bypass Bit[3]: Y channel BLC bypass Bit[2:1]: UV delay 00: 0 tp 01: 1 tp 10: 2 tp 11: 3 tp Bit[0]: Reserved
66	RSVD	XX	–	Reserved
67	YMXB	01	RW	Output Format – YUV Matrix Bit[7:6]: Color Matrix – Matrix Output Select: (Sets coefficients for RGB → YUV/YCbCr conversion) 0.59G + 0.31R + 0.11B → Y α(B - Y) → U and Cb β(R - Y) → V and Cr Bit[7] Bit[6] α β Format 0 0 1 1 YUV 0 1 0.938 0.838 Customer 1 0 0.568 0.713 YCbCr 1 1 0.5 0.5 Customer Bit[5]: Saturation level clip for RGB/Color channel selection 0: 120% over saturation 1: 140% over saturation Bit[4]: Image Quality – UV Channels '3 Pixel' Averaging Enable (Noise reduction, default is 'single pixel' averaging) Bit[3:2]: Y channel delay to synchronize with UV channel Bit[1:0]: Reserved ***Note:*** *This function is not available on the B&W OV7141.*
68	ARL	AC	RW	AGC/AEC – Voltage Reference Bit[7:5]: Reference level for Analog method AEC/AGC Bit[4]: Low-Power – A/D "½ Current Option" Enable Bit[3:2]: ADC common mode feedback reference Bit[1]: ADC reference voltage selection Bit[0]: AD 1 channel power down – when used as Raw RGB output, this bit should be high if COML[4] is low.

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
69	ADRC	42	RW	A/D Control Bit[7:6]: ADC clock edge control Bit[5:4]: ADC comparator reference control Bit[3]: A/D – Range Multiplier 0: Standard range 1: 1.5x standard range Bit[2:0]: A/D – Range Control 000: Minimum (0.8V A/D Maximum) 100: Mid-point (1.0V A/D Maximum) 111: Maximum (1.2V A/D Maximum)
6A-6B	RSVD	XX	–	Reserved
6C	RMCO	11	RW	Color Matrix – RGB Crosstalk Compensation – R Channel $R = R^{\#} + 0.155 \times ((RMCO[7:4] \times (R^{\#}-G^{\#})) + RMCO[3:0](R^{\#}-B^{\#}))$ (Where $R^{\#}$, $G^{\#}$, $B^{\#}$ = Uncompensated Data) ***Note:*** *This function is not available on the B&W OV7141.*
6D	GMCO	01	RW	Color Matrix – RGB Crosstalk Compensation – G Channel $G = G^{\#} + 0.155 \times ((GMCO[7:4] \times (G^{\#}-R^{\#})) + GMCO[3:0](G^{\#}-B^{\#}))$ (Where $R^{\#}$, $G^{\#}$, $B^{\#}$ = Uncompensated Data) ***Note:*** *This function is not available on the B&W OV7141.*
6E	BMCO	06	RW	Color Matrix – RGB Crosstalk Compensation– B Channel $B = B^{\#} + 0.155 \times ((BMCO[7:4] \times (B^{\#}-R^{\#})) + BMCO[3:0](B^{\#}-G^{\#}))$ (Where $R^{\#}$, $G^{\#}$, $B^{\#}$ = Uncompensated Data) ***Note:*** *This function is not available on the B&W OV7141.*
6F	EOC	00	RW	Image Quality – Even/Odd DC Offset (“Noise”) Compensation Bit[7:6]: Reserved Bit[5]: Bypass final stage BLC for Y channel Bit[4]: Compensation Sign Bit[3:0]: Compensation Value • Range: [0] to [F] ***Note:*** *This function is not available on the B&W OV7141.*

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
70	COMK	01	RW	Common Mode Control K Bit[7]: Reserved Bit[6]: Y[7:0] 2X I_{OL} / I_{OH} Enable Bit[5]: Image Quality – Edge Enhancement ½x Strength Enable 0: Multiplier = 1x 1: Multiplier = ½x Bit[4:3]: Reserved Bit[2]: Image Quality – Edge Enhancement 2x Strength Enable 0: Multiplier = 1x 1: Multiplier = 2x Bit[1]: AWB – Slow Mode Select 0: Update every 16 frames 1: Update every 64 frames Bit[0]: Reserved
71	COML	00	RW	Common Mode Control L Bit[7]: ABC – Slow Mode Enable 0: Fast Mode: Update every frame 1: Slow Mode: Update every 16 frames Bit[6]: Data Format – PCLK output gated by HREF Enable Bit[5]: Data Format – Output HSYNC on HREF Pin Enable Bit[4]: Raw RGB option – when high, use 2-channel ADC in this mode Bit[3:2]: Data Format – HSYNC Rising Edge Delay MSB Bit[1:0]: Data Format – HSYNC Falling Edge Delay MSB
72	HSDYR	10	RW	Data Format – HSYNC Rising Edge Delay LSB HSYNCR[9:0] = MSB + LSB = COML[3:2] + HSDYR[7:0] • Range 000 to 762 pixel delays
73	HSDYF	50	RW	Data Format – HSYNC Falling Edge Delay LSB HSYNCF[9:0] = MSB + LSB = COML[1:0] + HSDYF[7:0] • Range 000 to 762 pixel delays
74	COMM	20	RW	Common Mode Control M Bit[7]: Reserved Bit[6:5]: AGC – Maximum Gain Select 00: +6 dB (2x) 01: +12 dB (4x) 10: +6 dB (2x) 11: +18 dB (8x) When FRARH[2] is high, these 2 bits control the frame rate adjust range Bit[4:0]: Reserved
75	COMN	02	RW	Common Mode Control N Bit[7]: Output Format – Vertical Flip Enable Bit[6:4]: Reserved Bit[3]: Drop frame for HREF Bit[2]: ABF– Automatic Band Filter Enable Bit[1:0]: Reserved

Table 9-3. SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
76	COMO	00	RW	Common Mode Control O Bit[7:6]: Reserved Bit[5]: Standby Mode Enable Bit[4:2]: Reserved Bit[1:0]: AEC – Exposure Time LSB
77	AEGR	F3	RW	AEC/AGC – Control Zone Limits Bit[7:4]: Upper Limit MSB Bit[3:0]: Lower Limit MSB As these limits are only 4 bits, they are used as the MSB Nibble as shown: Upper Limit = AEGR[7:4] + 0000 Lower Limit = AEGR[3:0] + 0000
78	YBAS	80	RW	BLC – Manual Y/G Black-Level Offset • Range: –127 to +127
79	UBAS	80	RW	BLC – Manual U/B Black-Level Offset • Range: –127 to +127 ***Note:*** *This function is not available on the B&W OV7141.*
7A	VBAS	80	RW	BLC – Manual V/R Black-Level Offset • Range: –127 to +127 ***Note:*** *This function is not available on the B&W OV7141.*
7B	RSVD	XX	–	Reserved
7C	AECL1	00	RW	AEC – Partial Row Sampling – Bits Sampled • Range: [40] (64 bits) to [FF] (256 bits)
7D	COMP	77	RW	Common Mode Control P Bit[7:3]: Reserved Bit[2]: Data Format – VSYNC Drop Option 0: VSYNC always exist 1: VSYNC will drop when frame data drops Bit[1:0]: Reserved
7E	AVGY	00	RW	AEC – Digital Y/G Channel Average (Automatically updated by AGC/AEC, user can only read the values)
7F	AVGR	00	RW	AEC – Digital R/V Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7141.*
80	AVGB	00	RW	AEC – Digital B/U Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7141.*

10 Prototyping and Evaluation Modules

OmniVision Technologies Inc. supplies prototyping and evaluation modules to demonstrate operation of the associated CAMERACHIP products, as well as to demonstrate associated companion back-end system ASICs, where required.

10.1 OV7640/OV7141AA Prototyping Module

The OV7640/OV7141AA prototyping module is used for general design-in and evaluation purposes. The module provides a simple 32-pin header-connector interface to the relevant I/O and control registers in the OV7640/OV7141 CAMERACHIP. The module includes the necessary 24 Mhz crystal, capacitors, and resistors.

The OV7640/OV7141AA prototyping module can be directly connected to any companion back-end ASIC solution or system interface. The header-connector interface allows for access to the 10-bit digital output data, PCLK, vertical sync, and horizontal sync signals. The back-end interface can use the Serial Camera Control Bus (SCCB) interface software to adjust the control register values.

10.2 OV7640/OV7141Cx USB2.0 Evaluation Module

The OV7640/OV7141Cx USB2.0 evaluation module is provided so that potential customers may evaluate both the live video function of the CAMERACHIP as well as the SCCB control interface software. The OV7640/OV7141 CAMERACHIP output is a RGB raw data stream connected to the input registers of a Cypress Semiconductors, Inc., USB FX2 controller operating at a high-speed bus data rate (40 Mbps).

Using a WinTel computer system with a P4® processor running at 1.5 GHz or faster, the OV7640/OV7141 USB module will stream video in VGA format (640x480 at 30 fps) or in QVGA format (320x240 at 60 fps). This configuration requires a Windows® 2000 or XP operating system. Additionally, the SCCB software allows the evaluator to adjust the image characteristics in real-time.

11 Lens selection

The OV7640/OV7141 is a quarter-inch format CAMERACHIP that is compatible with numerous lenses in the market. The key considerations in lens selection are lens quality and resultant cost. OmniVision Technologies, Inc. has qualified several lens suppliers for the various formats, sizes, and quality of lenses available. OmniVision has developed a Lens Supplier Partner List to complement our CAMERACHIP products. This listing is available at http://www.ovt.com on the Partners page.

12 OV7640/OV7141 Bug List

None as of this revision

Appendix A Reference SCCB Settings

Sensor: OV7640 VGA sensor
Main Clock Speed: 24 MHz
Image Transfer Rate: 30 fps VGA video
Output Format: RGB:565
Auto ON/OFF: ON
Pixel Clock Speed: 24 MHz

Address	Value
0x12	0x80
0x03	0xA4
0x04	0x30
0x05	0x88
0x06	0x60
0x11	0x00
0x12	0x0D
0x13	0xA3
0x14	0x04
0x15	0x04
0x1F	0x51
0x20	0xD0
0x23	0xDE
0x24	0x80
0x25	0x60
0x26	0xC2
0x27	0xE2
0x28	0x20
0x2A	0x11
0x2B	0x00

Address	Value
0x2D	0x05
0x2F	0x9C
0x30	0x00
0x31	0xC4
0x60	0xA6
0x61	0x68
0x62	0x88
0x63	0x11
0x64	0x88
0x65	0x00
0x67	0x94
0x68	0x7A
0x69	0x04
0x6C	0x11
0x6D	0x33
0x6E	0x22
0x6F	0x00
0x74	0x20
0x75	0x0E
0x77	0xC4

Sensor: OV7640 VGA sensor
Main Clock Speed: 24 MHz
Image Transfer Rate: 30 fps VGA video
Output Format: Raw RGB
Auto ON/OFF: OFF (ON)
Pixel Clock Speed: 12 MHz

Address	Value
0x12	0x80
0x03	0xA4
0x04	0x30
0x05	0x88
0x06	0x60
0x11	0x00 (0x01 for 15 fps)
0x12	0x09 (0x0D for Auto ON)
0x13	0xA0 (0xA3 for Auto ON)
0x14	0x00 (0x20 for QVGA)
0x15	0x04
0x1F	0x41
0x20	0xC0
0x23	0xDE
0x24	0xA0
0x25	0x80
0x26	0x32
0x27	0xF2
0x28	0xA0
0x2A	0x11
0x2B	0x00
0x2D	0x05

Address	Value
0x2F	0x9C
0x30	0x00
0x31	0xC4
0x60	0xA6
0x61	0x68
0x62	0x88
0x63	0x11
0x64	0x88
0x65	0x00
0x67	0x94
0x68	0x7A
0x69	0x04
0x6C	0x11
0x6D	0x33
0x6E	0x22
0x6F	0x00
0x74	0x20
0x75	0x0E
0x77	0xB5
0x01	0x80
0x02	0x80

Sensor: OV7640 VGA sensor
Main Clock Speed: 14.7 MHz
Image Transfer Rate: 15 fps QVGA video
Output Format: RGB:565
Auto ON/OFF: ON
Pixel Clock Speed: 14.7/4 MHz

Address	Value	Address	Value
0x12	0x80	0x2D	0x05
0x03	0xA4	0x2F	0x9C
0x04	0x30	0x30	0x00
0x05	0x88	0x31	0xC4
0x06	0x60	0x60	0xA6
0x11	0x01	0x61	0x68
0x12	0x0D	0x62	0x88
0x13	0xA3	0x63	0x11
0x14	0x24	0x64	0x88
0x15	0x04	0x65	0x00
0x1F	0x51	0x67	0x94
0x20	0xD0	0x68	0x7A
0x23	0xDE	0x69	0x04
0x24	0x80	0x6C	0x11
0x25	0x60	0x6D	0x33
0x26	0xC2	0x6E	0x22
0x27	0xE2	0x6F	0x00
0x28	0x00	0x74	0x20
0x2A	0x91	0x75	0x0E
0x2B	0xAC	0x77	0xC4

Sensor: OV7640 VGA sensor
Main Clock Speed: 24 MHz
Image Transfer Rate: 30 fps VGA video
Output Format: YUV 4:2:2 8 bits
Auto ON/OFF: ON
Pixel Clock Speed: 24 MHz

Address	Value	Address	Value
0x12	0x80	0x2D	0x05
0x03	0xA4	0x2F	0x9C
0x04	0x30	0x30	0x00
0x05	0x88	0x31	0xC4
0x06	0x60	0x60	0x86
0x11	0x00 (0x01 for 15 fps)	0x61	0xE0
0x12	0x05	0x62	0x88
0x13	0xA3	0x63	0x11
0x14	0x04	0x64	0x89
0x15	0x04	0x65	0x00
0x1F	0x41	0x67	0x94
0x20	0xD0	0x68	0x7A
0x23	0xDE	0x69	0x04
0x24	0xA0	0x6C	0x11
0x25	0x80	0x6D	0x33
0x26	0x32	0x6E	0x22
0x27	0xE2	0x6F	0x00
0x28	0x20	0x74	0x20
0x2A	0x11	0x75	0x0E
0x2B	0x00	0x77	0xC4

Note:

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