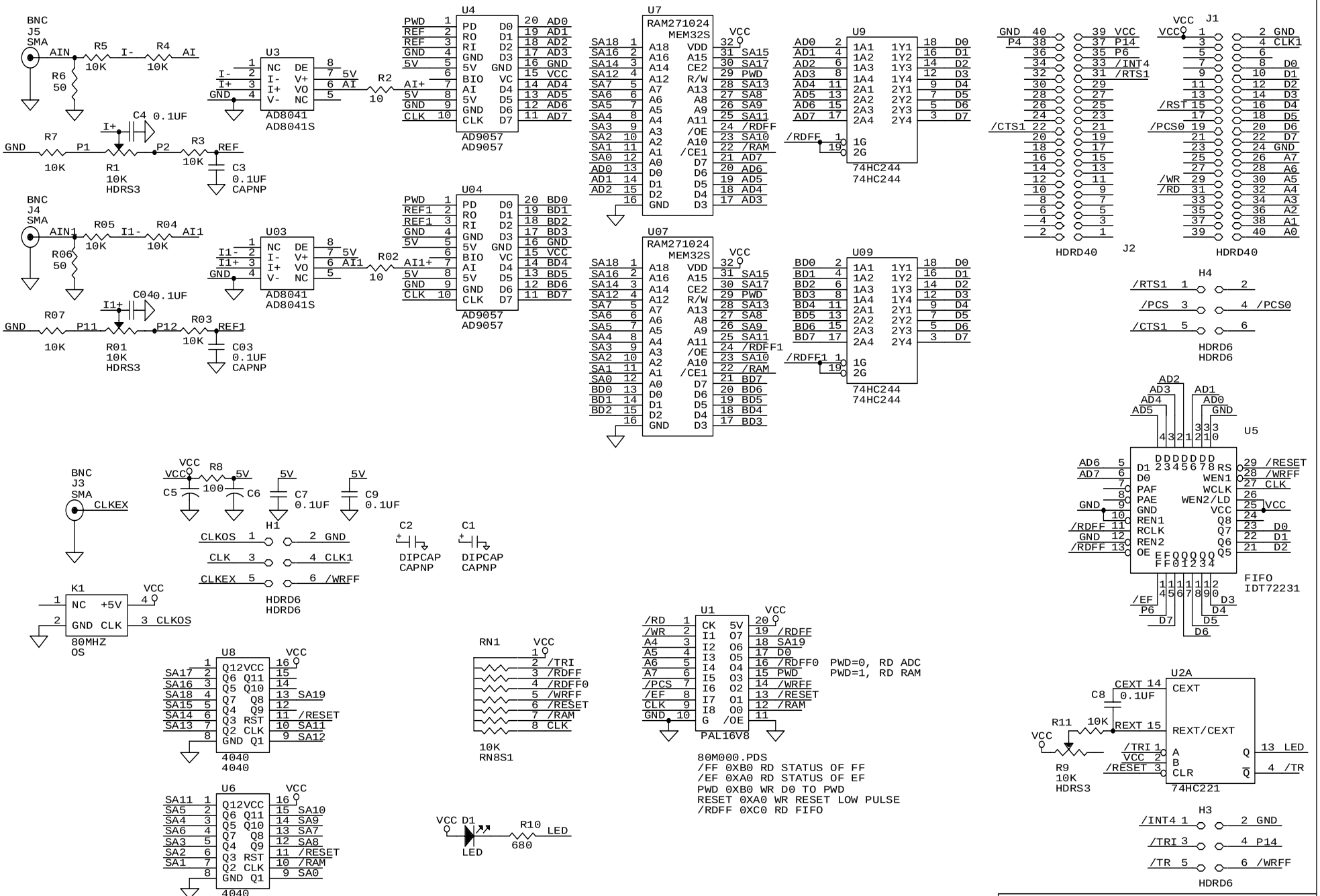
BNC J5 SMA
AIN
R5 10K
R4 10K
I-
AI
R6 50
C4 0.1UF
I+
GND
R7 10K
P1
P2
R1 10K HDRS3
R3 10K
REF
C3 0.1UF CAPNP
U3
NC DE
I- V+
I+ VO
V- NC
AD8041
AD8041S
5V
AI
R2 10
AI+
U4
PD D0
RO D1
RI D2
GND D3
5V GND
BIO VC
AI D4
5V D5
GND D6
CLK D7
AD9057
AD9057
PWD
REF
GND
5V
CLK
AD0
AD1
AD2
AD3
U7
RAM271024
MEM32S
A18 VDD
A16 A15
A14 CE2
A12 R/W
A7 A13
A6 A8
A5 A9
A4 A11
A3 /OE
A2 A10
A1 /CE1
A0 D7
D0 D6
D1 D5
D2 D4
GND D3
VCC
SA15
SA17
PWD
SA13
SA8
SA9
SA11
/RDFF
SA10
/RAM
U9
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
1G
2G
74HC244
74HC244
/RDFF
J1
J2
HDRD40
HDRD40
/RTS1
/INT4
/CTS1
/RST
/PCS0
/WR
/RD
H4
/PCS
HDRD6
HDRD6
BNC J4 SMA
AIN1
R05 10K
R04 10K
I1-
AI1
R06 50
C04 0.1UF
I1+
R07 10K
P11
P12
R01 10K HDRS3
R03 10K
REF1
C03 0.1UF CAPNP
U03
I1-
I1+
AI1+
R02 10
U04
REF1
AI1
U07
RAM271024
MEM32S
/RDFF1
U09
BNC J3 SMA
CLKEX
VCC
R8 100
C5
C6
C7 0.1UF
C9 0.1UF
H1
CLKOS
CLK
CLKEX
HDRD6
HDRD6
C2
C1
DIPCAP CAPNP
DIPCAP CAPNP
K1
NC +5V
GND CLK
80MHZ OS
U5
AD2
AD3
AD4
AD5
AD1
AD0
GND
AD6
AD7
/RDFF
/RESET
/WRFF
CLK
WEN1
WCLK
WEN2/LD
REN1
RCLK
REN2
OE
Q8
Q7
Q6
Q5
FIFO IDT72231
/EF
P6
D3
D4
D5
D6
D7
U8
Q12VCC
Q6 Q11
Q5 Q10
Q7 Q8
Q4 Q9
Q3 RST
Q2 CLK
GND Q1
4040
4040
SA19
/RESET
SA11
SA12
RN1
/TRI
/RDFF0
/WRFF
/RESET
/RAM
CLK
10K RN8S1
U1
CK 5V
I1 O7
I2 O6
I3 O5
I4 O4
I5 O3
I6 O2
I7 O1
I8 O0
G /OE
PAL16V8
/RD
/WR
/PCS
/EF
CLK
GND
PWD=0, RD ADC
PWD=1, RD RAM
80M000.PDS
/FF 0XB0 RD STATUS OF FF
/EF 0XA0 RD STATUS OF EF
PWD 0XB0 WR D0 TO PWD
RESET 0XA0 WR RESET LOW PULSE
/RDFF 0XC0 RD FIFO
U6
SA11
SA10
SA9
SA7
SA8
SA0
VCC D1
LED
R10 680
U2A
CEXT
C8 0.1UF
R11 10K
REXT 15
REXT/CEXT
/TRI
/RESET
R9 10K HDRS3
74HC221
LED
/TR
H3
/INT4
/TR
HDRD6
STE/TERN
Title
80MHZ ADC
Size B
Document Number
80M.SCH
REV
Date: November 6, 1999
Sheet 1 of 1