The Main Difference between R8800/10/20/30/22 Ver.D and Am186(188)EM/ES/ED

- **The corresponding type:**

  R8800 <-> Am186EM ; R8810 <-> Am188EM

  R8820 <-> Am186ES ; R8830 <-> Am188ES

  R8822 <-> Am186ED

- **Main Difference:**

  1. The processor release ID value.
     - Please refer the Appendix A for the Processor release ID of R88xx
  2. The I/O characteristic.
     - Please refer the Appendix B for the I/O Characteristics description
  3. The crystal pad characteristic.
     - Please refer the Appendix C for the crystal description
  4. The instruction set clock cycle.
     - Please refer the Instruction Set Opcodes and Clock Cycles Unit of datasheet.
  5. Boot ROM size with 8bit/16bit data bus option for R8820.
     - Am186ES only supports 16bit data bus access.
     - Add USIZ bit in Auxiliary Configuration Register. Please refer the Auxiliary Configuration Register of datasheet.
  6. INT3 with internal 10K pull up resistor.
     - External 2.2K pull low resistor should be added when enable INT3
  7. Programming procedure to enable Pin76 (DRQ1/INT6/PIO13) as INT6 or Pin77 (DRQ0/INT5/PIO12) as INT5.
     - The enable INT5/INT6 procedure for R8820/30/22

       (a). Program pin77/ pin76 as normal function (0xff70/0xff72)

       (b). IMASK register (0xff28), bit3/bit2 clear as 0

       (c). Set the int5con/int6con (0xff34/0xff36) register as (0x0003)

       (d). Set DMA Control Register Bit 3 (0xffca/0xffda) as 1
     - The procedure doesn't care item (d) for Am186ES/ED and Am188ES.
     - INT5/DMA0 and INT6/DMA1 can't share common interrupt vector. (INT5 and DMA0 can't exist at the same time.)
     - Default normal function pin as DMA0/DMA1.
     - INT5 and INT6 are both level-triggered only, not necessary to be held high level until the interrupt is acknowledged.

8. INT0~INT4 Interrupts.
   - Add Edge trigger mode enable bit (bit7 ETM) in each Interrupt Control register. Please refer each Interrupt Control Register of datasheet.
9. The Interrupts are requested with same priority.
   - Suggest the specific EOI is the most secure method.
10. Power down function.
   - Please refer the Power Save and Power Down Unit of datasheet.
11. Pulse Width Demodulation for R8820/30/22.
   - Timer 0 for INT2, Timer 1 for INT4.
12. DCE/DTE Protocol for R8820/30/22.
   - RTS signal only goes active before the character is shifted out.
13. Clock Prescalar Register and Enable RCU Register.
   - Extend Refresh Counter Reload Value (RC14-RC0) and Refresh Count (T14-T0)
14. CLKOUT B doesn't supply an additional clock with a delayed output compared to CLKOUT A.
15. Don't supply data strobe (DS) signal.
   - Please refer $\overline{\text{DEN}}$/PIO5 pin description of datasheet.
16. Don't supply bus lock (LOCK) signal for R8820/30.
   - Please refer S6/$\overline{\text{CLKDIV2}}$/PIO29 pin description of datasheet.

Appendix A.

Released Level number of R88xx

The value of R88xx release ID in the Processor Release Level Register (Offset 00F4h)

CPU Type	ID Number
R8800D	84D9h
R8810D	84D9h
R8820D	04D9h
R8830D	04D9h
R8822D	64D9h

Appendix B

R88xx I/O Characteristics of each pin

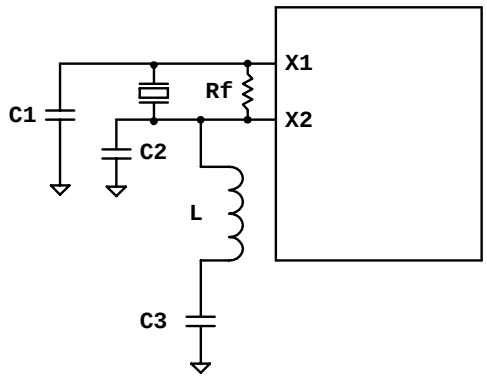
Pin NO.	Pin Name	Characteristics
71	$\overline{RST}$	Schmitt Trigger input, with internal 50K pull-up resistor
8	ARDY	Schmitt Trigger input, with internal 50K pull-down resistor
45 47	HOLD NMI	CMOS input, with internal 50K pull-down resistor
56 55	INT0 INT1/$\overline{SELECT}$	Schmitt Trigger TTL input, with internal 10K pull-down resistor
16 17	CLKOUTA CLKOUTB	8 mA 3-State CMOS output
9	$\overline{S2}$	Bi-direction I/O, with 50 K internal pull-up resistor 4mA TTL output
10 11	$\overline{S1}$ $\overline{S0}$	4 mA 3-State CMOS output
43 6 5	$\overline{WLB}$ $\overline{RD}$ $\overline{WR}$	12 mA 3-State CMOS output
19 20 22	A19/PIO9 A18/PIO8 A17/PIO7	Bi-direction I/O, with enabled/disabled 10 K internal pull-up resistor when functions as PIO, for normal function the 10k pull-up resistor is disabled. 16mA TTL output

23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 39 40	A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	16 mA 3-State CMOS output
78 80 82 84 86 88 91 94 79 81 83 85 87 90 93 95	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	Bi-direction I/O, 16mA TTL output
7	ALE	Bi-direction I/O , with 50 K internal pull-down resistor 4mA TTL output
46 74 73 2 1	SRDY/PIO6 TMROUT0/PIO10 TMROUT1/PIO1 TXD0/PIO22 RXD0/PIO23	Bi-direction I/O , with enabled/disabled 10 K internal pull-down resistor when functions as PIO, for normal function the 10k pull-down resistor is disabled. 8mA TTL output
4	$\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$	Bi-direction I/O , with 50 K internal pull-up resistor 4mA TTL output
42	$\overline{\text{WHB}}$	Bi-direction I/O , with 50 K internal pull-up resistor 12mA TTL output
44	HLDA	4 mA CMOS output
54 52	INT2/ $\overline{\text{INTA0}}$ /PIO31 INT4/PIO30	Bi-direction I/O , with enabled/disabled 10 K internal pull-up resistor when functions as PIO, for normal function the 10k pull-up resistor is disabled. 8mA TTL output, TTL Schmitt Trigger input
53	INT3/ $\overline{\text{INTA1}}$ /IRQ	Bi-direction I/O , with 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input
57 58	$\overline{\text{UCS}}$/ $\overline{\text{ONCE1}}$ $\overline{\text{LCS}}$/ $\overline{\text{ONCE0}}$	Bi-direction I/O , with 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input

49	$\overline{DEN}$/PIO5	Bi-direction I/O, with enabled/disabled 10 K internal pull-up resistor when functions as PIO, for normal function the 10k pull-up resistor is disabled. 8mA TTL output
48	DT/$\overline{R}$ /PIO4	
66	$\overline{PCS0}$/PIO16	
65	$\overline{PCS1}$/PIO17	
63	$\overline{PCS2}$/$\overline{CTS1}$/$\overline{ENRX1}$/PIO18	
62	$\overline{PCS3}$/$\overline{RTS1}$/$\overline{RTR1}$/PIO19	
60	$\overline{PCS5}$/A1/PIO3	
59	$\overline{PCS6}$/A2/PIO2	
50	$\overline{MCS0}$/PIO14	
51	$\overline{MCS1}$/PIO15	
68	$\overline{MCS2}$/PIO24	
69	$\overline{MCS3}$/$\overline{RFSH}$/PIO25	
97	$\overline{UZI}$/PIO26	
96	S6/$\overline{CLKDIV2}$/PIO29	
75	TMRIN0/PIO11	
72	TMRIN1/PIO0	
77	DRQ0/INT5/PIO12	
76	DRQ1/INT6/PIO13	
98	TXD1/PIO27	
99	RXD1/PIO28	
100	$\overline{CTS0}$/$\overline{ENRX0}$/PIO21	
3	$\overline{RTS0}$/$\overline{RTR0}$/PIO20	

Appendix C

Crystal Oscillator R, L, C reference value for R88xx



For fundamental-mode crystal:

Reference valve

Frequency	10.8288M Hz	19.66M Hz	30M Hz	33M Hz	40M Hz
Rf	None	None	None	None	None
C1	10Pf	10Pf	None	None	None
C2	10Pf	10Pf	10Pf	10Pf	10Pf
C3	None	None	None	None	None
L	None	None	None	None	None

For third-overtone mode crystal:

Reference valve

Frequency	22.1184M Hz	28.322M Hz	33.177M Hz	40M Hz	44.1M Hz
Rf	1M	1.5M	1.5M	1.5M	1.5M
C1	15Pf	15Pf	15Pf	15Pf	15Pf
C2	30Pf	30Pf	30Pf	30Pf	30Pf
C3		220Pf	220Pf	220Pf	120Pf
L		10uL	4.7uL	2.7uL	2.7uL