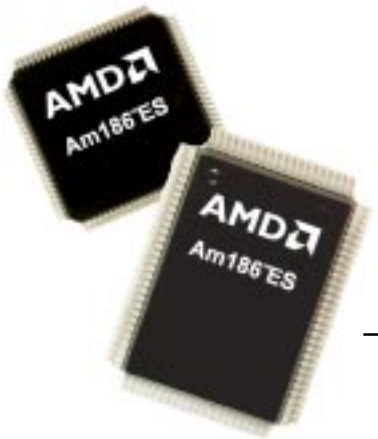
Systems in Silicon

Am186ES Microcontroller

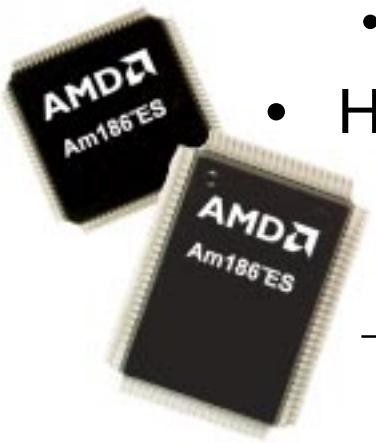
386-class performance, enhanced system integration, and lower system cost



Systems in Silicon

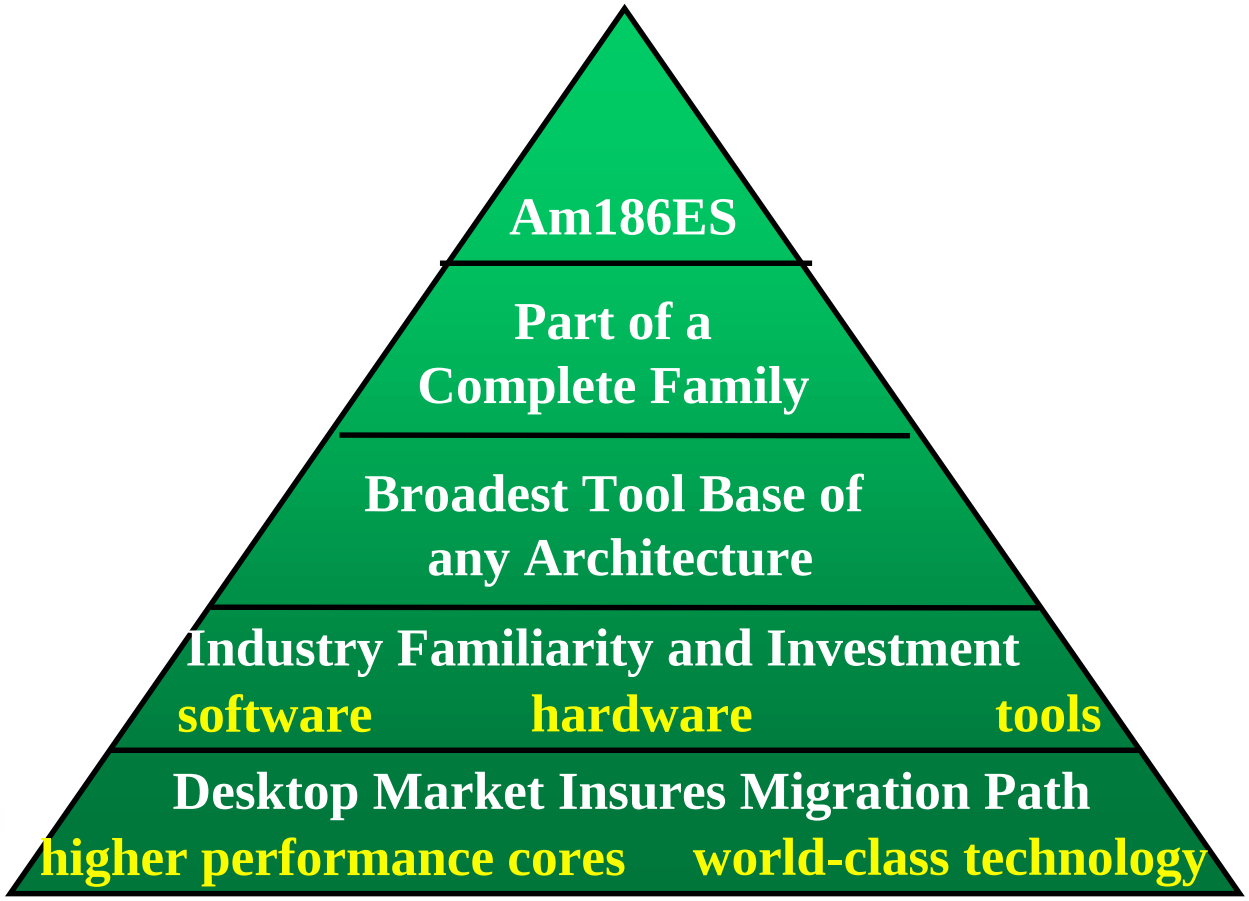
Why x86?

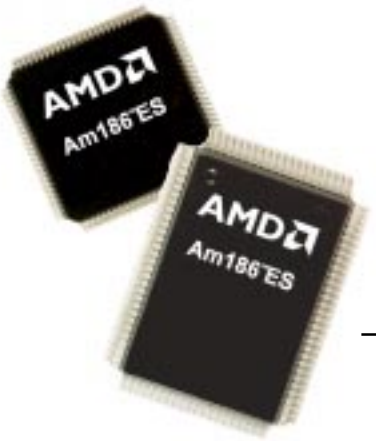
- Industry leader in development tools
- Industry familiarity
  - Hardware/software
  - Tools
  - Yearly investment in architecture
- Desktop market insures migration path
  - One architecture encompassing 16-/32-bit applications and beyond
  - Upgradability and backward compatibility
- High code density



Systems in Silicon

x86 Compatibility Leverage



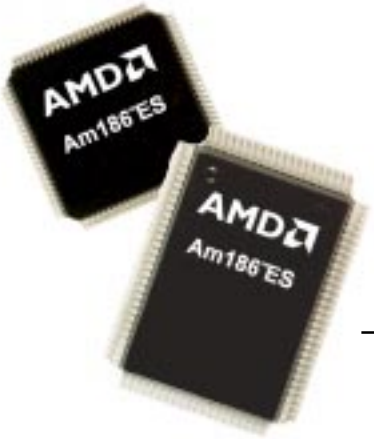


x86 is the worlds most successful architecture

Systems in Silicon

Am186 System Evolution

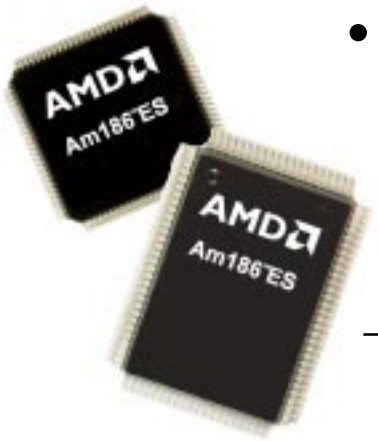
	80C186 Based 3.37 MIP System	Am186EM Based 5.35 MIP System	Am186ES Based 5.35 MIP System
Internal	CPU Basic System Logic	CPU Basic System Logic 1 Async & 1 Sync. Serial 32 PI/O 3 New Interrupts	CPU Basic System Logic 2 Async Serial Ports PWD 2 DMA 32 PI/O
External	Advanced System Logic RAM FLASH	RAM FLASH	RAM FLASH



Systems in Silicon

Faster Time-To-Market

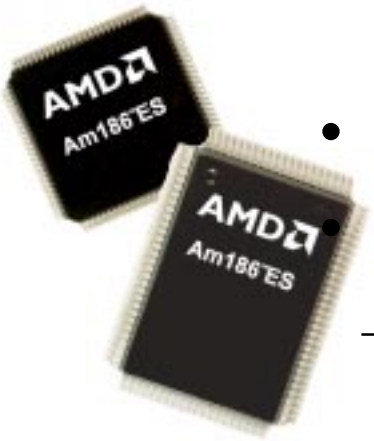
- Leverage 186 compatibility
  - Previous software
  - Existing tools
  - Industry Experience
- Leverage system integration
  - Glueless memory interface
  - General system logic
  - 32-bit performance
- Results: Faster time-to-market



Systems in Silicon

Am186ES Feature Set

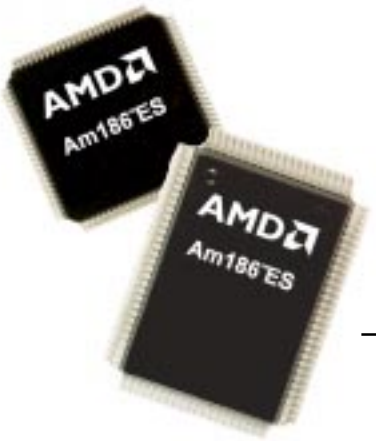
- Two Asynchronous Serial Ports
- 1x clocking (40MHz crystal, not 80MHz)
- Glueless interface to ROM, SRAM, and FLASH
- Pulse width modulation and pulse width demodulation
- 32 programmable I/Os
- 8 external and 8 internal interrupts
  - Watch dog timer
- 2 DMA channels (to and from Asynchronous Ports)
- 12 Chip Selects



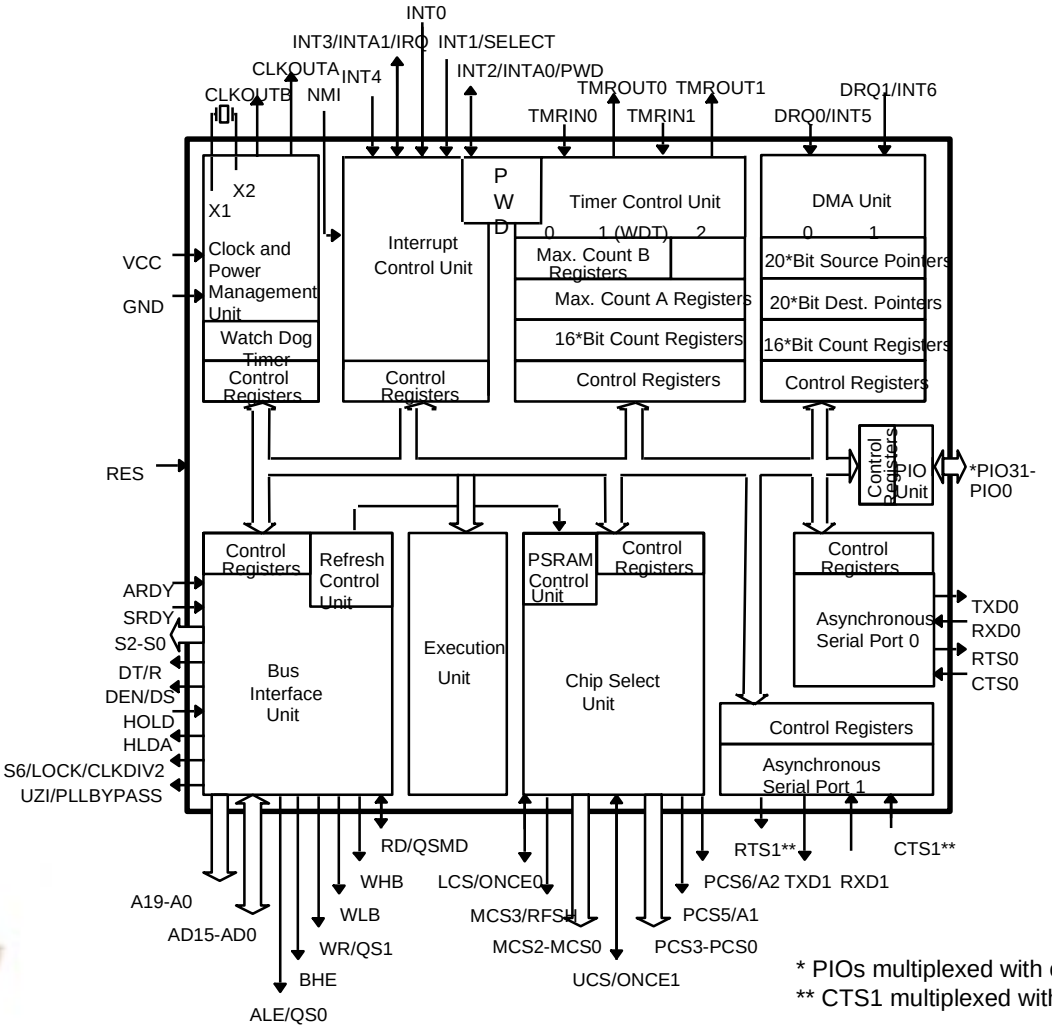
Systems in Silicon

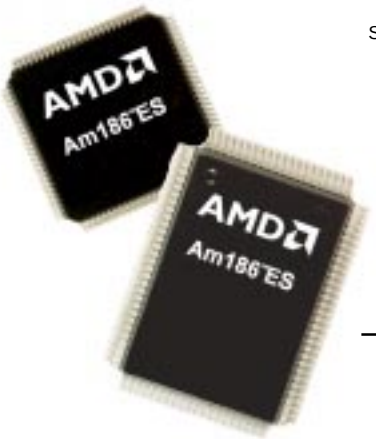
Am186ES Value Proposition

- 32-bit performance for 16-bit price
- 186 compatible software and device drivers
- Extended feature set
  - glueless interface to memory
  - two asynchronous serial ports
  - pulse width demodulation



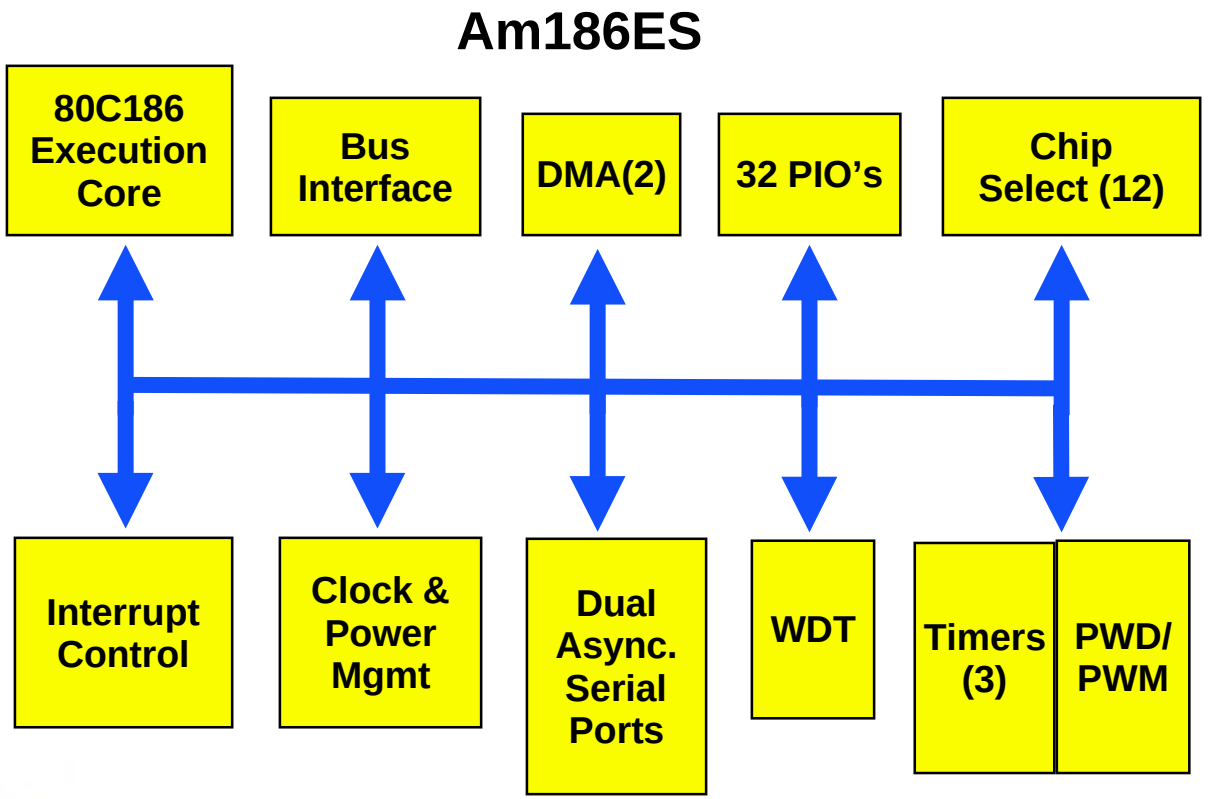
Am186ES Block Diagram

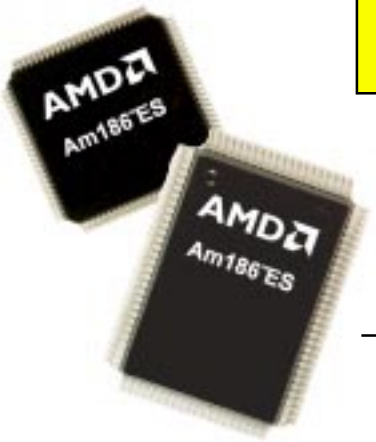




* PIOs multiplexed with other signals
** CTS1 multiplexed with PCS2, RTS1 multiplexed with PCS3

Am186ES Logic Diagram

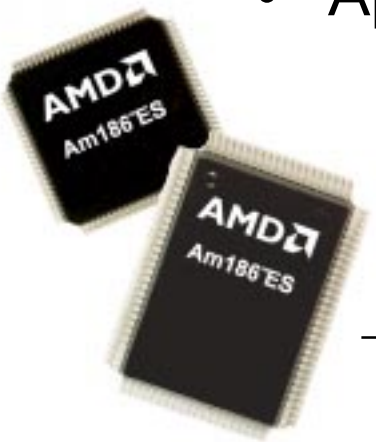




Systems in Silicon

Upgrading from the 186/188 to the Am186ES or Am188ES

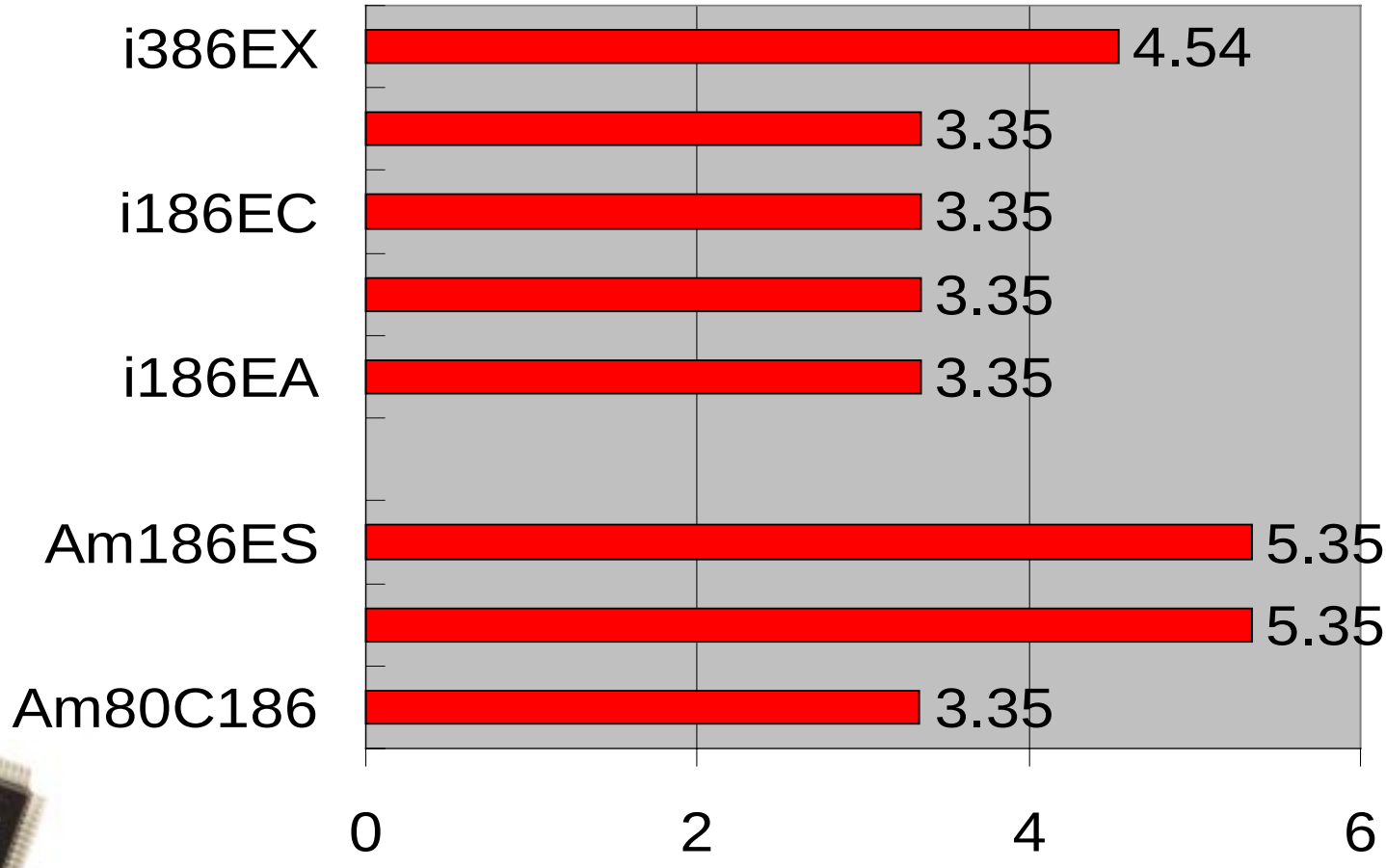
- Software compatible with 186/188
- Glueless connection to memory (lower system cost)
- Demultiplexed address bus (higher performance)
  - Zero wait state w/ 70ns memories
- 2 Integrated Asynchronous Serial Ports
- Approximately 60% performance of 186

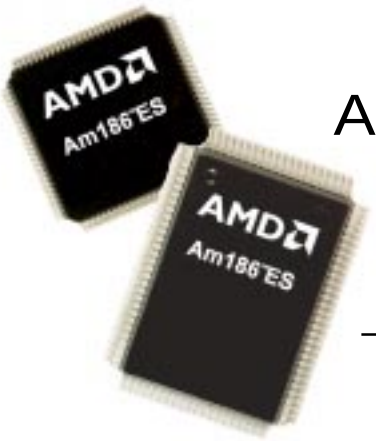


E86 Performance

Systems in Silicon

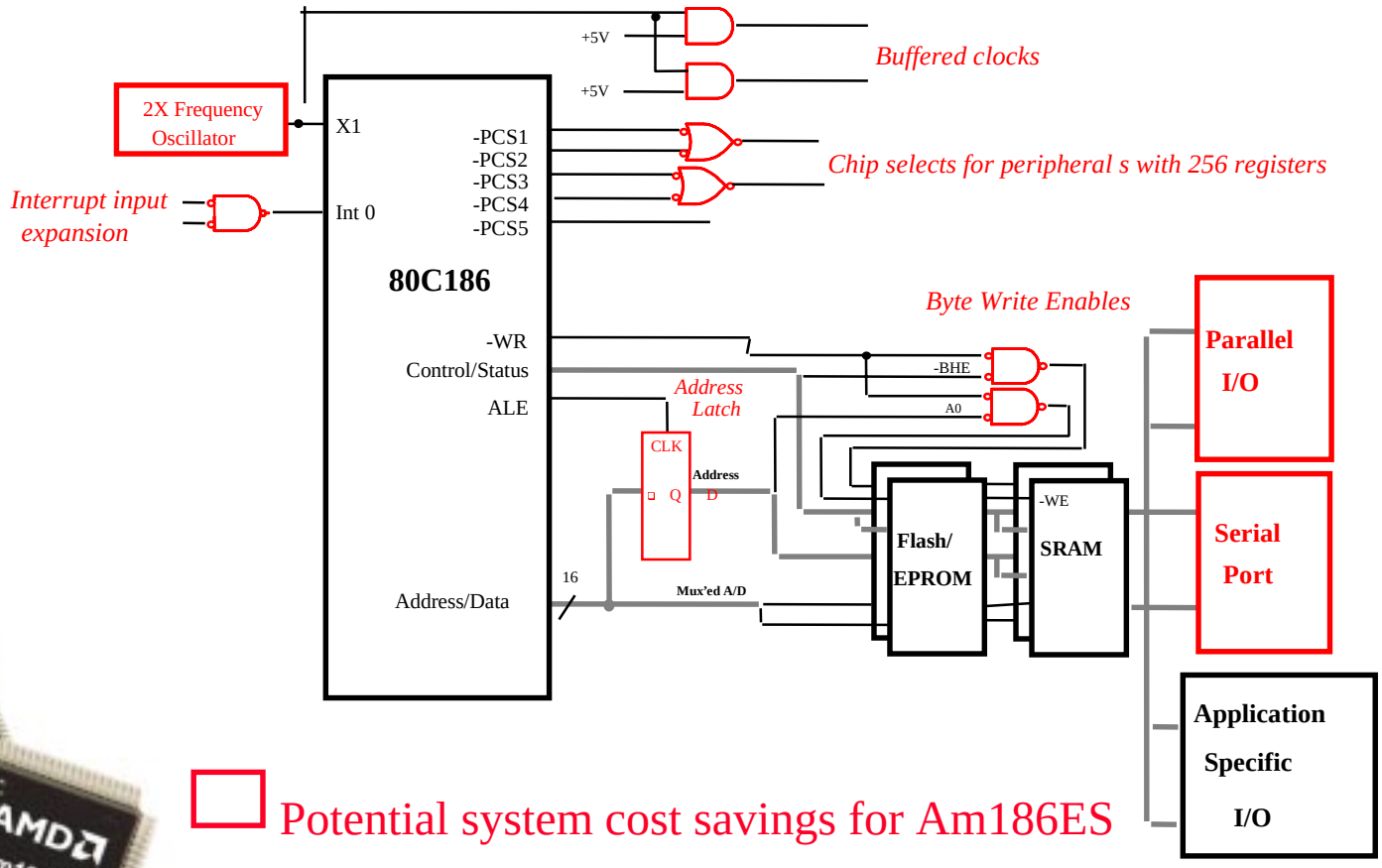
VAX MIPs based on Dhrystone 2.1 using 70ns Memory

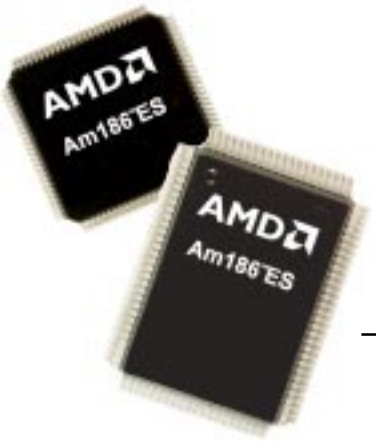




Typical 80C186 Design

Systems in Silicon

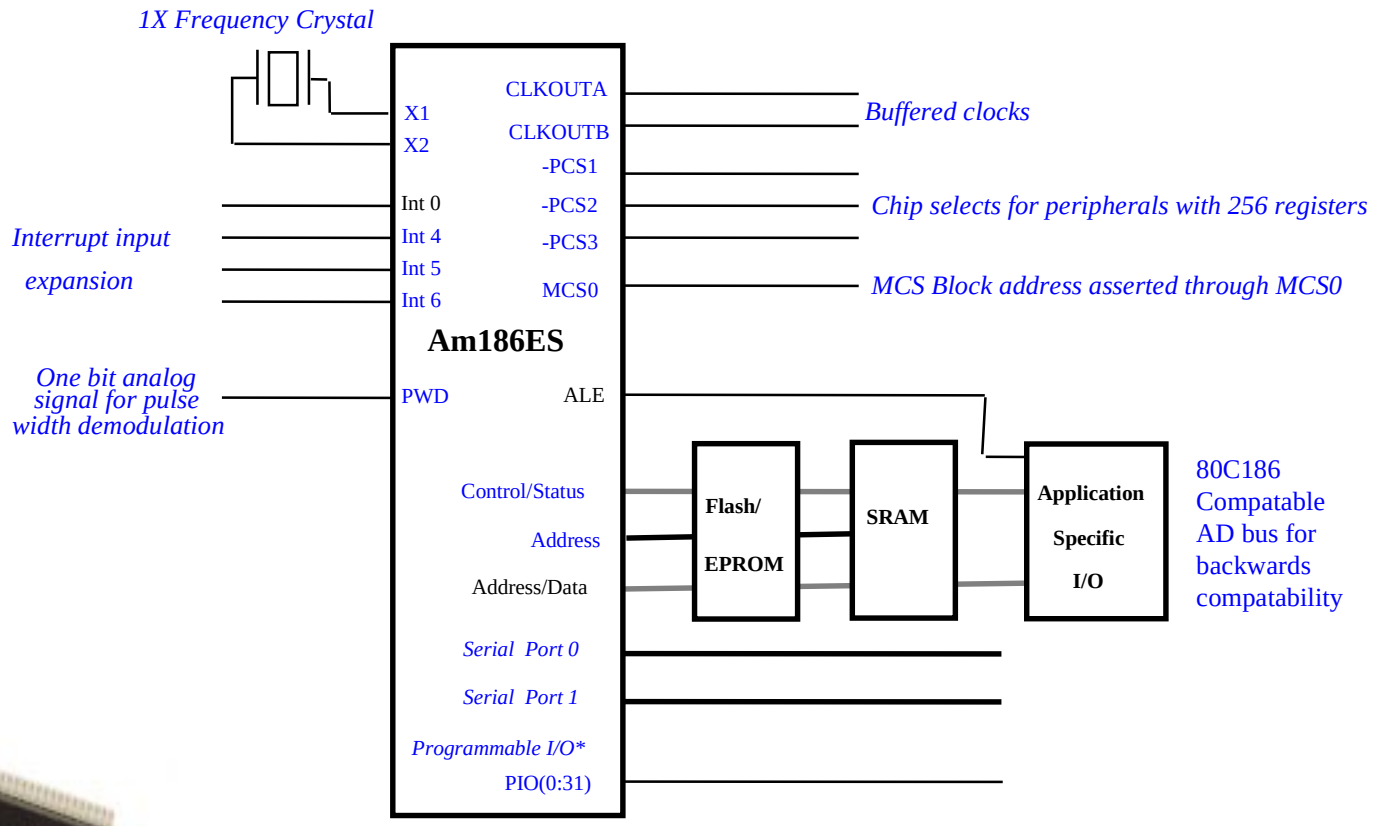


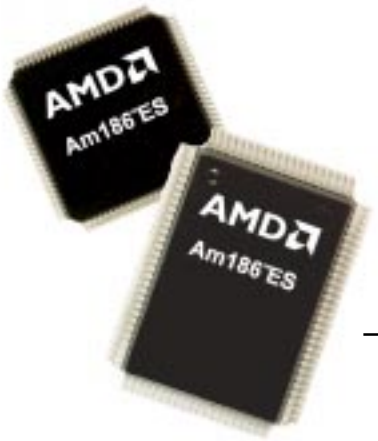


Potential system cost savings for Am186ES

Glueless System Bus

Systems in Silicon



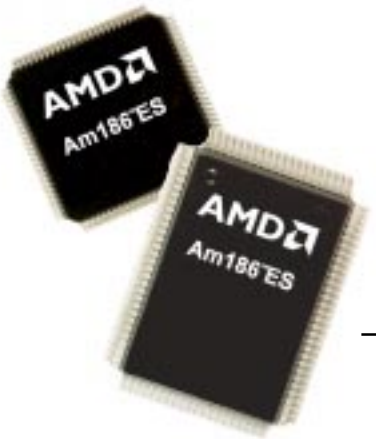


New or Enhanced Features

*16 bit reset configuration latch on AD15-AD0 and up to 32 general purpose programmable I/Os

Dual Asynchronous Serial Port

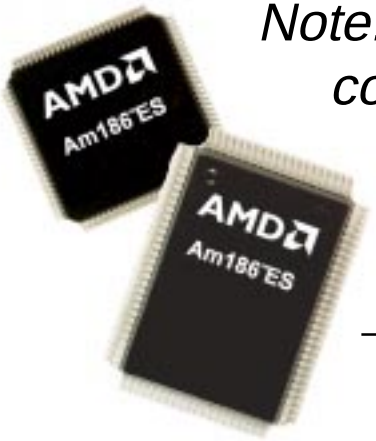
- Four data modes
  - includes multi-drop capability
- Hardware handshaking optional
- Independently enable interrupts for
  - Transmit ready
  - Receive ready
  - Break character detection, parity, framing, or overrun error



DMA to-and-from Serial Ports

- Frees the CPU from handling routine serial port receive and transmit
- DMA controller performs transfers between a data buffer(in memory or I/O space) and a serial port peripheral control register
  - Supports one serial port channel in full duplex or two channels in half duplex

Note: When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated.

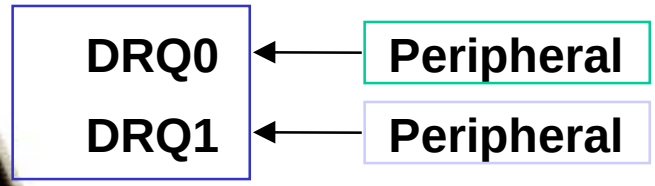


Systems in Silicon

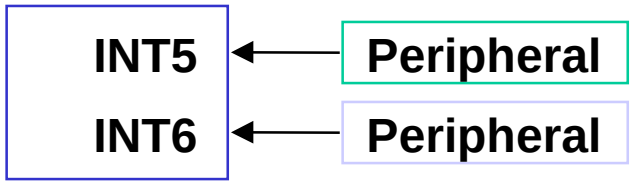
INT5 and INT6

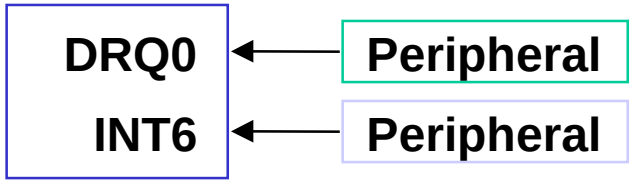
- Internal DMA and external INT5 & INT6 multiplexed together.
- Interrupt service routine can be written to handle just DMA interrupts, just external interrupts or both.

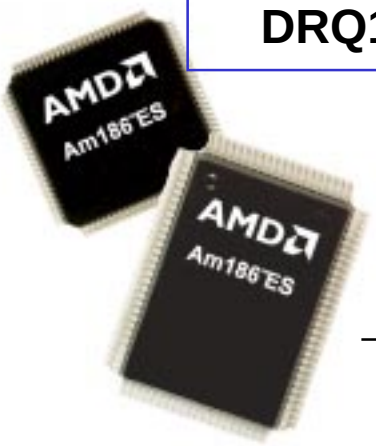
80C186 Computability Mode



New Expanded Interrupts



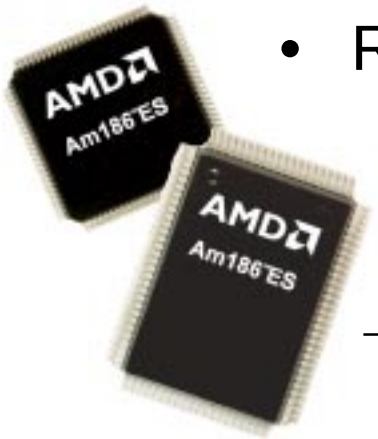




Systems in Silicon

32 Programmable I/O Pins

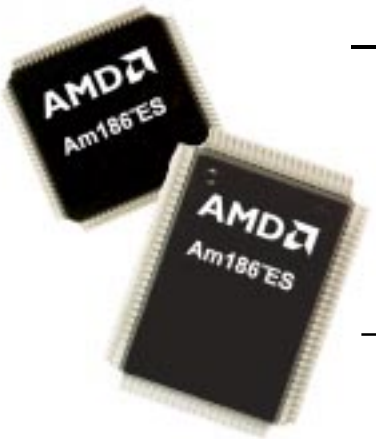
- Up to 32 PIO pins are available for I/O
  - Input
  - Input with weak internal pull-up/pull-down
    - polarity depends on original pin
  - Output
  - Open-drain output
- Multiplexed with other signals
  - Default depends on pin
- Read or written through the peripheral control block



Systems in Silicon

Chip Selects

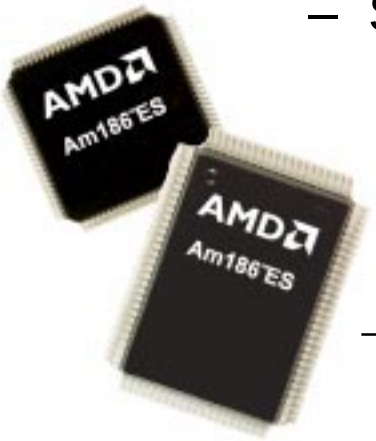
- 6 chip-selects (PCS) with a range of 256 bytes for use with peripheral devices
  - Mapped to memory or I/O space
- 4 chip-selects (MCS) with a range of 2K to 128Kbytes
- 2 chip select outputs (UCS and LCS) for use in the top and bottom of memory map
  - Good for system code and external RAM
  - UCS is initial chip select after reset



Systems in Silicon

Peripheral Chip Select Unit

- Each PCS covers a range of 256 bytes
  - 80C186 range is 128 bytes
- 6 PCS pins are provided
- Mapped to peripheral or I/O space
- PCS3 - PCS0 have 0,1,2,3,5,7,9,15 wait states or external ready
  - 80C186 range is 0,1,2, 3 or external ready
  - Simplifies peripheral connections at higher frequencies



Unified MCS Mode

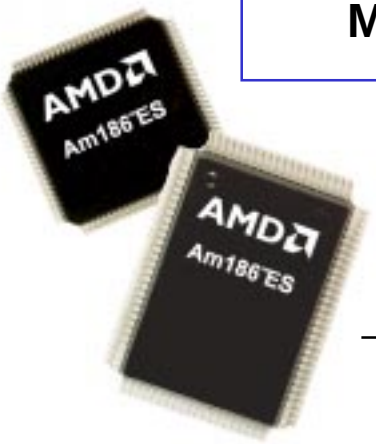
- **Programmable choice to have entire Middle Chip Select memory block space assert through MCS0 or have it divided into four equal parts for MCS0-MCS3.**

80C186 Computability Mode

MCS0	→	Memory
MCS1	→	Peripheral
MCS2	→	Peripheral
MCS3	→	Memory

New Unified MCS Mode

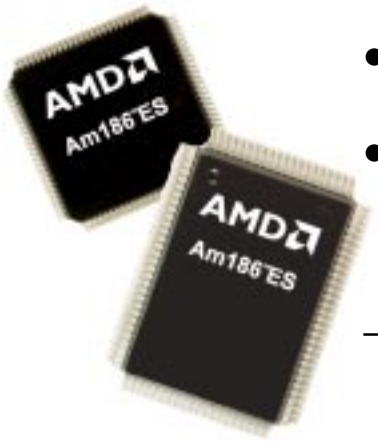
MCS0	→	Memory
MCS1	↔	Programmable I/O
MCS2	↔	Programmable I/O
MCS3	↔	Programmable I/O or PSRAM refresh



Systems in Silicon

PIC - Peripheral Interrupt Controller

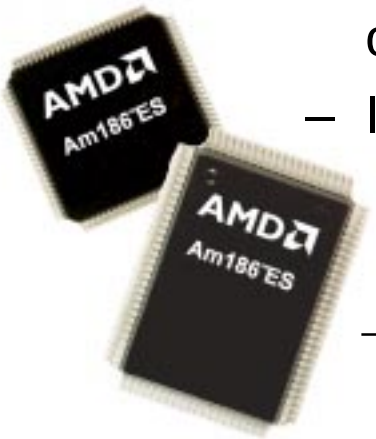
- Total of 16 interrupts
  - 8 internal interrupts
    - 3 timer interrupts
      - watchdog timer interrupt
    - 2 DMA interrupts
    - 2 asynchronous serial port interrupt
  - 8 external interrupts
    - 7 maskable interrupt pins
    - 1 nonmaskable interrupt pin
- Edge or level sensitive
- Masked or slave mode options



Systems in Silicon

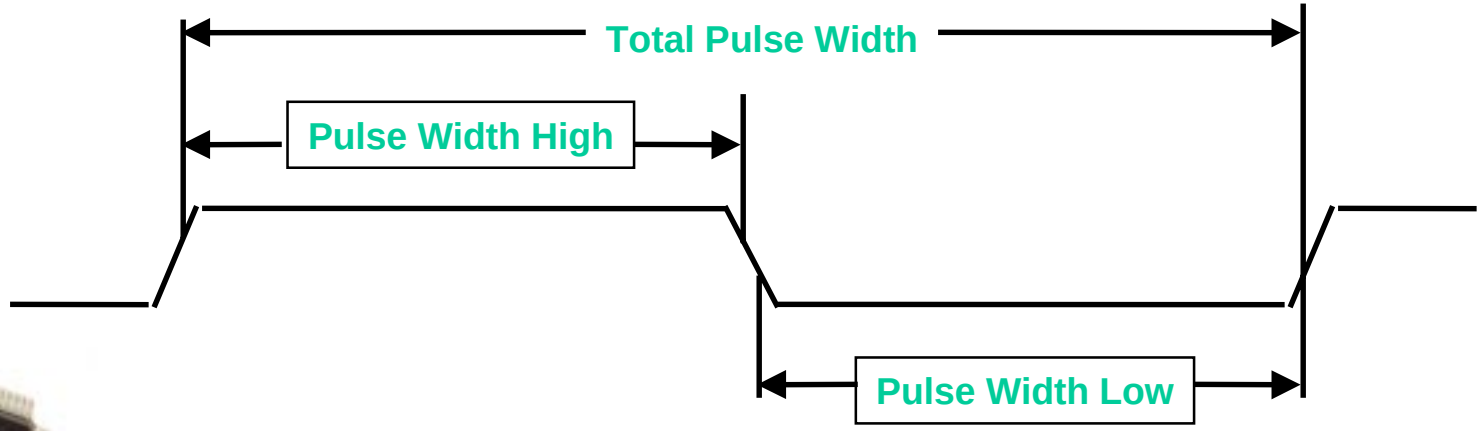
Programmable Bus Sizing

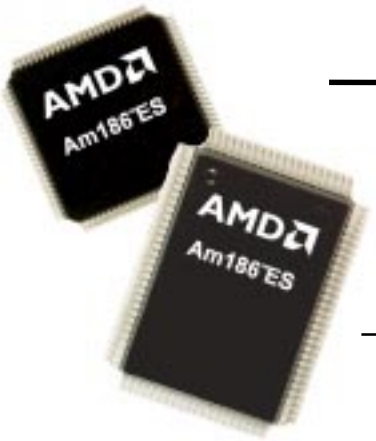
- Allows interface to 8 or 16 bit buses within the same system, independent of software
- Bus width selected by programming internal register
- Bus sizing on Am186ES (Am188ES always 8-bit external)
  - UCS always 16-bit
  - LCS programmable as 8 or 16-bit
  - Memory space that isn't LCS or UCS is programmable as 8 or 16
  - I/O space is programmable as 8 or 16



Pulse Width Demodulation

- Times width of pulses high, low and total.
- Maskable interrupt generated on each edge transition.
- Measurement accuracy to within 4 system clock periods.

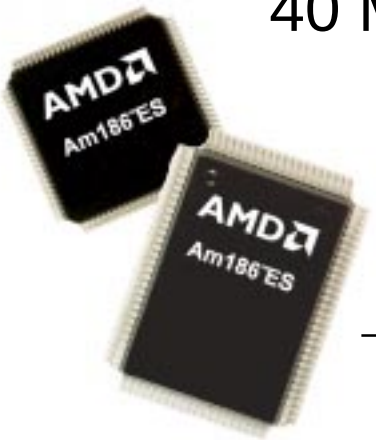




Systems in Silicon

Watchdog Timer

- Watchdog timer provides hardware monitor to prevent errant code from running unchecked
- Special software sequences prevent errant code from changing the watchdog timer
- Selectable choice of non-maskable interrupt or internal reset
- Watchdog counter periods of up to 1.67 seconds at 40 MHz



Options

Am186ES -40 V C \W

DEVICE NUMBER/DESCRIPTION

Am186ES = High-Performance, 10C186-Compatible 16-Bit Embedded Microcontroller with 2 asynch. ports

Am188ES = High-Performance, 80C188-Compatible 16-Bit Embedded Microcontroller with 2 asynch. ports

SPEED OPTION

-20=20MHz

-25=25MHz

-33=33MHz

-40=40MHz

PACKAGE TYPE

V=100-pin thin quad flat pack (TQFP)

K=100-pin plastic quad flat pack(PQFP)

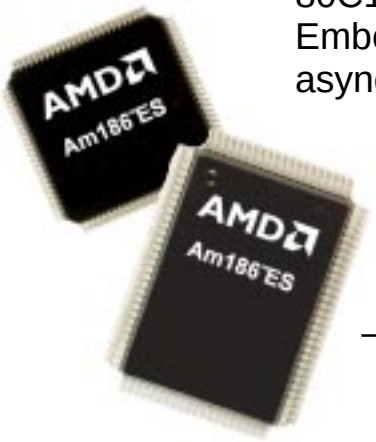
TEMPERATURE RANGE

C = Commercial(Ta = 0 to 70 C)

I = Industrial(Ta = -40 to 85 C)

LEAD FORMING

\W = Trimmed and Formed

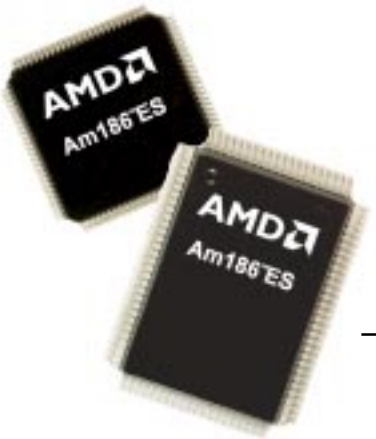


3.3V and Industrial temperature range available in 20 and 25MHz

Systems in Silicon

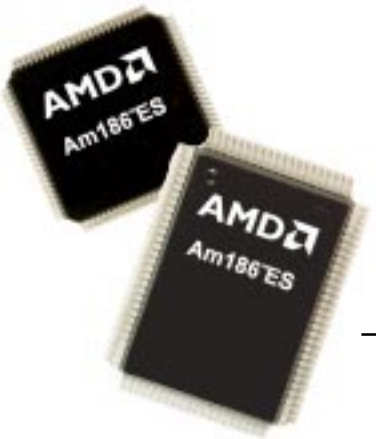
E86 Family Market Opportunities

- 186 upgrades
- 8-bit market
- Market Segments
  - Traditional: Industrial Control, PC Peripheral
  - Office Automation
  - Communications
  - Networking
  - Mass Storage



186 Upgrades

- The Am186ES offers four reasons why a customer would upgrade:
  - Preserve existing software investment
  - Higher integration at same price as the standard 186
  - Higher speed devices (up to 40MHz) with lower systems costs
  - Higher levels of integration



Systems in Silicon

Preserve Existing Software

- Am186ES takes advantage of existing 186 software that customers have developed
- Many customers are already using Microsoft or Borland compilers today and these tools can be used to develop additional code for the E86 family