Application note for using R11xx Ver.B

R11xx is high speed CPU with 3.3 volt power supply. The maximum internal clock is up to 80MHz, so R11 includes the PLL. The PLL default is 1 time factor.
Please note the following description items when using this high speed CPU:

(a) The pins definition of R11xx is same as R88xx.
(b) There is an extra register PLLCON (offset F8h) for R11xx.
The value of the Processor Release Level Register (offset 00F4h) is a new number.
Adding new R3 bit (bit3) in register (offset A0h) for $\overline{UCS}$ inserts more wait states.
Adding new SALEn bit (bit 4) in register (offset F0h) for ALE inserts wait state.
(c) The new release number (value of F4h) :

CPU Type	ID	CPU Type	ID
R1100	C5D9h	R1130	05D9h
R1110	45D9h	R1122	B5D9h
R1120	85D9h		

(d) The I/O pin output is 3.3 volt level and the input is 3.3 volt to 5 volt tolerance.
(e) It need pure and stable 3.3 volt power supply for the CPU. So it need the bypass 0.1uF and 10uF capacitor near each VCC pin.
(f) To select the PLL factor by programming the register PLLCON (offset 0F8h).

- The input clock range : 2 MHz < frequency < 24 MHz
- Example configuration:

Input Clock	Value of 0F8h	Factor	Internal/Output clock
10MHz	0203h	1 **(default)**	10MHz
10MHz	0207h	2	20MHz
10MHz	020Bh	3	30MHz
10MHz	050Fh	4	40MHz
10MHz	0213h	5	50MHz
10MHz	040Bh	6	60MHz
10MHz	040Dh	7	70MHz
10MHz	051Fh	8	80MHz

Input Clock	Value of 0F8h	Factor	Internal/Output clock
20MHz	0203h	1 **(default)**	20MHz
20MHz	0103h	2	40MHz
20MHz	0105h	3	60MHz
20MHz	0107h	4	80MHz

(g) The **PLLCON** register (Offset F8h, reset value is 050Fh) definition:

Bit 15–12 : Reserved

Bit 11–10 : Pre-Divider (PRS) – Programming signals for pre-divider.

Bit 9–8 : Post-Divider (POS) – Programming signals for post-divider.

Bit 7–5 : Reserved

Bit 4–0 : Feedback Divider (FBS) – Programming signals for feedback divider.

$$CLKOUT = FREF * \frac{N}{M * R}$$

(CKOUT : Internal/output frequency, FREF : input frequency)

PRS	M
00	1
01	2
10	3
11	4

POS	R
00	1
01	2
10	4
11	8

FBS	N	FBS	N	FBS	N	FBS	N
00000	1	01000	9	10000	17	11000	25
00001	2	01001	10	10001	18	11001	26
00010	3	01010	11	10010	19	11010	27
00011	4	01011	12	10011	20	11011	28
00100	5	01100	13	10100	21	11100	29
00101	6	01101	14	10101	22	11101	30
00110	7	01110	15	10110	23	11110	31
00111	8	01111	16	10111	24	11111	32

Note1 : 20 MHz < FREF * N / M < 280MHz

Note2 : N=1 : 5 MHz * M <= FREF < 50 MHz,

N=2 : 3.5 MHz * M <= FREF < 50 MHz,

N=3-32 : 2.8 MHz * M<= FREF < 50 MHz

Note3 : The frequency working range of crystal pad is 2 ~ 24 MHz.

(h) **UMCS** Register (Offset A0h,reset value is F033h) definition.

Bit 15: Reserved

Bit 14-12: LB2-LB0

Bit 11-8 :Reserved

Bit 7: DA

Bit 6-4 : Reserved

Bit 3: R3

Bit 2 :R2

Bit 1–0 : R1-R0

UCS_ Wait-State Encoding

R3	R1	R0	Wait States
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3 (Default)
1	0	0	5
1	0	1	7
1	1	0	9
1	1	1	15

(i) **PSCON** Register (Offset F0h, reset value is 0000h) definition.

Bit 15 : PSEN

Bit 14-12: Reserved

Bit 11: CBF

Bit 10: CBD

Bit 9 :CAF

Bit 8 : CAD

Bit 7-4 :Reserved

Bit 3: SALEn, ALE inserts wait state.

Set to 0 : ALE without wait state

Set to 1 : one more T1 is added, bus should be 5T cycle

Bit 2-0 : F2-F0.