R1100
Datasheet
16-BIT RISC MICROCONTROLLER

RDC ***RISC DSP Communication***

RDC Semiconductor Co., Ltd

http://www.rdc.com.tw

TEL: 886-3-666-2866

FAX: 886-3-563-1498

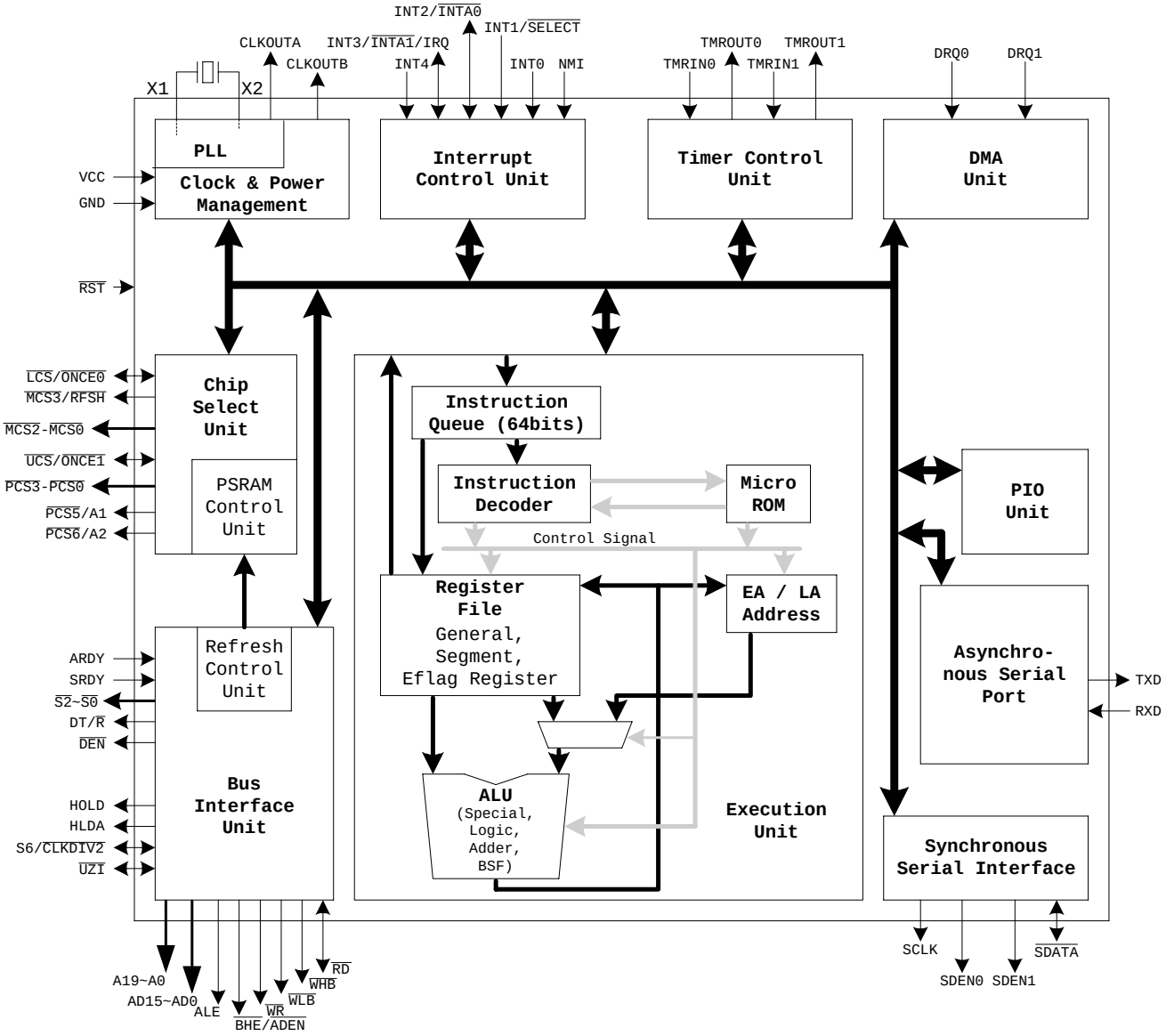
CONTENTS

High Speed 16-Bit Microcontroller

1. Features

- **CPU Core**
  - RDC's proprietary RISC architecture
  - Five-stages pipeline
  - Operation frequency: 80MHz
  - Support CPU ID
  - Supports 32 PIO pins
  - External bus, Internal bus and core in the same clock base
- **Bus interface**
  - Multiplexed address and Data bus
  - With 8-bit or 16-bit boot ROM bus size
  - Supports direct address bus [A19 : A0]
  - 8-bit or 16-bit external bus dynamic access
- **ROM/RAM/DRAM Controller and Addressing Space**
  - 1M byte memory address space
  - 64K byte I/O space
- **Software**
  - Software compatible with generic 80C186 microprocessor
- **Asynchronous Serial Channels**
  - Support two Asynchronous serial channels with hardware handshaking signals.
- **Interrupt Controller**
  - The interrupt controller with seven maskable external interrupts and one non-maskable external interrupt (NMI)
- **Two Independent DMA Channels**
- **Integrate PLL(*1~*8)**
- **Programmable Chip-select Logic**
  - Programmable chip-select logic for Memory or I/O bus cycle decoder
- **Programmable Wait-state Generator**
- **Counter/Timers**
  - Three independent 16-bit timers and one independent programmable watchdog timer
- **Operating Voltage Range**
  - Operation voltage: 3.3V
  - I/O pin input voltage: 3.3V ~ 5V
  - I/O pin output voltage: 3.3V
- **Package Type**
  - 100-pin PQFP
  - 100-pin LQFP

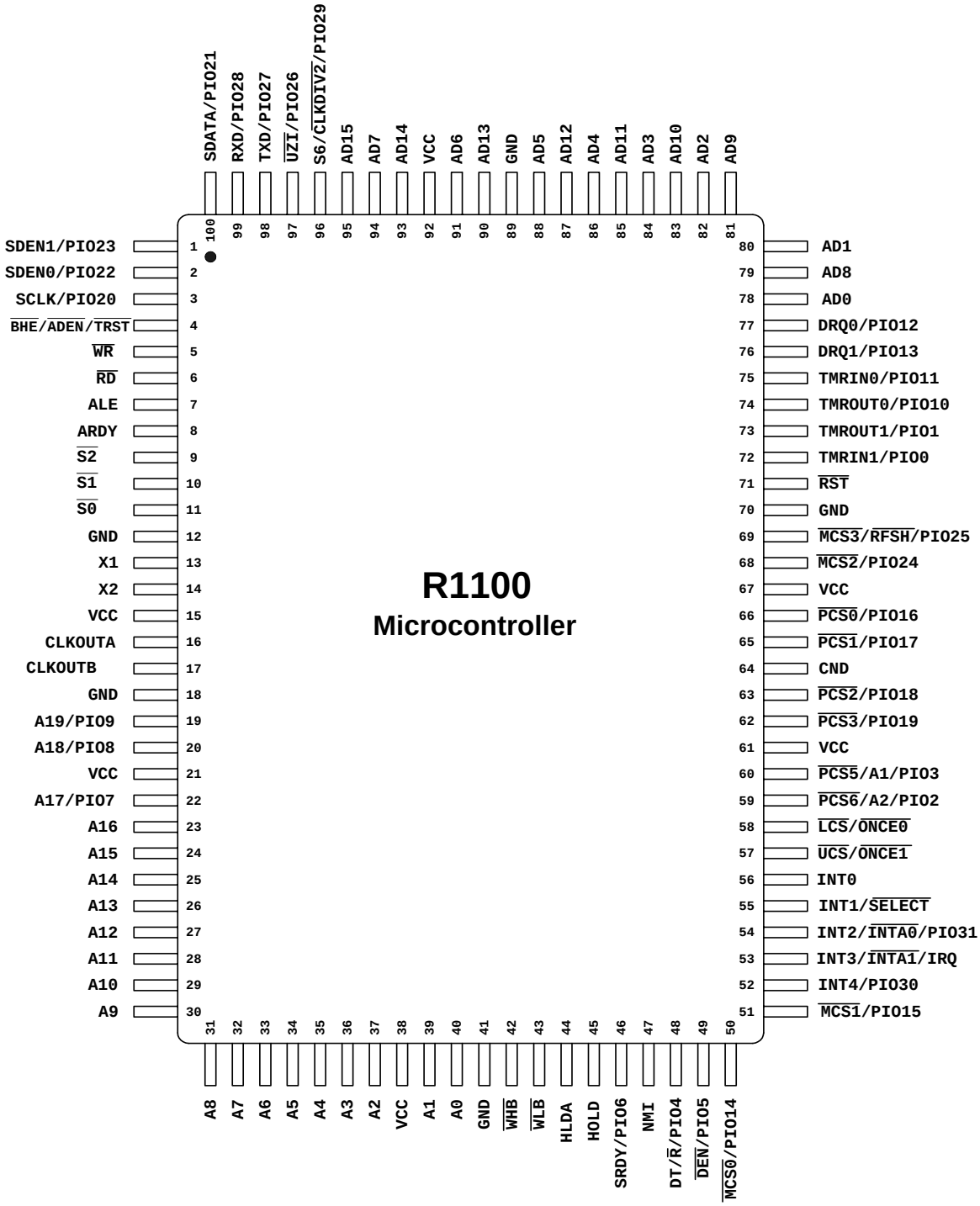
2. Block Diagram



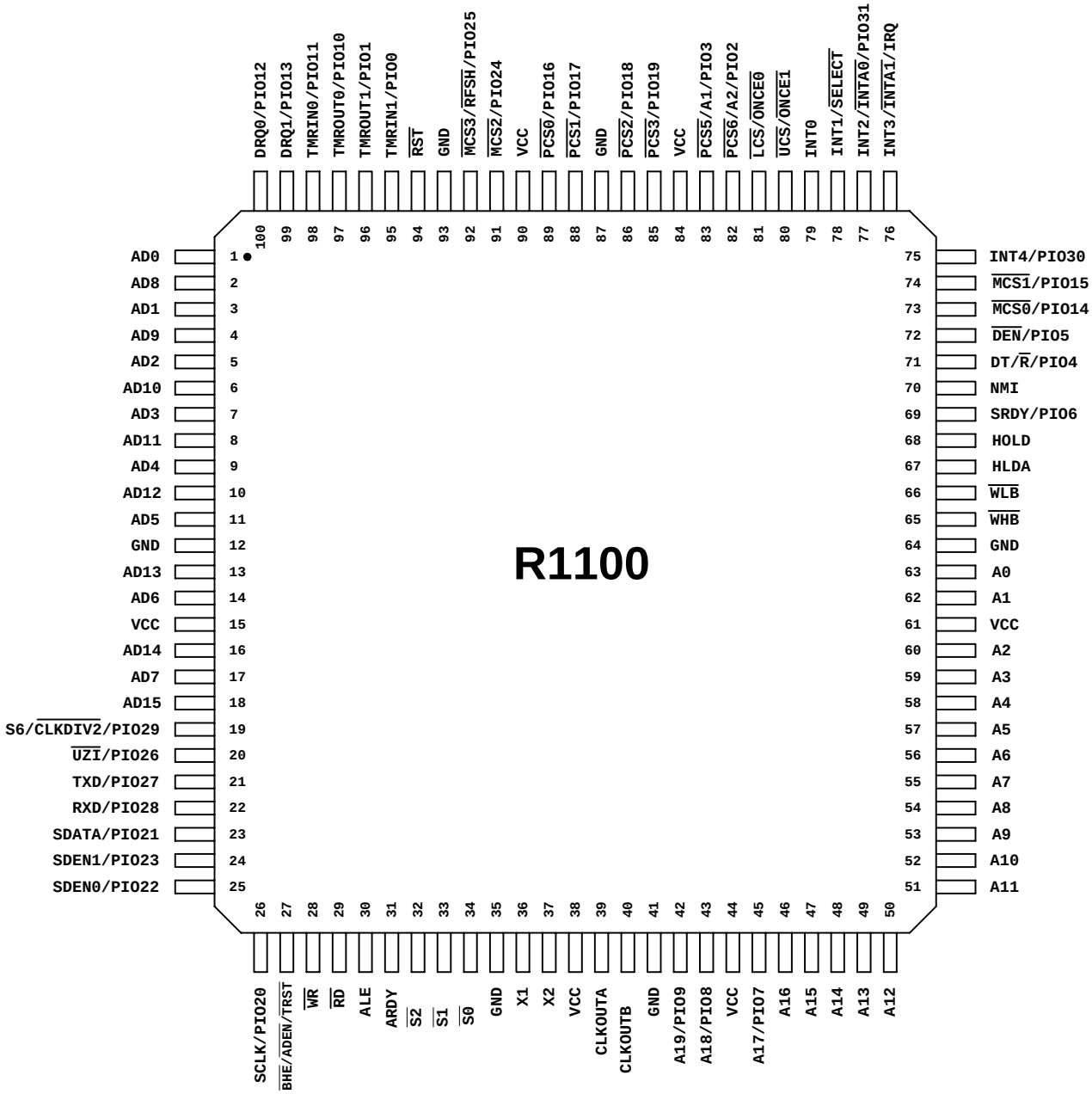
3. Pin Description

3.1 Pin Placement

3.1.1 PQFP



3.1.2 LQFP


R1100
1 AD0
2 AD8
3 AD1
4 AD9
5 AD2
6 AD10
7 AD3
8 AD11
9 AD4
10 AD12
11 AD5
12 GND
13 AD13
14 AD6
15 VCC
16 AD14
17 AD7
18 AD15
19 S6/CLKDIV2/PIO29
20 UZI/PIO26
21 TXD/PIO27
22 RXD/PIO28
23 SDATA/PIO21
24 SDEN1/PIO23
25 SDEN0/PIO22
26 SCLK/PIO20
27 BHE/ADEN/TRST
28 WR
29 RD
30 ALE
31 ARDY
32 S2
33 S1
34 S0
35 GND
36 X1
37 X2
38 VCC
39 CLKOUTA
40 CLKOUTB
41 GND
42 A19/PIO9
43 A18/PIO8
44 VCC
45 A17/PIO7
46 A16
47 A15
48 A14
49 A13
50 A12
51 A11
52 A10
53 A9
54 A8
55 A7
56 A6
57 A5
58 A4
59 A3
60 A2
61 VCC
62 A1
63 A0
64 GND
65 WHB
66 WLB
67 HLDA
68 HOLD
69 SRDY/PIO6
70 NMI
71 DT/R/PIO4
72 DEN/PIO5
73 MCS0/PIO14
74 MCS1/PIO15
75 INT4/PIO30
76 INT3/INTA1/IRQ
77 INT2/INTA0/PIO31
78 INT1/SELECT
79 INT0
80 UCS/ONCE1
81 LCS/ONCE0
82 PCS6/A2/PIO2
83 PCS5/A1/PIO3
84 VCC
85 PCS3/PIO19
86 PCS2/PIO18
87 GND
88 PCS1/PIO17
89 PCS0/PIO16
90 VCC
91 MCS2/PIO24
92 MCS3/RFSH/PIO25
93 GND
94 RST
95 TMRIN1/PIO0
96 TMROUT1/PIO1
97 TMROUT0/PIO10
98 TMRIN0/PIO11
99 DRQ1/PIO13
100 DRQ0/PIO12

3.2 R1100 PQFP & LQFP Pin-Out Table

Pin Name	LQFP Pin No.	PQFP Pin No.	Pin Name	LQFP Pin No.	PQFP Pin No.
AD0	1	78	A11	51	28
AD8	2	79	A10	52	29
AD1	3	80	A9	53	30
AD9	4	81	A8	54	31
AD2	5	82	A7	55	32
AD10	6	83	A6	56	33
AD3	7	84	A5	57	34
AD11	8	85	A4	58	35
AD4	9	86	A3	59	36
AD12	10	87	A2	60	37
AD5	11	88	VCC	61	38
GND	12	89	A1	62	39
AD13	13	90	A0	63	40
AD6	14	91	GND	64	41
VCC	15	92	$\overline{WHB}$	65	42
AD14	16	93	$\overline{WLB}$	66	43
AD7	17	94	HLDA	67	44
AD15	18	95	HOLD	68	45
S6/ $\overline{UZI}$ /PIO29	19	96	SRDY/PIO6	69	46
$\overline{UZI}$/PIO26	20	97	NMI	70	47
TXD/PIO27	21	98	DT/ $\overline{R}$ /PIO4	70	48
RXD/PIO28	22	99	$\overline{DEN}$ /PIO5	72	49
SDATA/PIO21	23	100	$\overline{MCS0}$ /PIO14	73	50
SDEN1/PIO23	24	1	$\overline{MCS1}$ /PIO15	74	51
SDEN0/PIO22	25	2	I NT4/ PIO30	75	52
SCLK/PIO20	26	3	I NT3/ $\overline{INTA1}$ /I RQ	76	53
$\overline{BHE}$ / $\overline{ADEN}$/ $\overline{TRST}$	27	4	I NT2/ $\overline{INTA0}$ /PIO31	77	54
$\overline{WR}$	28	5	I NT1/ $\overline{SELECT}$	78	55
$\overline{RD}$	29	6	I NT0	79	56
ALE	30	7	$\overline{UCS}$/ $\overline{CNCE1}$	80	57
ARDY	31	8	$\overline{LCS}$/ $\overline{CNCE0}$	81	58
$\overline{S2}$	32	9	$\overline{PCS6}$ /A2/PIO2	82	59
$\overline{S1}$	33	10	$\overline{PCS5}$ /A1/PIO3	83	60
$\overline{S0}$	34	11	VCC	84	31
GND	35	12	$\overline{PCS3}$/PIO19	85	62
X1	36	13	$\overline{PCS2}$ /PIO18	86	63
X2	37	14	GND	87	64

VCC	38	15	$\overline{PCS1}$/PIO17	88	65
CLKOUTA	39	16	$\overline{PCS0}$/PIO16	89	66
CLKOUTB	40	17	VCC	90	67
GND	41	18	$\overline{MCS2}$/PI O24	91	68
A19/PIO9	42	19	$\overline{MCS3}$/ $\overline{RFSH}$/PIO25	92	69
A18/PIO8	43	20	GND	93	70
VCC	44	21	$\overline{RST}$	94	71
A17/PIO7	45	22	TMRI N1/PIO0	95	72
A16	46	23	TMROUT1/PIO1	96	73
A15	47	24	TMROUT0/PIO10	97	74
A14	48	25	TMRI N0/PIO11	98	75
A13	49	26	DRQ1/PIO13	99	76
A12	50	27	DRQ0/PIO12	100	77

3.3 Functional Description

I = Input;

O = Output;

● CPU Core

PIN No. (PQFP)	Symbol	Type	Description
15, 21, 38, 61, 67, 92	VCC	I	System power: +3.3 volt power supply.
12, 18, 41, 64, 70, 89	GND	I	System ground.
71	$\overline{RST}$	I*	Reset input. When $\overline{RST}$ is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and the address transfers to the reset address FFFF0h.
13	X1	I	Input to the oscillator amplifier.
14	X2	O	Output from the inverted oscillator amplifier.
16	CLKOUTA	O	Clock output A. The CLKOUTA operation is the same as crystal input frequency (X1). CLKOUTA remains active during reset and bus hold conditions.
17	CLKOUTB	O	Clock output B. The CLKOUTB operation is the same as crystal input frequency (X1). CLKOUTB remains active during reset and bus hold conditions. When enable the JTAG interface,this pin is active for TDI.

● Synchronous Serial Port Interface

PIN No. (PQFP)	Symbol	Type	Description
1 2	SDEN1/PIO23 SDEN0/PIO22	O/I	Serial data enables. Active-high. These pins enable data transfers of the synchronous serial interface. SDEN1 for port1, SDEN0 for port0.
3	SCLK/PIO20	O/I	Synchronous serial data clock. This pin provides the shift clock to an external device. SCLK=X1/2, 4, 8 or 16 depending on register setting. This pin held high during the UART inactive.
100	SDATA/PIO21	I/O	Synchronous serial data. This pin provides the shift data to or receives a serial data from an external device.

● Asynchronous Serial Port Interface

PIN No. (PQFP)	Symbol	Type	Description
98	TXD/PIO27	O/I	Transmit data. This pin transmits asynchronous serial data from the UART of the microcontroller.
99	RXD	I	Receive data. This pin receives asynchronous serial data.

Bus Interface

<table>
<tr><th>PIN No. (PQFP)</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>4</td><td>$\overline{BHE}$ / $\overline{ADEN}$ / $\overline{TRST}$</td><td>O/I</td><td>Bus high enable/address enable. During a memory access, the $\overline{BHE}$ and (AD0 or A0) encodings indicate what type of the bus cycle. $\overline{BHE}$ is asserted during T1 and keeps the asserted to T3 and Tw. This pin is floating during bus hold and reset.
$\overline{BHE}$ and (AD0 or A0) Encodings
<table>
<tr><th>$\overline{BHE}$</th><th>AD0 or A0</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>High byte transfer (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Low byte transfer (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Refresh</td></tr>
</table>
The address portion of the AD bus can be enabled or disabled by DA bit in the LMCS and UMCS register during LCS or UCS bus cycle access, if $\overline{BHE}$ / $\overline{ADEN}$ is held high during power-on reset. The $\overline{BHE}$ / $\overline{ADEN}$ with an internal weak pull-up register, so no external pull-up register is required. The AD bus always drives both address and data during LCS or UCS bus cycle access, if the $\overline{BHE}$ / $\overline{ADEN}$ pin with external pull-low resister during reset.
This pin is active as $\overline{TRST}$ when JTAG interface is enabled.</td></tr>
<tr><td>5</td><td>$\overline{WR}$</td><td>O</td><td>Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active during T2, T3 and Tw of any write cycle, floats during a bus hold or reset.</td></tr>
<tr><td>6</td><td>$\overline{RD}$</td><td>O</td><td>Read Strobe. Active low signal which indicates that the microcontroller is performing a memory or I/O read cycle. $\overline{RD}$ Floats during bus hold or reset.</td></tr>
<tr><td>7</td><td>ALE</td><td>O</td><td>Address latch enable. Active high. This pin indicates that an address output on the AD bus. Address is guaranteed to be valid on the trailing edge of ALE. This pin is tri-stated during ONCE mode and is never floating during a bus hold or reset.</td></tr>
<tr><td>8</td><td>ARDY</td><td>I</td><td>Asynchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active high. The falling edge of ARDY must be synchronized to CLKOUTA. Tie ARDY high, the microcontroller is always asserted in the ready condition. If the ARDY is not used, tie this pin low to yield control to SRDY.
Both SRDY and ARDY should be tied to high if the system need not assert wait state by externality.</td></tr>
</table>

<table>
<tr><td rowspan="2">9
10
11</td><td rowspan="2">$\overline{S2}$
$\overline{S1}$
$\overline{S0}$</td><td rowspan="2">O</td><td>Bus cycle status. These pins are encoded to indicate the bus status. $\overline{S2}$ can be used as memory or I/O indicator. $\overline{S1}$ can be used as DT/$\overline{R}$ indicator. These pins are floating during hold and reset.</td></tr>
<tr><td>Bus Cycle Encoding Description
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>19
20
22
23-37
39, 40</td><td>A19/PIO9
A18/PIO8
A17/PIO7
A16-A2
A1 , A0</td><td>O/I</td><td>Address bus. Non-multiplexed memory or I/O address. The A bus is one-half of a CLKOUTA period earlier than the AD bus. These pins are high-impedance during bus hold or reset.</td></tr>
<tr><td>78,80,82,84,
86,88
91,94
79,81,83,85,
87,90
93,95</td><td>AD0-AD7

AD8-AD15</td><td>I/O</td><td>The multiplexed address and data bus for memory or I/O accessing. The address is present during the t1 clock phase, and the data bus phase is in t2-t4 cycle.
The address phase of the AD bus can be disabled when the $\overline{BHE}$ / $\overline{ADEN}$ pin with external pull-low resister during reset.
The AD bus is in high-impedance state during bus hold or reset condition and this bus also be used to load system configuration information (with pull-up or pull-Low resister) into the F6h register when the reset input from low go high.</td></tr>
<tr><td>42</td><td>$\overline{WHB}$</td><td>O</td><td>Write high byte. This pin indicates the high byte data (AD15-AD8) on the bus is to be written to a memory or I/O device.
This pin is floating during reset or bus hold.</td></tr>
<tr><td>43</td><td>$\overline{WLB}$</td><td>O</td><td>Write low byte. This pin indicates the low byte data (AD7-AD0) on the bus is to be written to a memory or I/O device.
This pin is floating during reset or bus hold.</td></tr>
<tr><td>44</td><td>HLDA</td><td>O</td><td>Bus hold acknowledge. Active high. The microcontroller will issue an HLDA in response to a HOLD request by external bus master at the end of T4 or Ti. When the microcontroller is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S0}$ - $\overline{S1}$, $\overline{S6}$, $\overline{BHE}$, DT/ $\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be driven high. After HOLD is detected as being low, the microcontroller will lower HLDA.</td></tr>
<tr><td>45</td><td>HOLD</td><td>I</td><td>Bus Hold request. Active high. This pin indicates that another bus master is requesting the local bus.</td></tr>
<tr><td>46</td><td>SRDY/PIO6</td><td>I/O</td><td>Synchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The SRDY pin accepts a falling edge that is asynchronous to CLKOUTA and is active high. SRDY is accomplished by elimination of the one-half clock period required to internally synchronize ARDY. Tie SRDY high the microcontroller is always asserted in the ready condition. If the SRDY is not used, tie this pin low to yield control to ARDY.
Both SRDY and ARDY should be tied to high if the system doesn't need to assert wait state by externality.</td></tr>
</table>

48	DT/$\overline{R}$ /PIO4	O/I	Data transmit or receive. This pin indicates the direction of data flow through an external data-bus transceiver. DT/ $\overline{R}$ low, the microcontroller receives data. When DT/R is asserted high, the microcontroller writes data to the data bus.
49	$\overline{DEN}$ /PIO5	O/I	Data enable. This pin is provided as a data bus transceiver output enable. $\overline{DEN}$ is asserted during memory and I/O access. $\overline{DEN}$ is driven high when DT/$\overline{R}$ changes state. It is floating during bus hold or reset condition.
96	S6/ $\overline{CLKDIV2}$ /PIO29	O/I	Bus cycle status bit6/clock divided by 2. For S6 feature, this pin is low to indicate a microcontroller-initiated bus cycle or high to indicate a DMA-initiated bus cycle during T2, T3, Tw and T4. For $\overline{CLKDIV2}$ feature. The internal clock of microcontroller is the external clock which divided by 2. (CLKOUTA, CLKOUTB=X1/2), if this pin held low during power-on reset. The pin is sampled on the rising edge of $\overline{RST}$.
97	$\overline{UZI}$ /PIO26	O/I	Upper zero indicate. This pin is the logical OR of the inverted A19-A16. It asserts in the T1 and is held throughout the cycle.

● Chip Select Unit Interface

PIN No. (PQFP)	Symbol	Type	Description
50 51 68 69	$\overline{MCS0}$ /PIO14 $\overline{MCS1}$ /PIO15 $\overline{MCS2}$ /PIO24 $\overline{MCS3}$/ $\overline{RFSH}$ /PIO25	O/I	Midrange memory chip selects. For $\overline{MCS}$ feature, these pins are active low when enable the MMCS(A6h) register to access a memory. The address ranges are programmable. $\overline{MCS3}$ - $\overline{MCS0}$ are held high during bus hold. When programming LMCS(A6h) register, pin69 is as a $\overline{RFSH}$ pin to auto refresh the PSRAM.
57	$\overline{UCS}$ / $\overline{ONCE1}$	O/I	Upper memory chip select/ONCE request 1. For $\overline{UCS}$ feature, this pin acts low when system accesses the defined portion memory block of the upper 512K bytes (80000h-FFFFFh) memory region. $\overline{UCS}$ default acted address region is from F0000h to FFFFFh after power-on reset. The address range acting $\overline{UCS}$ is programmed by software.
58	$\overline{LCS}$ / $\overline{ONCE0}$	O/I	Lower memory chip select/ONCE mode request 0. For $\overline{LCS}$ feature, this pin acts low when the microcontroller accesses the defined portion memory block of the lower 512K (00000h-7FFFFh) memory region. The address range acting $\overline{LCS}$ is programmed by software.
59 60	$\overline{PCS6}$ /A2/PIO2 $\overline{PCS5}$ /A1/PIO3	O/I	Peripheral chip selects/latched address bit. For $\overline{PCS}$ feature, these pins act low when the microcontroller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of $\overline{PCS}$ is programmable. These pins assert with the AD address bus and are not floated during bus hold. For latched address bit feature. These pins output the latched address A2, A1 when cleared the EX bit in the $\overline{MCS}$ and $\overline{PCS}$ auxiliary register. The A2, A1 retains previous latched data during bus hold.

62 63 65 66	$\overline{PCS3}$ /PIO19 $\overline{PCS2}$ /PIO18 $\overline{PCS1}$ /PIO17 $\overline{PCS0}$ /PIO16	O/I	Peripheral chip selects. These pins act low when the microcontroller accesses the defined memory area of the peripheral memory block (I/O or memory address). For I/O accessed, the base address can be programmed in the region 00000h to 0FFFFh. For memory address access, the base address can be located in the 1M byte memory address region. These pins assert with the multiplexed AD address bus and are not floated during bus hold.

● Interrupt Control Unit Interface

PIN No. (PQFP)	Symbol	Type	Description
47	NMI	I	Non-maskable Interrupt. The NMI is the highest priority hardware interrupt and is non-maskable. When this pin is asserted (NMI transition from low to high), the microcontroller always transfers the address bus to the location specified by the non-maskable interrupt vector in the microcontroller interrupt vector table. The NMI pin must be asserted for at least one CLKOUTA period to guarantee that the interrupt is recognized.
52	INT4/PIO30	I/O	Maskable interrupt request 4. Act high. This pin indicates that an interrupt request has occurred. The microcontroller will jump to the INT4 address vector to execute the service routine if the INT4 is enabled. The interrupt input can be configured to be either edge- or level-triggered. The requesting device must hold the INT4 until the request is acknowledged to guarantee interrupt recognition.
53	INT3/ $\overline{INTA1}$ /IRQ	I/O	Maskable interrupt requests 3/interrupt acknowledge 1/slave interrupt request. For INT3 feature, except the difference interrupt line and interrupt address vector, the function of INT3 is the same as INT4. For $\overline{INTA1}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to the INT1. For IRQ feature, when the microcontroller is as a slave device, this pin issues an interrupt request to the master interrupt controller.
54	INT2/ $\overline{INTA0}$ /PIO31	I/O	Maskable interrupt requests 2/interrupt acknowledge 0. For INT2 feature, except the difference interrupt line and interrupt address vector, the function of INT2 is the same as INT4. For $\overline{INTA0}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to the INT0.
55	INT1/ $\overline{SELECT}$	I/O	Maskable interrupt requests 1/slave select. For INT1 feature, except the difference interrupt line and interrupt address vector, the function of INT1 is the same as INT4. For $\overline{SELECT}$ feature, when the microcontroller is as a slave device, this pin is driven from the master interrupt controller decoding. This pin acts to indicate that an interrupt appears on the address and data bus. The INT0 must act before $\overline{SELECT}$ acts when the interrupt type appears on the bus.
56	INT0	I	Maskable interrupt request 0. Except the interrupt line and interrupt address vector, the function of INT0 is the same as INT4.

● Timer Control Unit Interface

PIN No. (PQFP)	Symbol	Type	Description
72 75	TMRIN1/PIO0 TMRIN0/PIO11	I/O	Timer input. These pins can be clock or control signal input, which depend upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. These pins must be pull-up if not being used.
73 74	TMROUT1/PIO1 TMROUT0/PIO10	O/I	Timer output. Depending on timer mode select these pins provide single pulse or continuous waveform. The duty cycle of the waveform can be programmable. These pins are floated during a bus hold or reset.

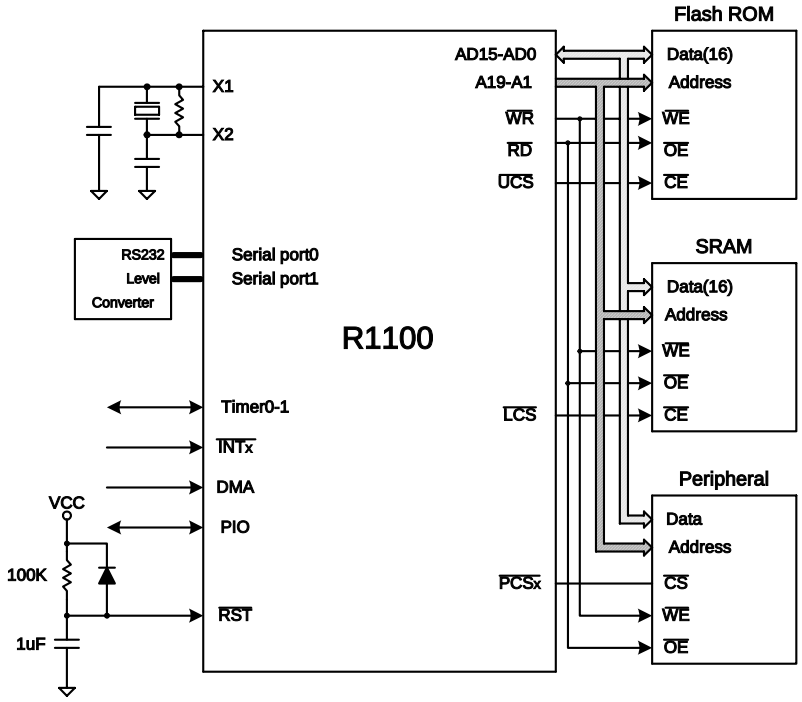
● DMA Unit Interface

PIN No. (PQFP)	Symbol	Type	Description
76 77	DRQ1/PIO13 DRQ0/PIO12	I/O	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals must remain act until finish serviced and are not latched.

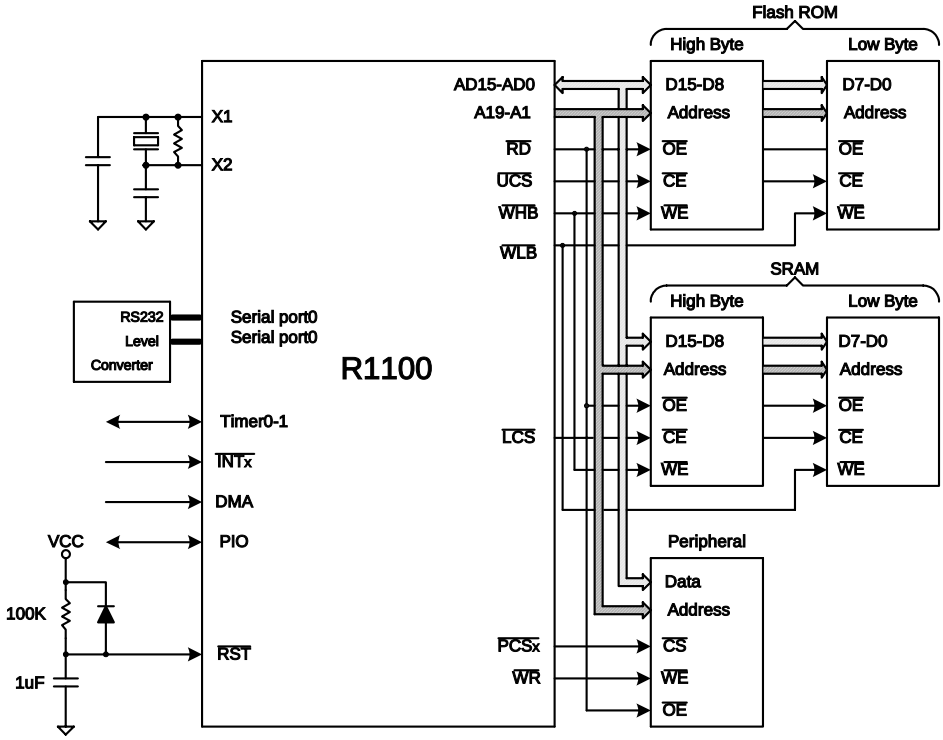
Notes:

1. When enable the PIO Data register, there are 32 MUX definition pins can be a PIO pin. For example, the DRD1/PIO13 (pin76) can be a PIO13 when enable the PIO Data register.
2. The PIO status during Power-On reset: PIO1, PIO10, PIO22, PIO23 are inputted with pull-down, PIO4 to PIO9 are normal operation and the others are inputted with pull-up.

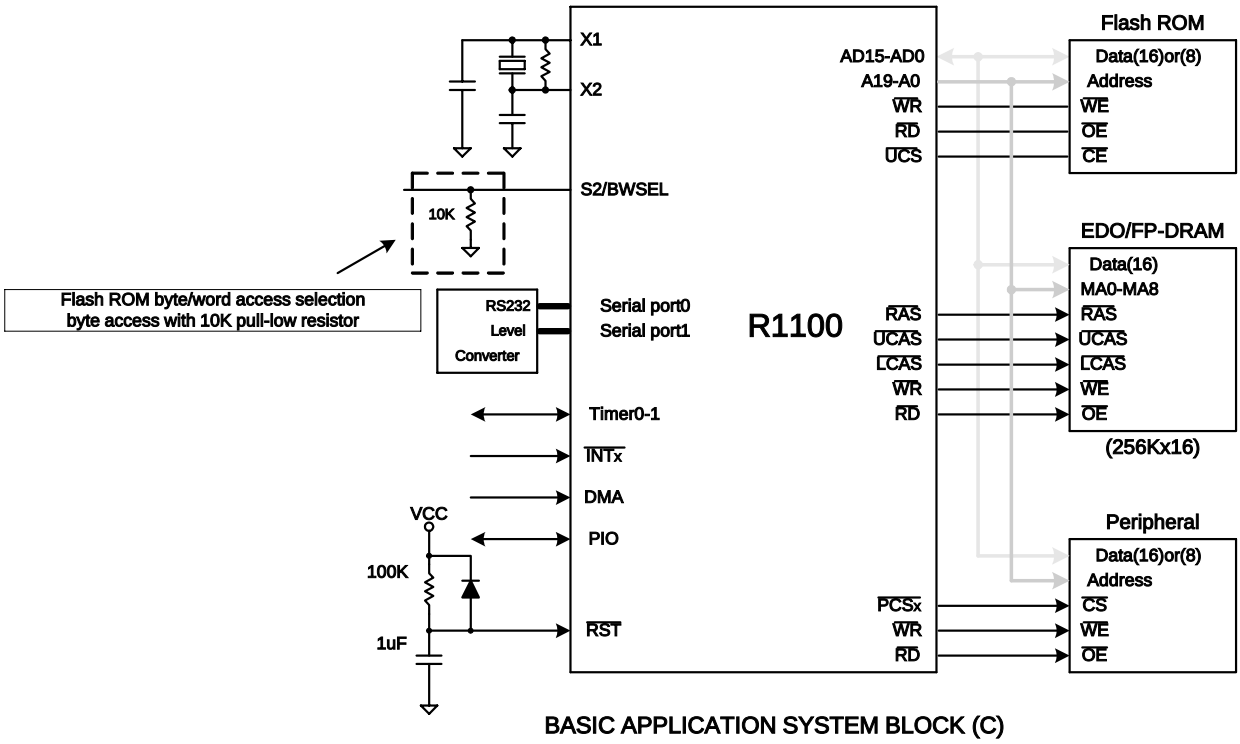
4. Basic Application System Block



BASIC APPLICATION SYSTEM BLOCK (A)

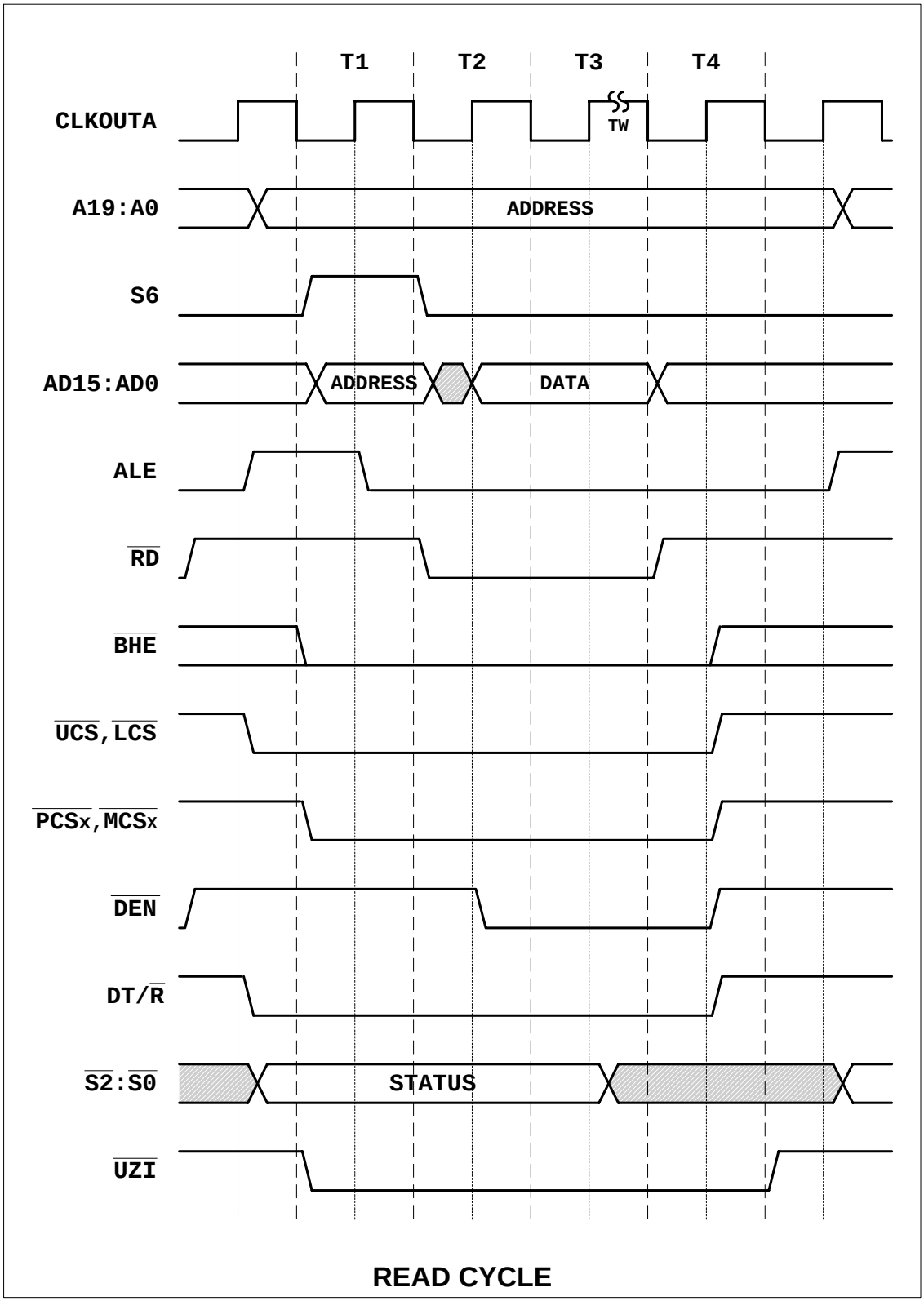


BASIC APPLICATION SYSTEM BLOCK (B)

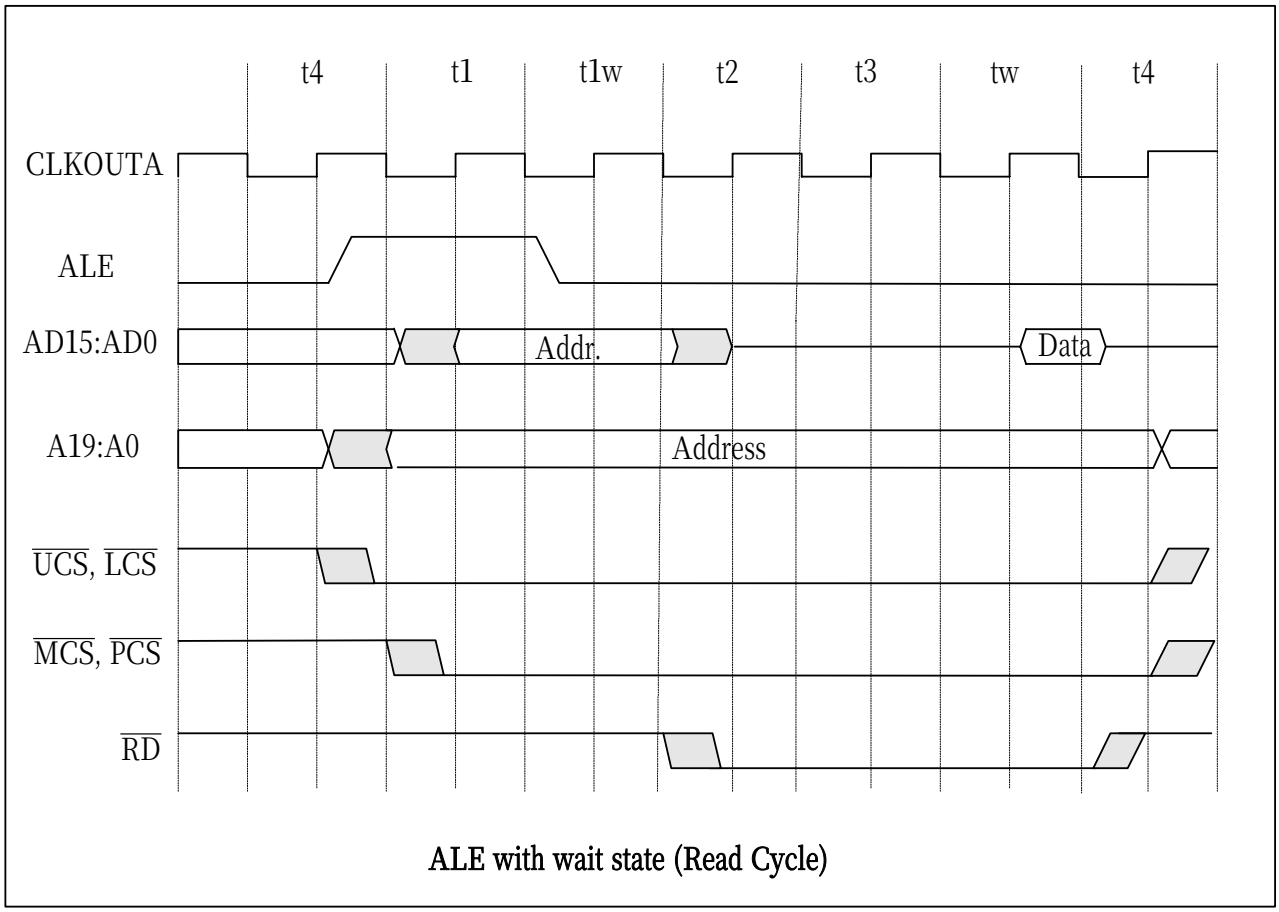


BASIC APPLICATION SYSTEM BLOCK (C)

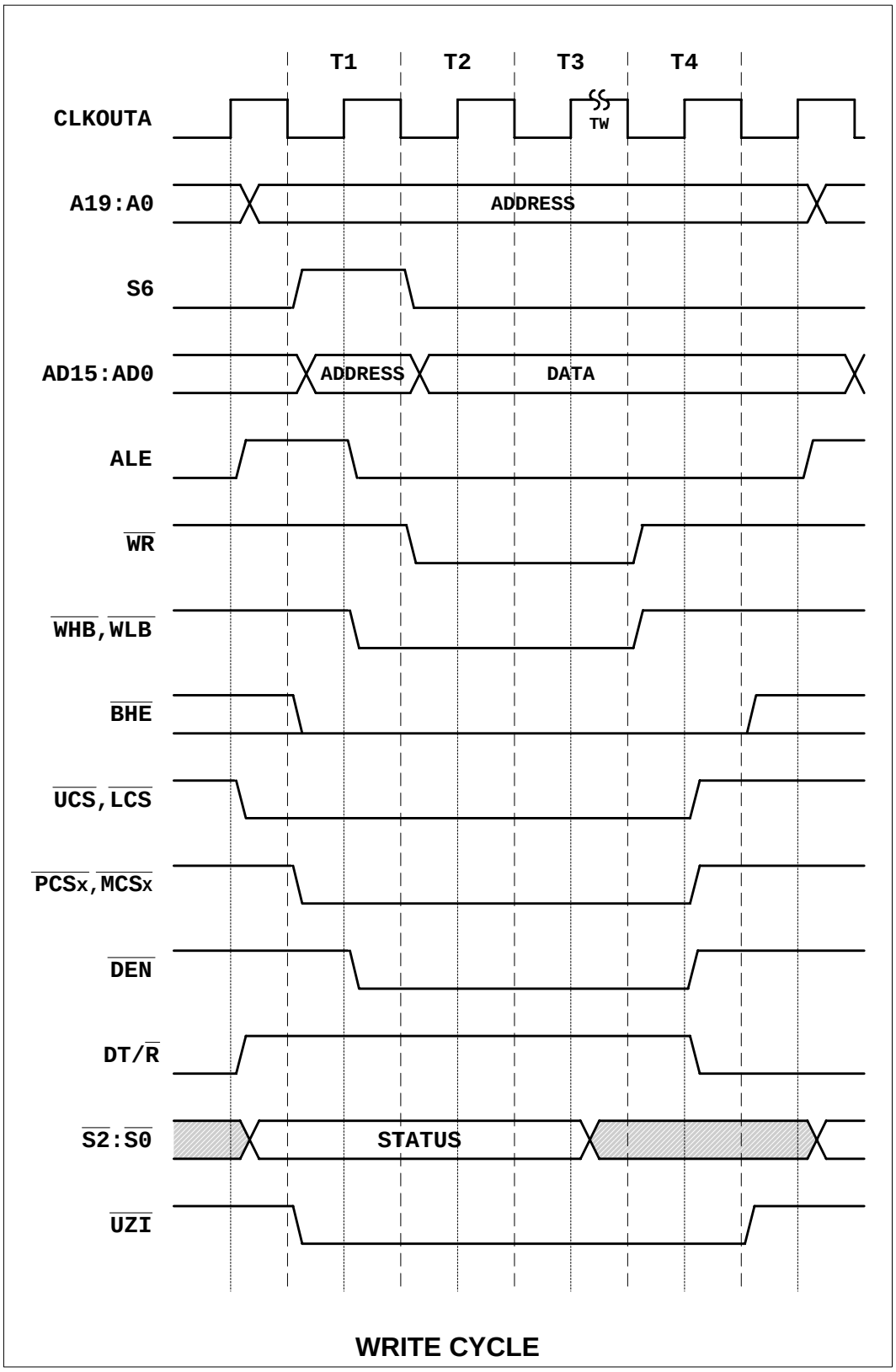
5. Read/Write Timing Diagram



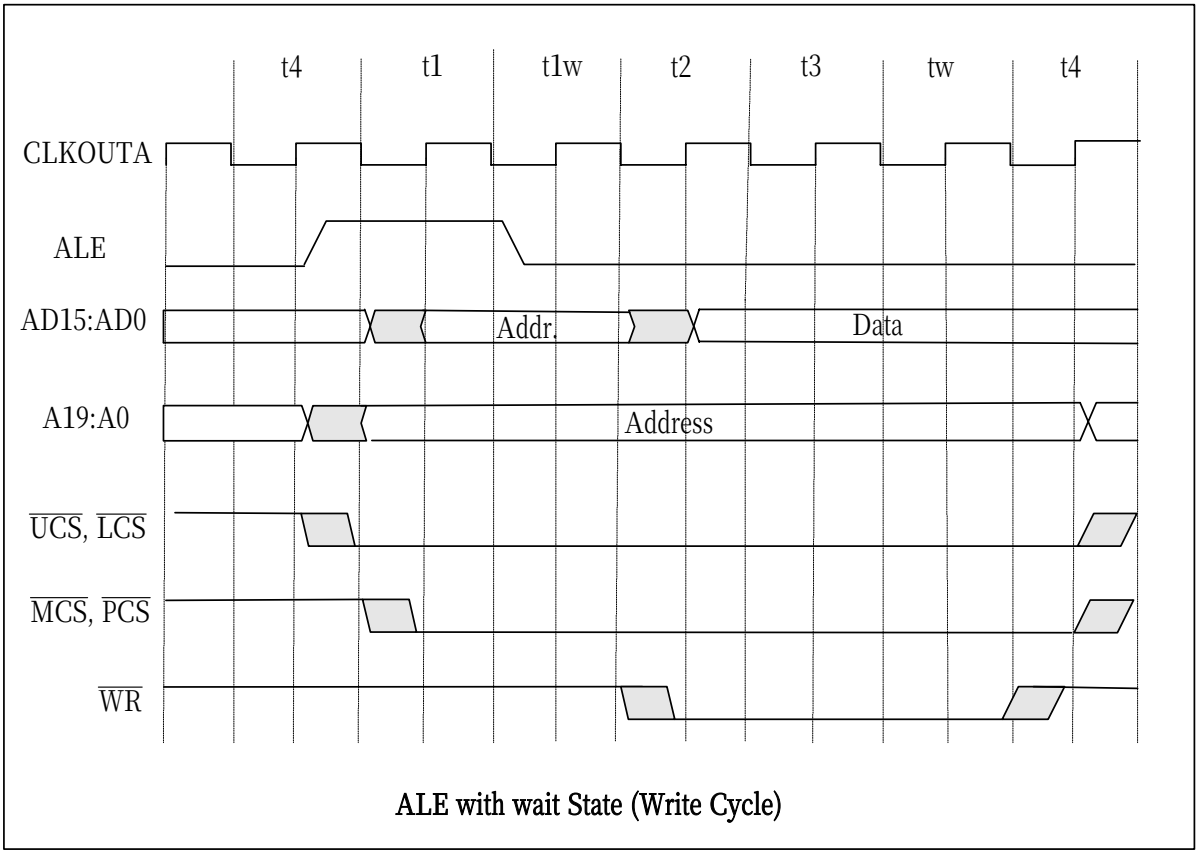
READ CYCLE



ALE with wait state (Read Cycle)

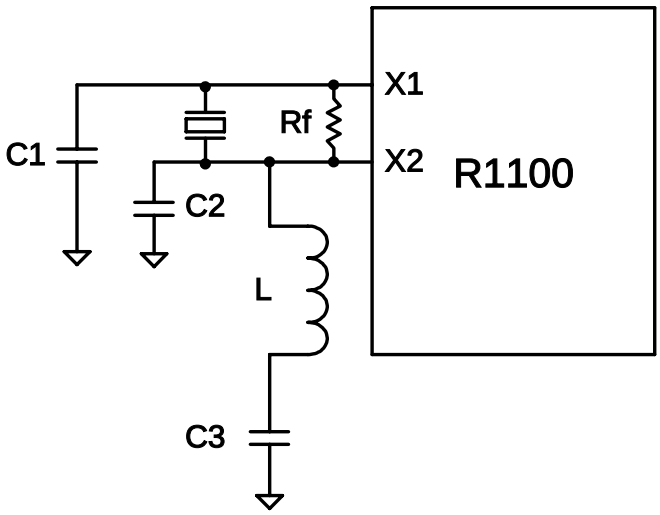

T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB, WLB
BHE
UCS, LCS
PCSx, MCSx
DEN
DT/R
S2:S0
STATUS
UZI

WRITE CYCLE



ALE with wait State (Write Cycle)

6. Oscillator Characteristics



For fundamental-mode crystal:

C1 --- 10pF ± 20% ; C2 --- 10pF ± 20% ; Rf --- Don't care; C3 , L --- Don't care

For third-overtone mode crystal:

C1 --- 20pF ± 20% ; C2 --- 20pF ± 20% ; C3 --- 200pf ; Rf --- 1 mega-ohm

L --- 8.2uH ± 20% (25MHz) , 12uH ± 20% (20MHZ)

7. Execution Unit

7.1 General Registers

The R1100 has eight 16-bit general registers. The AX, BX, CX and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows:

AX: word divide, word multiply, word I/O operation

AH: byte divide, byte multiply, byte I/O, decimal arithmetic, translate operation

AL: byte divide, byte multiply operation

BX: translate operation

CX: loops, string operation

CL: variable shift and rotate operation

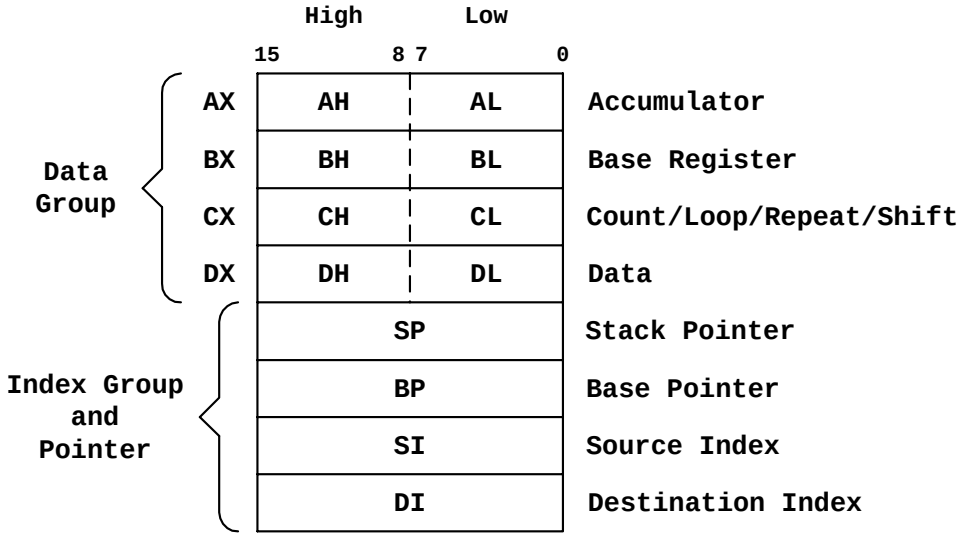
DX: word divide, word multiply, indirect I/O operation

SP: stack operations (POP, POPA, POPF, PUSH, PUSHA and PUSHF)

BP: general-purpose registers which can be used to determine offset address of operands in memory

SI: string operations

DI: string operations



GENERAL REGISTERS

7.2 Segment Registers

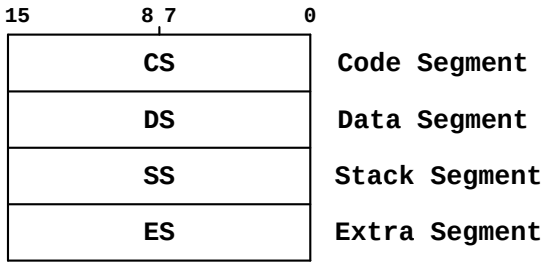
The R1100 has four 16-bit segment registers: CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments. They are immediately addressable for code (CS), data (DS & ES) and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instructions to be fetched. The default memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000h.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000h.

ES (Extra Segment): The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000h.



SEGMENT REGISTERS

7.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register containing the offset of the next instruction to be fetched. This register cannot be directly accessed by software. It is updated by the bus interface unit and can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000h and the starting execution address for CS: IP is at 0FFFF0h.

Register Name: Processor Status Flags Register

Reset Value : 0000h

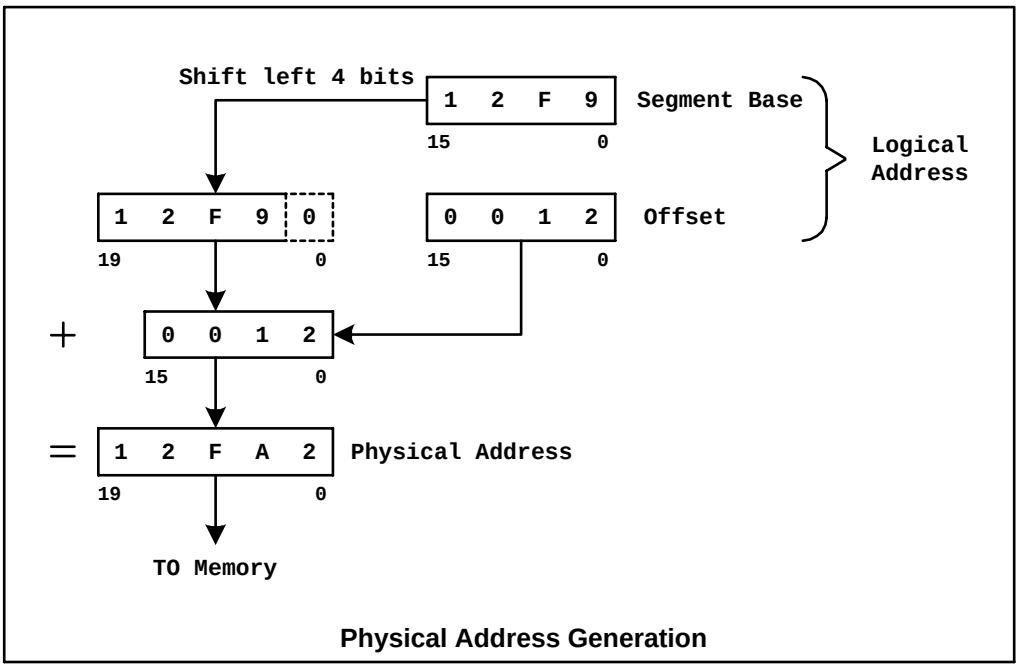
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing addresses. If DF is cleared, the string instructions are in the process of decrementing addresses. Refer to the STD and CLD instructions for setting and clearing the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for setting and clearing the IF flag. Set 1: The CPU enables the maskable interrupt requests. Set 0: The CPU disables the maskable interrupt requests.
8	TF	Trace Flag. Set to enable single-step mode for debugging; cleared to disable the single-step mode. If an application program sets the TF flag with a POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of the operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low one of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	Parity Flag. If this flag is set, the result of the low-order 8-bit operation will have even parities.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

7.4 Address Generation

The Execution Unit generates a 20-bit physical address to Bus Interface Unit by Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



Physical Address Generation

8. Peripheral Register List

The peripheral control block can be mapped into either memory or I/O space by programming the FEh register. It starts at FF00h in I/O space when the microprocessor is reset. The definitions of all the peripheral control block registers are listed in the following tables and the complete descriptions arranged in the related block units.

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	24	5E	Timer 1 Mode / Control Register	64
F6	Reset Configuration Register	29	5C	Timer 1 Maxcount Compare B Register	66
F4	Processor Release Level Register	24	5A	Timer 1 Maxcount Compare A Register	66
F0	PDCON Register	26	58	Timer 1 Count Register	66
DA	DMA 1 Control Register	58	56	Timer 0 Mode / Control Register	63
D8	DMA 1 Transfer Count Register	60	54	Timer 0 Maxcount Compare B Register	64
D6	DMA 1 Destination Address High Register	60	52	Timer 0 Maxcount Compare A Register	64
D4	DMA 1 Destination Address Low Register	61	50	Timer 0 Count Register	63
D2	DMA 1 Source Address High Register	61	44	Serial Port Interrupt Control Register	43
D0	DMA 1 Source Address Low Register	61	42	Watchdog Timer Control Register	69
CA	DMA 0 Control Register	57	40	INT4 Control Register	44
C8	DMA 0 Transfer Count Register	57	3E	INT3 Control Register	44
C6	DMA 0 Destination Address High Register	57	3C	INT2 Control Register	45
C4	DMA 0 Destination Address Low Register	58	3A	INT1 Control Register	45
C2	DMA 0 Source Address High Register	58	38	INT0 Control Register	46
C0	DMA 0 Source Address Low Register	58	36	DMA 1 Interrupt Control Register	47
A8	$\overline{PCS}$ and $\overline{MCS}$ Auxiliary Register	36	34	DMA 0 Interrupt Control Register	48
A6	Midrange Memory Chip Select Register	36	32	Timer Interrupt Control Register	48
A4	Peripheral Chip Select Register	37	30	Interrupt Status Register	49
A2	Low Memory Chip Select Register	35	2E	Interrupt Request Register	49
A0	Upper Memory Chip Select Register	34	2C	In-service Register	50
88	Serial Port Baud Rate Divisor Register	74	2A	Priority Mask Register	52
86	Serial Port Receive Register	73	28	Interrupt Mask Register	53
84	Serial Port Transmit Register	73	26	Poll Status Register	53
82	Serial Port Status Register	72	24	Poll Register	54
80	Serial Port Control Register	71	22	End-of-Interrupt	54
7A	PIO Data 1 Register	80	20	Interrupt Vector Register	55
78	PIO Direction 1 Register	80	18	Synchronous Serial Receive Register	76
76	PIO Mode 1 Register	80	16	Synchronous Serial Transmit 0 Register	76
74	PIO Data 0 Register	81	14	Synchronous Serial Transmit 1 Register	76
72	PIO Direction 0 Register	81	12	Synchronous Serial Enable Register	75
70	PIO Mode 0 Register	81	10	Synchronous Serial Status Register	75
66	Timer 2 Mode / Control Register	67	F8	PLLCON Register	25
62	Timer 2 Maxcount Compare A Register	68			
60	Timer 2 Count Register	68			

Register Offset: FEh

Register Name: Peripheral Control Block Relocation Register

Reset Value : 20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	S/$\overline{M}$	Rsvd	M/$\overline{IO}$	R [19:8]											

The peripheral control block is mapped into either memory or I/O space by programming this register. When the other chip selects ($\overline{PCSx}$ or $\overline{MCSx}$) are programmed to zero wait states and ignore the external ready, the $\overline{PCSx}$ or $\overline{MCSx}$ can overlap the control block.

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14	S/$\overline{M}$	R/W	Slave/Master – configures the interrupt controller. Set 0: Master mode. Set 1: Slave mode.
13	Rsvd	RO	Reserved.
12	M/$\overline{IO}$	R/W	Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The PCB is located in memory space. Set 0: The PCB is located in I/O space (default).
11-0	R[19:8]	R/W	Relocation Address bits. The upper address bits of the PCB base address. The lower eight bits default to 00h. When the PCB is mapped into the I/O space, R[19:16] must be programmed to 0000b.

Register Offset: F4h

Register Name: Processor Release Level Register

Reset Value : --D9h

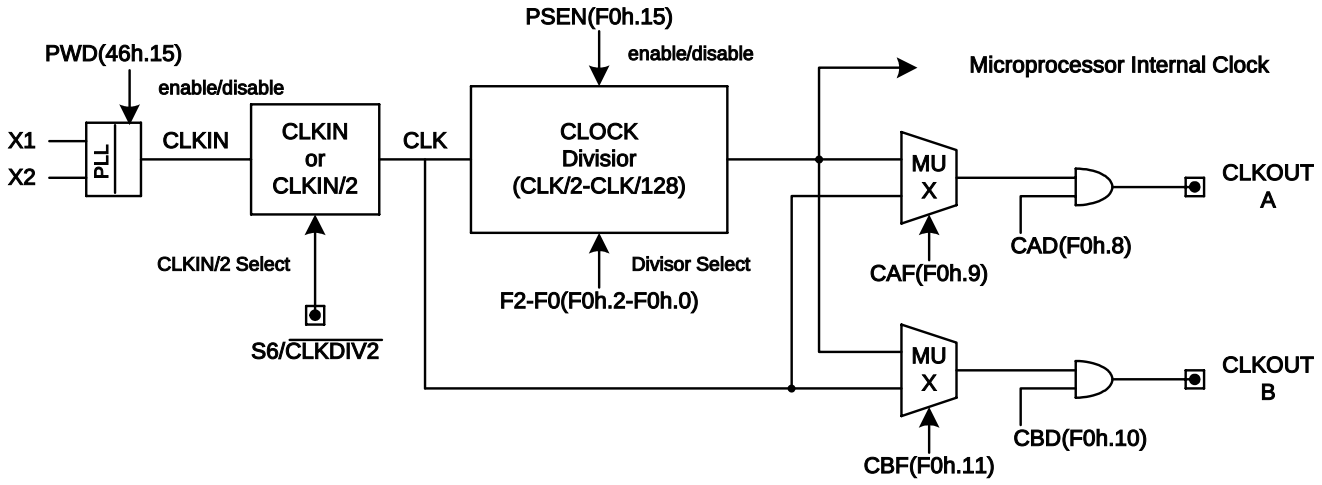
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	0	1	1	1	0	1	1	0	0	1

This read-only register specifies the processor release version and RDC identification number.

Bit	Name	Attribute	Description
15-0			C5D9h

---

9. System Clock Block



System Clock

Register Offset: F8h
Register Name: PLL Configuration Register
Reset Value : 05Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd				PRS1	PRS0	POS1	POS0	Rsvd			FBS4	FBS3	FBS2	FBS1	FBS0

The initial PLL factor is 1(CLKIN=Crystal frequency). The factor is adjusted by changing the value of N, M and R.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-10	PRS	R/W	Programming signals for pre-divider.
9-8	POS	R/W	Programming signals for post-divider.
7-5	Rsvd	RO	Reserved.
4-0	FBS	R/W	Programming signals for feedback divider.

PRS	M
00	1
01	2
10	3
11	4

POS	R
00	1
01	2
10	4
11	8

FBS	N	FBS	N	FBS	N	FBS	N
00000	1	01000	9	10000	17	11000	25
00001	2	01001	10	10001	18	11001	26
00010	3	01010	11	10010	19	11010	27
00011	4	01011	12	10011	20	11011	28
00100	5	01100	13	10100	21	11100	29
00101	6	01101	14	10101	22	11101	30
00110	7	01110	15	10110	23	11110	31
00111	8	01111	16	10111	24	11111	32

$$CLKOUT = FREF * \frac{N}{M * R}$$

(CKOUT : Internal/output frequency, FREF : input frequency), 2MHz≤ FREF ≤24MHz

PRS	M
00	1
01	2
10	3
11	4

POS	R
00	1
01	2
10	4
11	8

FBS	N	FBS	N	FBS	N	FBS	N
00000	1	01000	9	10000	17	11000	25
00001	2	01001	10	10001	18	11001	26
00010	3	01010	11	10010	19	11010	27
00011	4	01011	12	10011	20	11011	28
00100	5	01100	13	10100	21	11100	29
00101	6	01101	14	10101	22	11101	30
00110	7	01110	15	10110	23	11110	31
00111	8	01111	16	10111	24	11111	32

Note

1. 20 MHz < FREF * N / M < 280MHz
2. N=1 : 5 MHz * M <= FREF < 50 MHz,
   N=2 : 3.5 MHz * M <= FREF < 50 MHz,
   N=3-32 : 2.8 MHz * M<= FREF < 50 MHz
3. The frequency working range of crystal pad is 2 ~ 24 MHz.

Register Offset: F0h
Register Name: Power-Save Control Register
Reset Value : 0000h

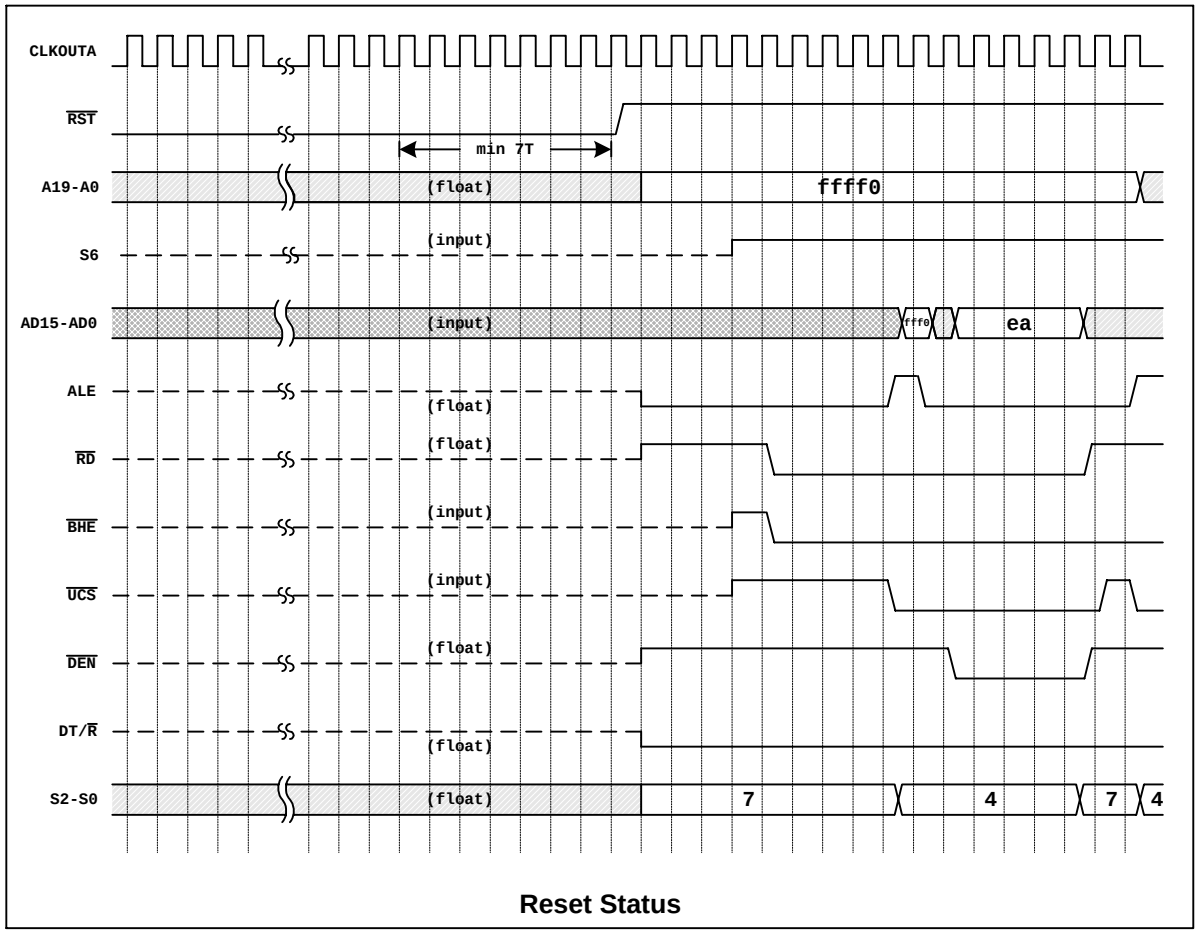
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	0	0	0	CBF	CBD	CAF	CAD	0	0	0	SALEn	0	F2	F1	F0

Bit	Name	Attribute	Description
15	PSEN	R/W	Enable Power-Save Mode. This bit is cleared by hardware when an external interrupt occurs. This bit will not change when software interrupts (INT instructions) and exceptions occur. Set 1: Enable power-save mode and divide the internal operating clock by values in F[2:0].
14-12	Rsvd	RO	Reserved.
11	CBF	R/W	CLKOUTB Output Frequency selection. Set 1: The CLKOUTB output frequency is the same as the crystal input frequency. Set 0: The CLKOUTB output frequency, which is the same as the internal clock frequency of the microprocessor, is generated from the clock divisor.
10	CBD	R/W	CLKOUTB Drive Disable Set 1: Disable CLKOUTB. This pin will be three-stated. Set 0: Enable CLKOUTB.
9	CAF	R/W	CLKOUTA Output Frequency selection. Set 1: The CLKOUTA output frequency is the same as the crystal input frequency. Set 0: The CLKOUTA output frequency, which is the same as the internal clock frequency of the microprocessor, is generated from the clock divisor.
8	CAD	R/W	CLKOUTA Drive Disable. Set 1: Disable CLKOUTA. This pin will be three-stated. Set 0: Enable CLKOUTA.
7-5	Rsvd	RO	Reserved.
4	SALEn	R/W	Insert ALE delay. Set 1: One more T1 is added, the bus should be 5T cycle. Set 0: Normal bus cycle. ALE without delay.
3	Rsvd	RO	Reserved.
2-0	F[2:0]	R/W	Clock Divisor Select. **F2, F1, F0 ----- Divider Factor** 0, 0, 0 ---- Divide by 1 0, 0, 1 ---- Divide by 2 0, 1, 0 ---- Divide by 4 0, 1, 1 ---- Divide by 8 1, 0, 0 ---- Divide by 16 1, 0, 1 ---- Divide by 32 1, 1, 0 ---- Divide by 64 1, 1, 1 ---- Divide by 128

10. Reset

Processor initialization is accomplished with activation of the $\overline{RST}$ pin. To reset the processor, this pin should be held how for at least seven oscillator periods. The Reset Status Figure shows the status of the $\overline{RST}$ pin and others relation pins.

When $\overline{RST}$ from low go high, the state of input pin (with weakly pull-up or pull-down) will be latched , and each pin will perform the individual function. The AD15-AD0 will be latched into the register F6h. $\overline{UCS}$ / $\overline{ONCE1}$, $\overline{LCS}$ / $\overline{ONCE0}$ will enter ONCE mode (All of the pins will floating except X1 , X2) when with pull-low resisters. The input clock will divide by 2 when S6/ $\overline{CLKDIV2}$ with pull-low resister. The AD15-AD0 bus will not drive the address phase during $\overline{UCS}$, $\overline{LCS}$ cycle if $\overline{BHE}$ / $\overline{ADEN}$ with pull-low resister



Reset Status

Register Offset: F6h

Register Name: Reset Configuration Register

Reset Value : AD [15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

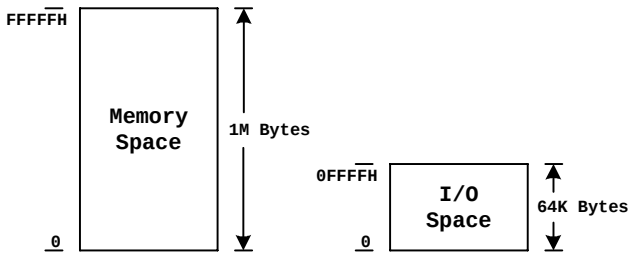
Bit	Name	Attribute	Description
15-0	RC	RO	The AD15 to AD0 must with weakly pull-up or pull-down resistors to correspond the contents when AD15-AD0 is latched into this register during the $\overline{RST}$ pin goes from low to high. And the value of the reset configuration register provides the system information when software read this register. This register is read only and the contents remain valid until the next processor reset.

11. Bus Interface Unit

The bus interface unit drives address, data, status, and control information to define a bus cycle. The bus A[19:0] are non-multiplex memory or I/O address. The AD[15:0] are multiplexed address and data bus for memory or I/O accessing. The $\overline{S2}$ - $\overline{S1}$ are encoded to indicate the bus status, which is described in the Pin Description table. The Basic Application System Block and Read/Write Timing Diagram describe the basic bus operation.

11.1 Memory and I/O Interface

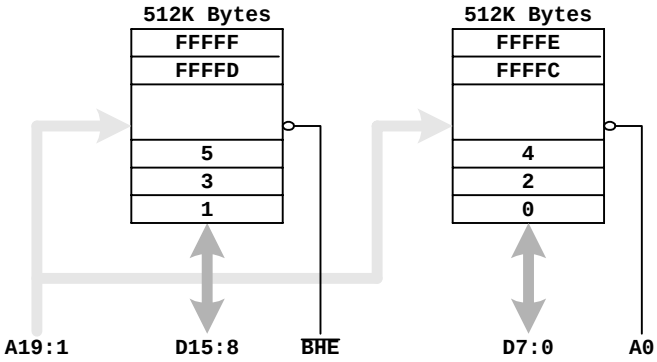
The memory space consists of 1M bytes (512k 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instructions can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of the I/O space can be accessed directly by the I/O instructions. The entire 64k-byte I/O address space can be accessed indirectly through the DX register. The I/O instructions always force address A[19:16] to low level.



Memory and I/O Space

11.2 Data Bus

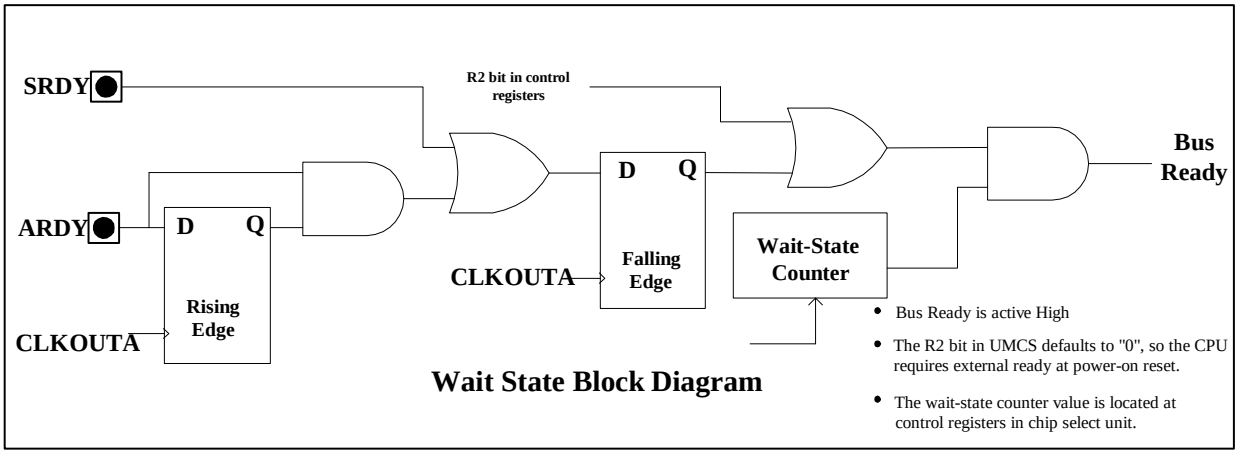
The memory address space data bus is physically implemented by dividing the address space into two banks of up to 512k bytes. Each one bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and $\overline{BHE}$ determine whether one bank or both banks participate in the data transfer.



Physical Data Bus Models

11.3 Wait States

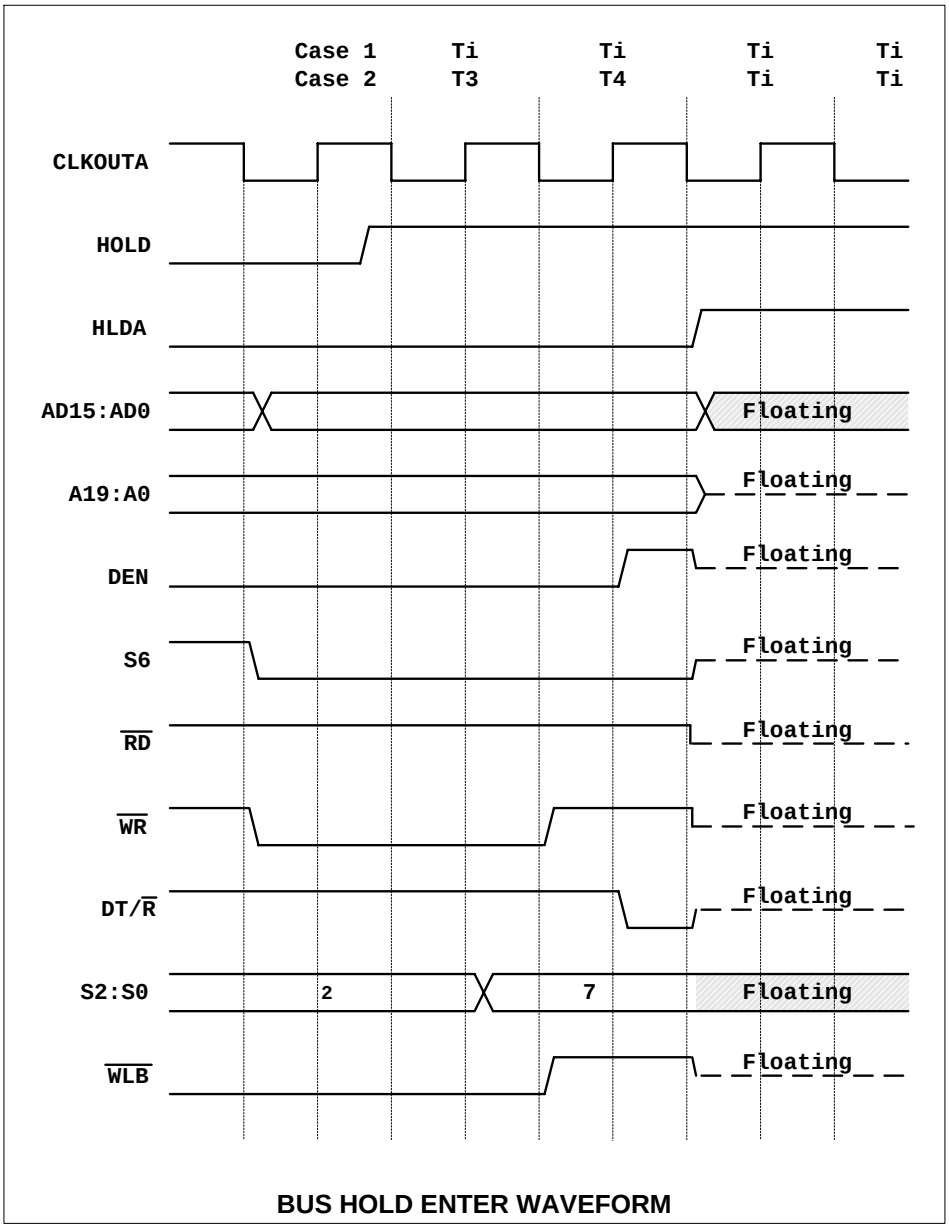
Wait states extend the data phase of the bus cycle. The ARDY or SRDY input with low level will insert wait states. If R2 bit=0, the user also can inserts wait state by programmed the internal chip select registers. The R2 bit of UMCS (offset 0A0h) default is low, so each one of the ARDY or SRDY should in ready state (with pull high resistor) when at power on reset or external reset. The wait state counter value is decided by the R3, R1, R0 bits in each chip select register. There are five group R3, R1, R0 bits in the registers offset A0h, A2h, A4h, A6h, A8h. Each group is independent.



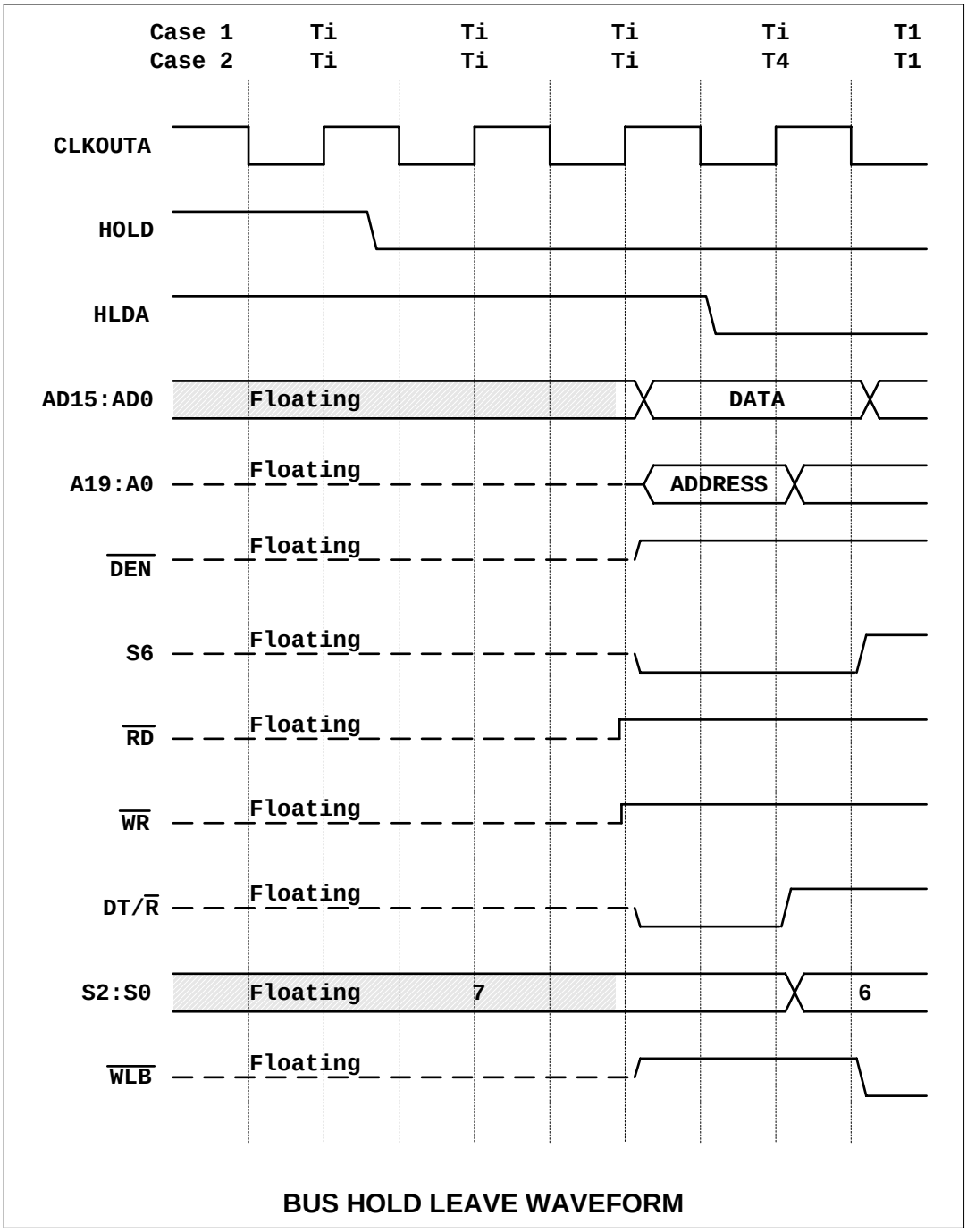
Wait State Block Diagram

11.4 Bus Hold

When the bus hold requested (HOLD pin active high) by the another bus master, the microprocessor will issue a HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S1}$ - $\overline{S0}$, $\overline{S6}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be drive high. After HOLD is detected as being low, the microprocessor will lower the HLDA.



BUS HOLD ENTER WAVEFORM



BUS HOLD LEAVE WAVEFORM

12. Chip Select Unit

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h and A8h) and all the chip selects can be inserted wait states in by programming the peripheral control registers.

12.1 $\overline{\text{UCS}}$

$\overline{\text{UCS}}$ defaults to active on reset for program code access. The memory active range is upper 512k (80000h – FFFFFh), which is programmable. And the default memory active range of $\overline{\text{UCS}}$ is 64k (F0000h – FFFFFh).

$\overline{\text{UCS}}$ is active to drive low four CLKOUTA oscillators if no wait state inserts. There are three wait-states insert to $\overline{\text{UCS}}$ active cycle on reset.

Register Offset: A0h
Register Name: Upper Memory Chip Select Register
Reset Value : F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB [2:0]			0	0	0	0	DA	0	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	LB[2:0]	R/W	Memory block size selection for $\overline{\text{UCS}}$ chip select pin. The $\overline{\text{UCS}}$ chip select pin active region can be configured by the LB2-LB0. The default memory block size is from F0000h to FFFFFh. **LB2, LB1, LB0 ---- Memory Block size , Start address, End Address** 1 , 1 , 1 ---- 64k , F0000h , FFFFFh 1 , 1 , 0 ---- 128k , E0000h , FFFFFh 1 , 0 , 0 ---- 256k , C0000h , FFFFFh 0 , 0 , 0 ---- 512k , 80000h , FFFFFh
11-8	Rsvd	RO	Reserved
7	DA	R/W	If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, then the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drive the address and data. Set 1 : Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted. Set 0 : Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

6-4	Rsvd	RO	Reserved
3	R3	R/W	See bit [1:0]
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**R3, R1-R0**, Wait-State value. When R2 is set to 0, it can be inserted wait-state into an access to the $\overline{\text{UCS}}$ memory area. **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 15

12.2 $\overline{\text{LCS}}$

The lower 512k bytes (00000h-7FFFFh) memory region chip selects. The memory active range is programmable, which has no default size on reset. So the A2h register must be programmed first before to access the target memory range. The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h register activates this pin.

Register Offset: A2h
Register Name: Low Memory Chip Select Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UB [2:0]			1	1	1	1	DA	PSE	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	UB[2:0]	R/W	**UB[2:0]**, Memory block size selection for $\overline{LCS}$ chip select pin.The $\overline{LCS}$ chip select pin active region can be configured by the UB2-UB0. The $\overline{LCS}$ pin is not active on reset, but any read or write access to the A2h (LMCS) register activates this pin. **UB2, UB1, UB0 ---- Memory Block size , Start address, End Address** 0 , 0 , 0 ---- 64k , 00000h , 0FFFFh 0 , 0 , 1 ---- 128k , 00000h , 1FFFFh 0 , 1 , 1 ---- 256k , 00000h , 3FFFFh 1 , 1 , 1 ---- 512k , 00000h , 7FFFFh
11-8	Rsvd	RO	Reserved
7	DA	R/W	Disable Address. If the $\overline{BHE}$ / $\overline{ADEN}$ pin is held high on the rising edge of $\overline{RST}$, then the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{BHE}$ / $\overline{ADEN}$ pin is held high on the rising edge of $\overline{RST}$, the AD bus always drive the address and data. Set 1: Disable the address phase of the AD15 – AD0 bus cycle when $\overline{LCS}$ is asserted. Set 0: Enable the address phase of the AD15 – AD0 bus cycle when $\overline{LCS}$ is asserted.
6	PSE	R/W	PSRAM Mode Enable. This bit is used to enable PSRAM support for the $\overline{LCS}$ chip select memory space. The refresh control unit registers E0h,E2h,E4h must be configured for auto refresh before PSRAM support is enabled. PSE set to 1: PSRAM support is enabled. PSE set to 0: PSRAM support is disabled.
5-3	Rsvd	RO	Reserved
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for $\overline{LCS}$ chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State value. When R2 is set to 0, it can be inserted wait-state into an access to the $\overline{LCS}$ memory area. **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

12.3 $\overline{\text{MCSx}}$

The memory block of $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$ can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with the $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ chip selects. The maximum $\overline{\text{MCSx}}$ active memory range is 512k bytes. The $\overline{\text{MCSx}}$ chip selects are programmed through two registers A6h and A8h, and these select pins are not active on reset. Both A6h and A8h registers must be accessed with a read or write to activate $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$. There aren't default value on A6h and A8h registers, so the A6h and A8h must be programmed first before $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$ active.

Register Offset: A6h
Register Name: Midrange Memory Chip Select Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:13]							1	1	1	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15-9	BA[19:13]	R/W	Base Address. BA[19:13] correspond to bits 19-13 of the 1M bytes (20-bits) programmable base address of the $\overline{\text{MCS}}$ chip select block. The bits 12 to 0 of the base address are always 0. The base address can be set to any integer multiple of the size of the memory block size selected in these bits. For example, if the midrange block is 32Kbytes, only the bits BA19 to BA15 can be programmed. So the block address could be located at 20000h or 38000h but not in 22000h. The base address of the $\overline{\text{MCS}}$ chip select can be set to 00000h only if the $\overline{\text{LCS}}$ chip select is not active. And the $\overline{\text{MCS}}$ chip select address range is not allowed to overlap the $\overline{\text{LCS}}$ chip select address range. The $\overline{\text{MCS}}$ chip select address range also is not allowed to overlap the $\overline{\text{UCS}}$ chip select address range.
8-3	Rsvd	RO	Reserved.
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{\text{MCS}}$ chip selects. The R1 and R0 bits of this register determine the number of wait states inserted in. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State Value. R1 and R0 determine the number of wait states inserted into an access to the $\overline{\text{MCS}}$ memory area.

Register Offset: A8h
Register Name: PCS_n and MCS_n Auxiliary Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	M[6:0]							EX	MS	Rsvd			R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-8	M[6:0]	R/W	$\overline{MCS}$ Block Size. These bits determines the total block size for the $\overline{MCS3}$ - $\overline{MCS0}$ chip selects. Each individual chip select is active for one quarter of the total block size. For example, if the block size is 32K bytes and the base address is located at 20000h. The individual active memory address range of $\overline{MCS3}$ to $\overline{MCS0}$ is $\overline{MCS0}$ – 20000h to 21FFF, $\overline{MCS1}$-22000 to 23FFFh, $\overline{MCS2}$ - 24000h to 25FFFh, $\overline{MCS3}$ - 26000h to 27FFFh. $\overline{MCSx}$ total block size is defined by M6-M0, **M[6:0]** , **Total block size**, $\overline{MCSx}$ **address active range** 0000001b , 8k , 2k 0000010b , 16k , 4k 0000100b , 32k , 8k 0001000b , 64k , 16k 0010000b , 128k , 32k 0100000b , 256k , 64k 1000000b , 512k , 128k
7	EX	R/W	Pin Selector. This bit configures the multiplex output which the $\overline{PCS6}$ - $\overline{PCS5}$ pins as chip selects or A2-A1. Set 1 : $\overline{PCS6}$, $\overline{PCS5}$ are configured as peripheral chip select pins. Set 0: $\overline{PCS6}$ is configured as address bit A2, $\overline{PCS5}$ is configured as A1.
6	MS	R/W	Memory or I/O space selector. Set 1: The $\overline{PCSx}$ pins are active for memory bus cycle. Set 0: The $\overline{PCSx}$ pins are active for I/O bus cycle.
5-3	Rsvd	RO	Reserved.
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{PCS5}$ and $\overline{PCS6}$ chip selects. The R1 and R0 bits of this register determine the number of wait states inserted. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State value. The R1, R0 determines the number of wait states inserted into a $\overline{PCS5}$ - $\overline{PCS6}$ access. **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

12.4 $\overline{\text{PCSx}}$

The peripheral or memory chip selects which are programmed through A4h and A8h register to define these pins. The base address memory block can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with the $\overline{\text{MCS4}}$, $\overline{\text{LCS}}$ and $\overline{\text{MCS}}$ chip elects. If the chip selects are mapped to I/O space, the access range is 64k bytes. $\overline{\text{PCS6}}$ – $\overline{\text{PCS5}}$ can be configured from 0 wait-state to 3 wait-states. $\overline{\text{PCS3}}$ – $\overline{\text{PCS0}}$ can be configured from 0 wait-state to 15 wait-states.

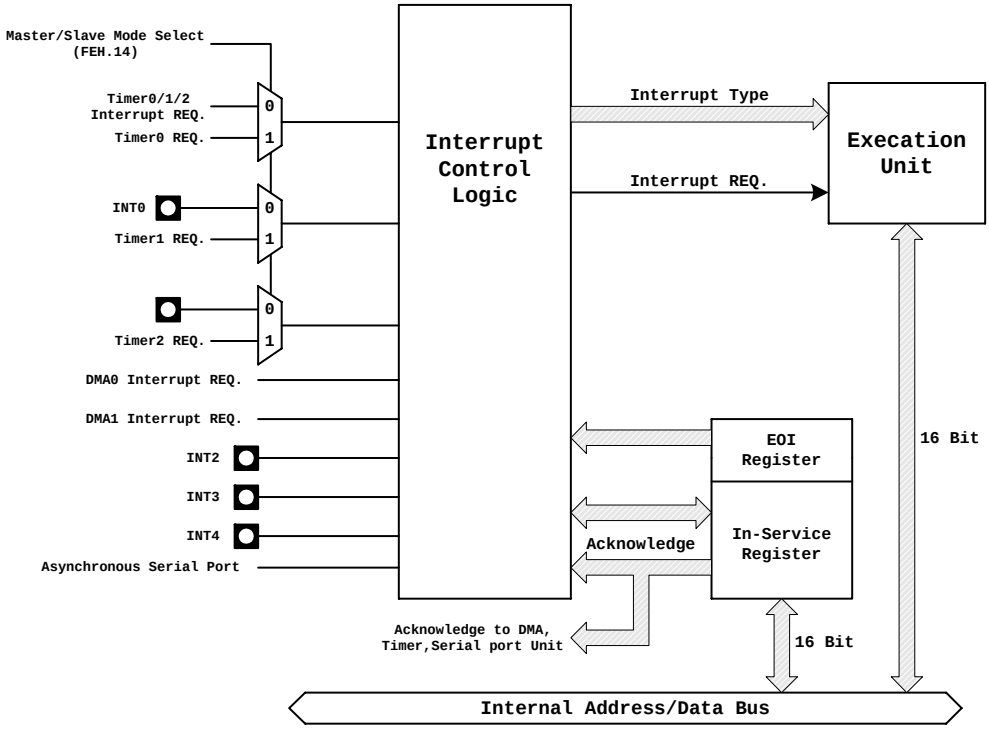
Register Offset: A4h
Register Name: Peripheral Chip Select Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA [19:11]									1	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15-7	BA[19:12]	R/W	Base Address. BA[19:11] correspond to bit [19:11] of the 1M-byte (20-bit) programmable base address of the $\overline{\text{PCS}}$ chip select block. When the $\overline{\text{PCS}}$ chip selects are mapped to I/O space, BA[19:16] must be written to 0000b because the I/O address bus is only 64K bytes (16 bits) wide. $\overline{\text{PCS}}$ **address range:** $\overline{\text{PCS0}}$: Base Address - Base Address+255 $\overline{\text{PCS1}}$: Base Address+256 - Base Address+511 $\overline{\text{PCS2}}$: Base Address+512 - Base Address+767 $\overline{\text{PCS3}}$: Base Address+768 - Base Address+1023 $\overline{\text{PCS5}}$: Base Address+1280 - Base Address+1535 $\overline{\text{PCS6}}$: Base Address+1536 - Base Address+1791
6-4	Rsvd	RO	Reserved.
3	R3	R/W	See bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{\text{PCS3}}$ - $\overline{\text{PCS0}}$ chip selects. The R3, R1 and R0 bits determine the number of wait states to be inserted. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Value. R3, R1 and R0 determine the number of wait states inserted into an access to the PCS3_n – PCS0_n memory area. **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 15

13. Interrupt Controller Unit

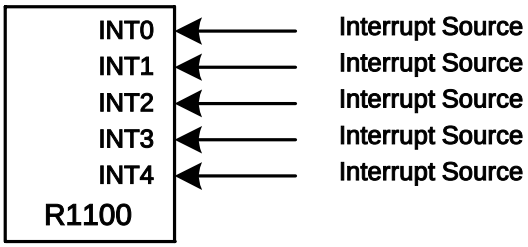
There are 12 interrupt request sources connected to the controller: 5 maskable interrupt pins (INT0 – INT4); 1 non-maskable interrupts (NMI); 6 internal unit request sources (Timer 0, 1 and 2; DMA 0 and 1; Asynchronous serial unit).



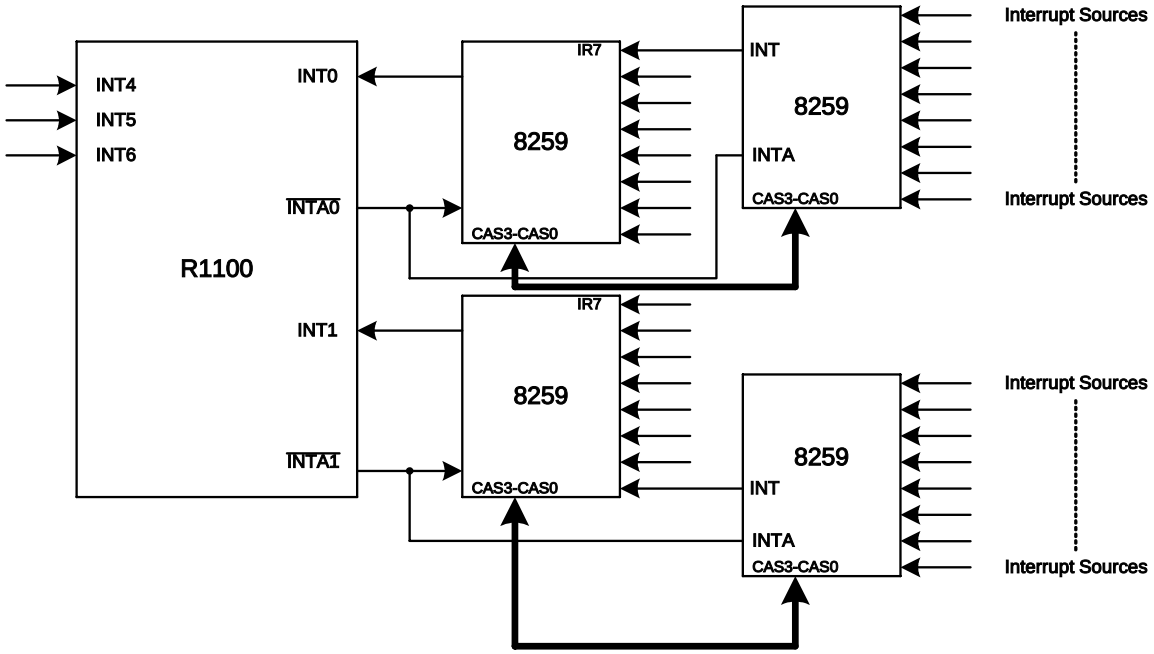
Interrupt Control Unit Block Diagram

13.1 Master Mode and Slave Mode

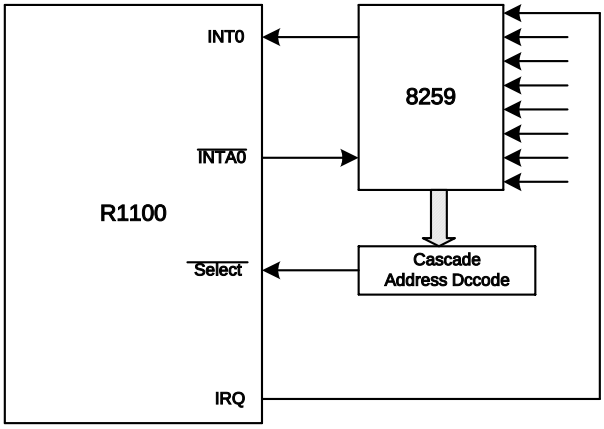
The interrupt controller can be programmed as master or slave mode. To program FEh [14], the master mode has two connections: fully nested mode or cascade mode.



Fully Nested Mode Connections



Cascade Mode Connection



Slave Mode Connection

13.2 Interrupt Vectors, Types and Priorities

The following table shows the interrupt vector addresses, types and priorities. Programming the priority registers may change the maskable interrupt priorities. The vector address for each interrupt is fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*/**
Reserved	09h				
DMA 0	0Ah	28h	0Ah	3	**
DMA 1	0Bh	2Ch	0Bh	4	**
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
INT4	10h	40h	10h	9	
Watchdog Timer	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*/**
Timer 2	13h	4Ch	08h	2-3	*/**
Asynchronous Serial port	14h	50h	14h	9	
Reserved	15h-1Fh				

***Note** *: When the interrupt occurs in the same time, the priority is (1-1 > 1-2); (2-1> 2-2 > 2-3)*

***Note **:** The interrupt types of these sources are programmable in slave mode.*

13.3 Interrupt Requests

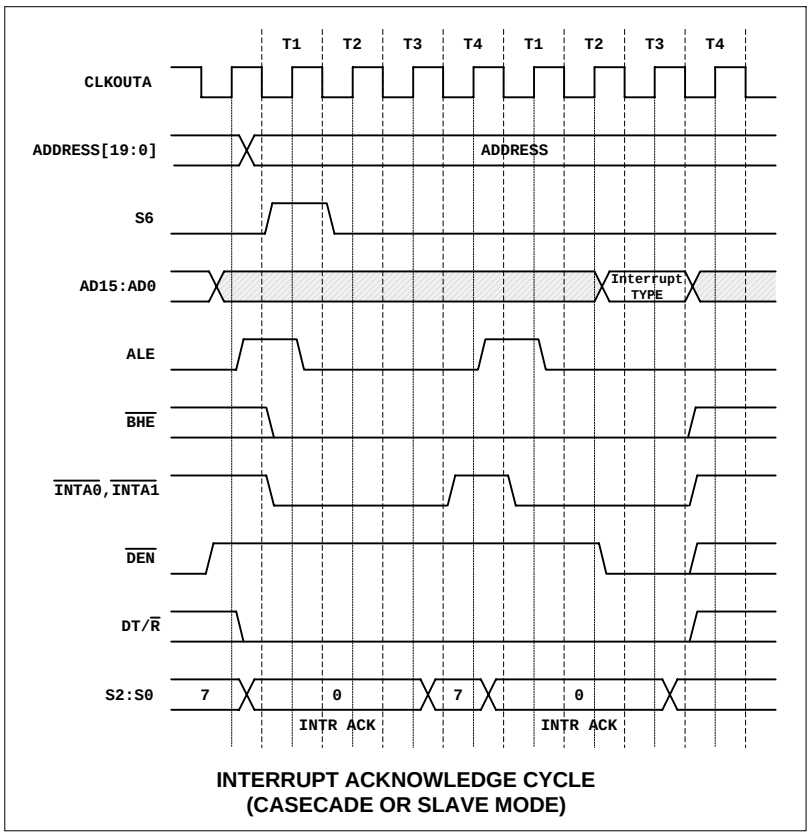
When an interrupt is requested, the internal interrupt controller verifies that the interrupt is enabled (the IF flag is enabled, but no MSK bit is set) and that there is no higher priority interrupt request being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-triggered) to request the interrupt controller service, the INT pins must be held till the microcontroller enters the interrupt service routine. There is no interrupt-acknowledge output when the microcontroller runs in fully nested mode, so the PIO pin should be used to simulate the interrupt-acknowledge pin if necessary.

13.4 Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. The internal interrupt can provide the interrupt type or an external controller can provide the interrupt type.

The internal interrupt controller provides the interrupt type to processor without external bus cycles generation. When an external interrupt controller is supplying the interrupt type, the processor generates two acknowledge bus cycles, and the interrupt type is written to the AD[7:0] lines by the external interrupt controller.



INTERRUPT ACKNOWLEDGE CYCLE (CASECADE OR SLAVE MODE)

13.5 Programming Registers

Registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 22h and 20h) are programmed by software to define the interrupt controller operation.

Register Offset: 44h
Register Name: Serial Port Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 0. Set 0: Enable the serial port 0 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 40h
Register Name: INT4 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set to 1 and bit 4 cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT4. Set 0: Enable the INT4 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 3Eh
Register Name: INT3 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd								ETM	Rsvd		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set to 1 and bit 4 cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT3. Set 0: Enable the INT3 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 3Ch
Register Name: INT2 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd								ETM	Rsvd		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT2. Set 0: Enable the INT2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 3Ah
Register Name: INT1 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1
5	C	R/W	Cascade Mode. Set this bit to 1 to enable the cascade mode for INT1 or INT0.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.

3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT1. Set 0: Enable the INT1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

(Slave Mode) This register is for Timer 2 interrupt control, reset value is 0000h.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of Timer 2. Set 0: Enable the Timer 2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 38h
Register Name: INT0 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0
5	C	R/W	Cascade Mode. Set this bit to 1 to enable the cascade mode for INT0.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT0. Set 0: Enable the INT0 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

(Slave Mode) For Timer 1 interrupt control register, reset value is 0000h.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of Timer 1. Set 0: Enable the Timer 1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 36h
Register Name: DMA1 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

(Slave Mode) Reset value is 0000h.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 34h
Register Name: DMA0 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

(Slave Mode) Reset value is 0000h.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 32h
Register Name: Timer Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer controller. Set 0: Enable the timer controller interrupt.

2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

(Slave Mode) Reset value is 0000h.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the Timer 0 controller. Set 0: Enable the Timer 0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit[2:0] in the 44h register.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2	TMR1	TMR0

(Master Mode) Reset value is not defined.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: When an IRET instruction is executed.
14-3	Rsvd	RO	Reserved.
2-0	TMR[2:0]	R/W	Set 1: Indicate that the corresponding timer has an interrupt request pending.

(Slave Mode) Reset value is 0000h.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: When an IRET instruction is executed.
14-3	Rsvd	RO	Reserved.
2-0	TMR[2:0]	R/W	Set 1: Indicate that the corresponding timer has an interrupt request pending.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Rsvd	TMR

(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5 and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT[4:0] external interrupts, the corresponding bits (I[4:0]) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SPI	RO	Serial Port Interrupt Request. Indicates the interrupt status of the serial port.
9	WD		Watchdog Timer Interrupt Request.
8-4	I[4:0]	RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/I6 D0/I5	RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved.
0	TMR	RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TRM1	D1/I6	D0/I5	Rsvd	TMR0

(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1, D0, TMR2, TMR1 and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
6-4	TMR[2:1]	RO	Timer2/Timer1 Interrupt Request. Set 1: Indicates the state of any interrupt requests from the associated timer.

3-2	D[1:0]	RO	DMA Channel Interrupt Request. Set 1: The corresponding DMA channel has an interrupt pending.
1	Rsvd	RO	Reserved.
0	TMR0	RO	Timer0 Interrupt Request. Set 1: Indicates the state of an interrupt request from Timer 0.

Register Offset: 2Ch
Register Name: In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Rsvd	TMR

(Master Mode)

The bits in the INSERV register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SPI	RO	Serial Port Interrupt In-Service. Set 1: the serial port interrupt is currently being serviced.
9	WD		Watchdog Timer Interrupt In-service.
8-4	I[4:0]	RO	Interrupt In-Service. Set 1: the corresponding INT interrupt is currently being serviced.
3-2	D[1:0]	RO	DMA Channel Interrupt In-Service. Set 1: the corresponding DMA channel interrupt is currently being serviced.
1	Rsvd	RO	Reserved.
0	TMR	RO	Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

Register Offset: 2Ch
Register Name: In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Rsvd	TMR

(Slave Mode)

The bits in the In-Service register are set by the interrupt controller when the interrupt is taken. The in-service bits are cleared by writing to the EOI register.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
5-4	TMR[2:1]	Ro	Timer2/Timer1 Interrupt In-Service. Set 1: the corresponding timer interrupt is currently being serviced.
3-2	D[1:0]	RO	DMA Channel Interrupt In-Service. Set 1: the corresponding DMA Channel Interrupt is currently being serviced.
1	Rsvd	RO	Reserved.
0	TMR0	RO	Timer 0 Interrupt In-Service. Set 1: the Timer 0 interrupt is currently being serviced.

Register Offset: 2Ah
Register Name: Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode)

It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2-0	PRM[2:0]	R/W	Priority Field Mask, It determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

(Slave Mode)

It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.

2-0	PRM[2:0]	R/W	Priority Field Mask, It determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : 07FDh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Rsvd	TMR

(Master Mode)

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SPI	RO	Serial Port Interrupt Mask. It indicates the state of the mask bit of the asynchronous serial port interrupt.
9	WD	RO	Virtual Watchdog Timer Interrupt Mask. It indicates the state of the mask bit of the Watchdog Timer interrupt.
8-4	I[4:0]	RO	Interrupt Masks. They indicate the states of the mask bits of the corresponding interrupts.
3-2	D1/I6 – D0/I5	RO	DMA Channel Interrupt Masks. They indicate the states of the mask bits of the corresponding DMA channel interrupts.
1	Rsvd	RO	Reserved.
0	TMR	RO	Timer Interrupt Mask. It indicates the state of the mask bit of the timer control unit.

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : 003Dh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/I6	D0/I5	Rsvd	TMR0

(Slave Mode)

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
5-4	TMR[2:1]	RO	Timer2/Timer1 Interrupt Mask. They indicate the states of the mask bits of the Timer Interrupt Control Register. Set 1: Timer2 or Time1 has its interrupt requests masked
3-2	D[1:0]	RO	DMA Channel Interrupt Masks. They indicate the states of the mask bits of the corresponding DMA Control Registers.
1	Rsvd	RO	Reserved.
0	TMR0	RO	Timer0 Interrupt Mask. It indicates the state of the mask bit of the Timer Interrupt Control Register

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Register Offset: 26h
Register Name: Poll Status Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

(Master Mode)

The Interrupt Poll Status Register mirrors the current state of the Interrupt Poll Register. This register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 24h
Register Name: Poll Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

(Master Mode)

When the Interrupt Poll Register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Interrupt Poll Register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 22h
Register Name: End-of-Interrupt Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC	Reserved											S[4:0]			

(Master Mode)

Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates the non-specific EOI. Set 0: indicates the specific EOI interrupt type in S4-S0.
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	WO	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

Register Offset: 22h
Register Name: Specific EOI Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	L2	L1	L0

(Slave Mode)

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2-0	L[2:0]	WO	Interrupt Type. The encoded value indicates the priority of the IS (interrupt service) bit to be reset. Writes to these bits cause an EOI issued for the interrupt type in slave mode.

Register Offset: 20h
Register Name: Interrupt Vector Register
Reset Value : ——

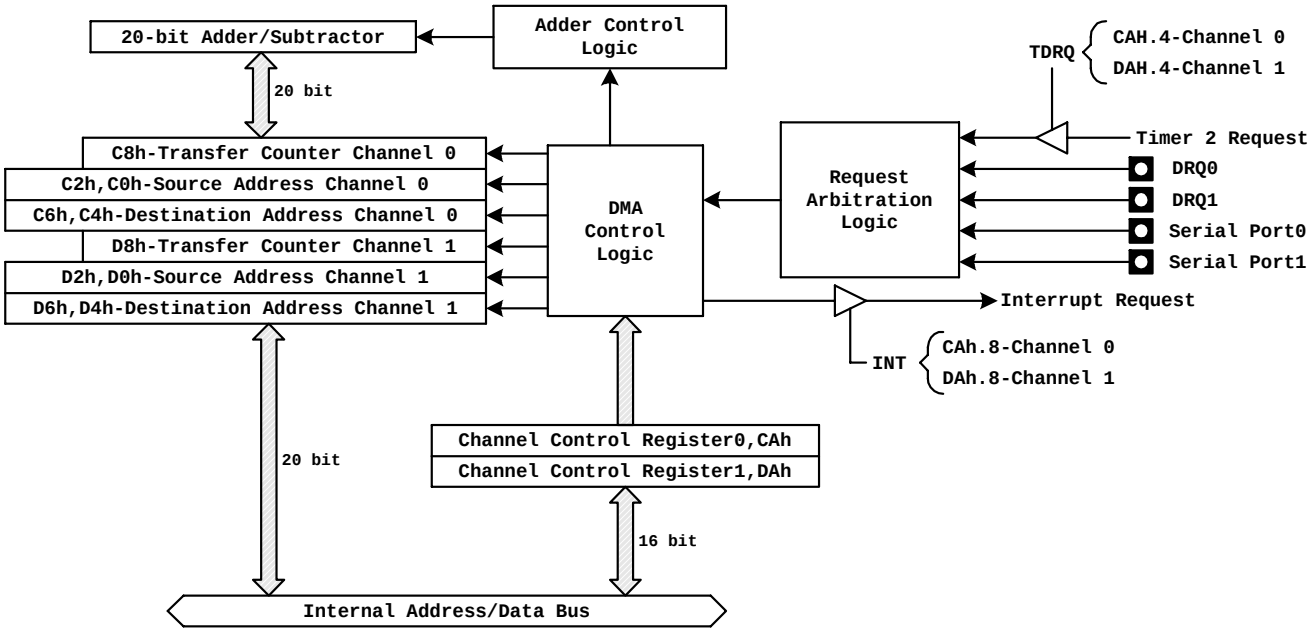
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	T[4:0]					0	0	0

(Slave Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-3	T[4:0]	R/W	Interrupt Types. The following interrupt types in slave mode can be programmed. Timer 2 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 1) b. Timer 1 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 0) b. DMA 1 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 1) b. DMA 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 0) b. Timer 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 0, 0) b.
2-0	Rsvd	RO	Reserved.

14. DMA Unit

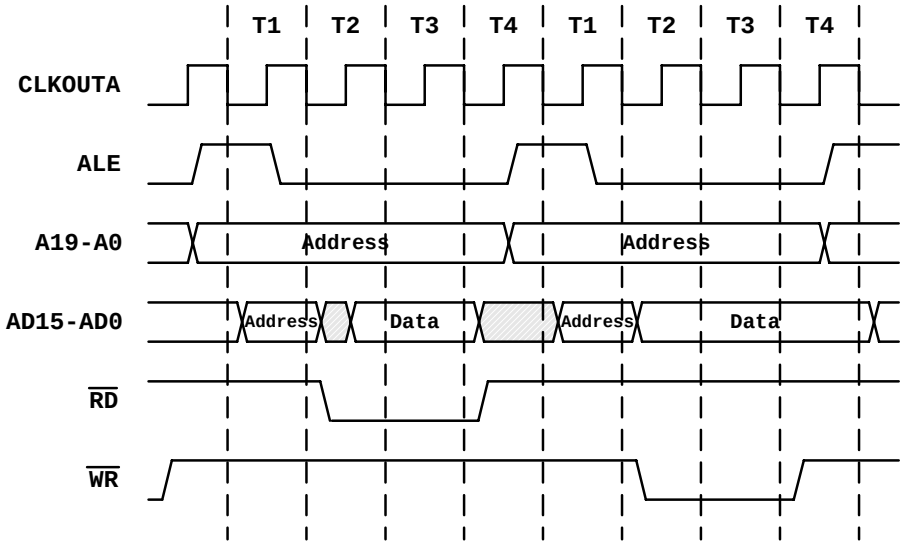
The DMA controller provides the data transfers between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port0 or port1), or Timer 2 overflow. The data transfers from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (reads from sources and writes to destinations) for each data transfer.



DMA Unit Block

14.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer). These two bus cycles cannot be separated by a bus hold request, a refresh request or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h and D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

Register Offset: CAh (DMA0)
Register Name: DMA0 Control Register
Reset Value : FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{DM}/\overline{IO}$	DDEC	DINC	SM/$\overline{IO}$	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	Rsvd	CHG	ST	$\overline{B}$/W

Bit	Name	Attribute	Description
15	$\overline{DM}/\overline{IO}$	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The $\overline{B}$/W (bit 0) bit determines the decrement value which is by 1 or 2 When both DDEC and DINC bits are set to 1, the address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The $\overline{B}$/W (bit 0) bit determines the increment value which is by 1 or 2. Set 0: Disable the increment function.
12	SM/$\overline{IO}$	R/W	Source Address Space Select. Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.

11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The $\overline{B}$/W (bit 0) bit determines the decremented value is by 1 or 2. When both the SDEC and SINC bits are set to 1 or 0, the address remains constant. Set 0: Disable the decrement function.
10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The $\overline{B}$/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
9	TC	R/W	Terminal Count. Set 1: Synchronized DMA transfers terminate when the DMA Transfer Count Register reaches 0. Set 0: Synchronized DMA transfers do not terminate when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfers always terminate when the DMA transfer count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: The DMA unit generates an interrupt request on completion of the transfer count. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. **SYN1 , SYN0 -- Synchronization Type** 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from timer 2. Set 0: Disable the DMA requests from timer 2.
3	Rsvd	RO	Reserved
2	CHG	R/W	Changed Start bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	$\overline{B}$/W	R/W	Byte/Word Select. Set 1: The address is incremented or decremented by 2 after each transfer. Set 0: The address is incremented or decremented by 1 after each transfer.

Register Offset: C8h (DMA0)
Register Name: DMA0 Transfer Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA0 Transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: C6h (DMA0)
Register Name: DMA0 Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA0 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: C4h (DMA0)
Register Name: DMA0 Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: C2h (DMA0)
Register Name: DMA0 Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA0 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b

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Register Offset: C0h (DMA0)
Register Name: DMA0 Source Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA0 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: DAh (DMA1)
Register Name: DMA1 Control Register
Reset Value : FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{DM}/\overline{IO}$	DDEC	DINC	SM/$\overline{IO}$	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	Rsvd	CHG	ST	$\overline{B}$ /W

The definitions of bit[15:0] for DMA1 are the same as those of bit[15:0] of Register CAh for DMA0.

Register Offset: D8h (DMA1)
Register Name: DMA1 Transfer Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: D6h (DMA1)
Register Name: DMA1 Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA1 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: D4h (DMA1)
Register Name: DMA1 Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: D2h (DMA1)
Register Name: DMA1 Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA 1 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: D0h (DMA1)
Register Name: DMA1 Source Address Low Register
Reset Value : ——

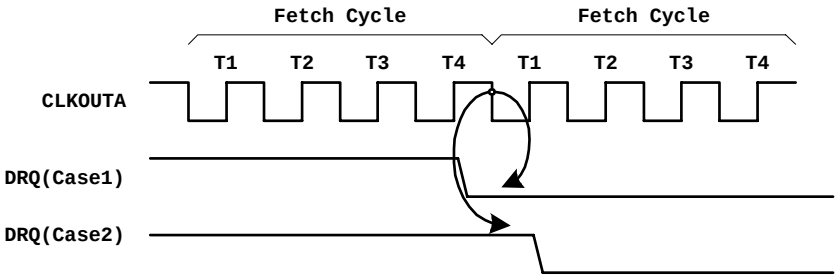
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

14.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of CLKOUTA. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. No DMA acknowledge is provided, since the chip-selects ($\overline{\text{MCSx}}$ and $\overline{\text{PCSx}}$) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

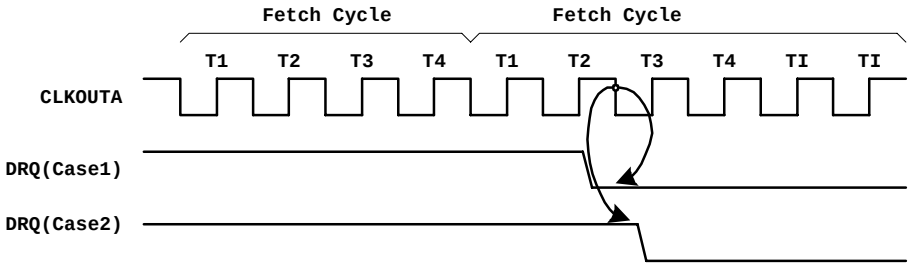
DMA transfers can be either source- or destination-synchronized, and they can also be unsynchronized. The Source-Synchronized Transfers figure shows the typical source-synchronized transfers which provide the source device at least three clock cycles from the time it is acknowledged to de-assert its DRQ line.



NOTES:
Case1 : The current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : The current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

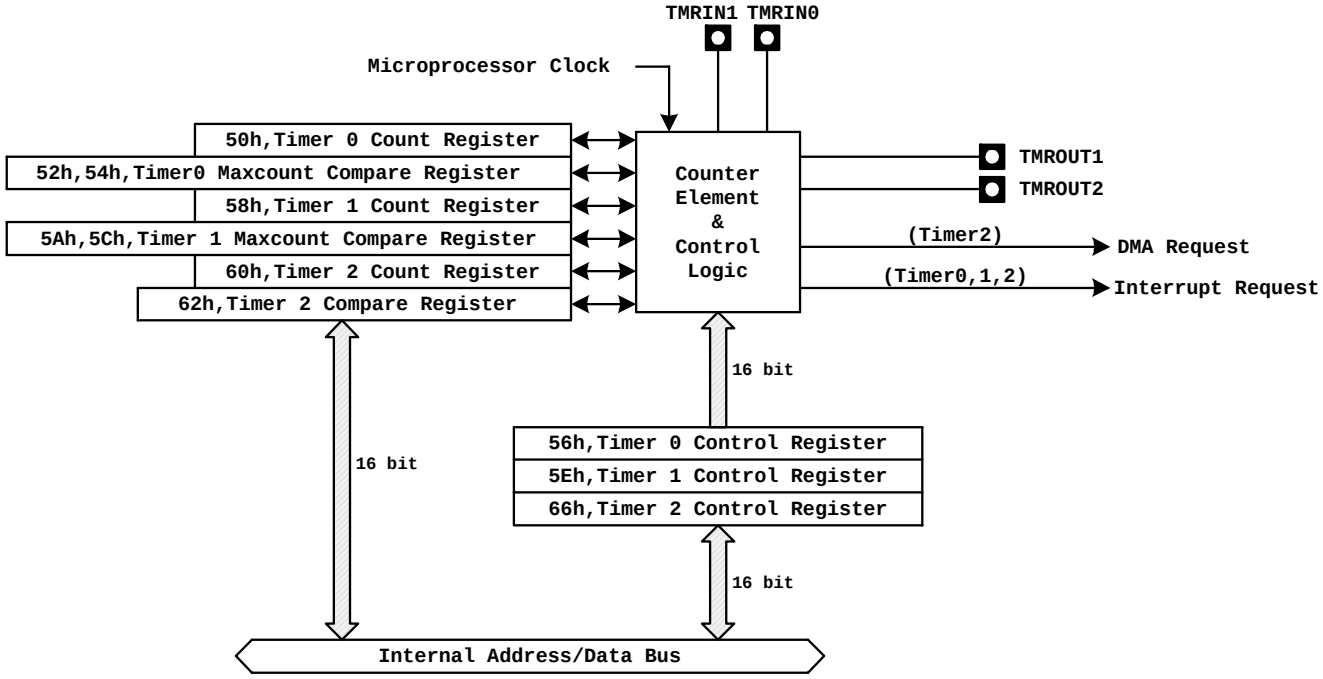
The Destination-Synchronized Transfers figure shows the typical destination-synchronized transfer which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NOTES:
Case1 : The current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : The current destination synchronized transfer will be immediately followed by another DMA transfer.

Destination-Synchronized Transfers

15. Timer Control Unit



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R1100. The timer operation is independent of the CPU. These three timers can be programmed as a timer element or as a counter element. Timer 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1 and TMROUT1), which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected to any external pins. It can be used as a pre-scale to Timer 0 and Timer 1 or as a DMA request source.

Register Offset: 56h
Register Name: Timer 0 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable bit. Set 1: The timer 0 is enabled. Set 0: The timer 0 is inhibited from counting. The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and both the $\overline{INH}$ and EN bits must be in the same write.

14	$\overline{\text{INH}}$	R/W	Inhibit bit. This bit allows selectively updating the EN bit. The $\overline{\text{INH}}$ bit must be set to 1 when the EN bit is written, and both the $\overline{\text{INH}}$ and EN bits must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time when the count reaches Max-Count A or Max-Count B. Set 0: Timer 0 will not issue interrupt requests.
12	RIU	R/W	Register in Use bit. Set 1: The Maxcount Compare B Register of Timer 0 is being used. Set 0: The Maxcount Compare A Register of Timer 0 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set as each time when either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the EN bit (offset 66h.15).
4	RTG	R/W	Re-trigger bit. This bit defines the control function by the input signal of the TMRIN0 pin. When EXT=1 (5Eh.2), this bit is ignored. Set 1: Timer0 Count Register (58h) counts internal events; reset the counting on every TMRIN0 input signal from low to high (rising edge trigger). Set 0: Low input holds the Timer 0 Count Register (58h) value; high input enables the counting which counts internal events. **The definitions of setting the (EXT, RTG)** (0, 0) – Timer 0 counts the internal events if the TMRIN1 pin remains high. (0, 1) – Timer 0 counts the internal events; the count register is reset on every rising transition on the TMRIN1 pin. (1, x) – The TMRIN0 pin input acts as clock source and Timer 0 Count Register is incremented by one every external clock.
3	P	R/W	Pre-scaler bit. This bit and EXT (5Eh.2) define the timer 0 clock source. **The definitions of setting the (EXT, P)** (0, 0) – Timer 0 Count Register is incremented by one every four internal processor clock. (0, 1) – Timer 0 Count Register is incremented by one which is pre-scaled by Timer 2. (1, x) – The TMRIN1 pin input acts as clock source and Timer 0 Count Register is incremented by one every external clock.
2	EXT	R/W	External Clock bit. Set 1: Timer 0 clock source from externals. Set 0: Timer 0 clock source from internals.
1	ALT	R/W	Alternate Compare bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare B, resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and the EN bit will be cleared.

Register Offset: 50h
Register Name: Timer 0 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every four internal processor clocks, pre-scaled by Timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN1 signal.

Register Offset: 52h
Register Name: Timer 0 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

Register Offset: 54h
Register Name: Timer 0 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

Register Offset: 5Eh
Register Name: Timer 1 Mode / Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bit definitions for timer 1 are the same as those of register 56h for timer 0.

Register Offset: 58h
Register Name: Timer 1 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every four internal processor clocks, pre-scaled by Timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN1 signal.

Register Offset: 5Ah
Register Name: Timer 1 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

Register Offset: 5Ch
Register Name: Timer 1 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

Register Offset: 66h
Register Name: Timer 2 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{\text{INH}}$	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The $\overline{\text{INH}}$ bit must be set to 1 when the EN bit is written, and both the $\overline{\text{INH}}$ and EN bits must be in the same write.
14	$\overline{\text{INH}}$	R/W	Inhibit bit. This bit allows selectively updating the EN bit. The $\overline{\text{INH}}$ bit must be set to 1 when the EN bit is written, and both the $\overline{\text{INH}}$ and EN bits must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt requests.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the INT bit (66h.15).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h.15) is cleared and the timer is held after each timer count reaches the maximum count.

Register Offset: 60h
Register Name: Timer 2 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every four internal processor clocks.

Register Offset: 62h
Register Name: Timer 2 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

---

16. Watchdog Timer

Timer 1 can also be configured as a watchdog timer. Software must fist programmed the Timer 1 Mode/Control (5Eh), Count (58h), and Max Count (5Ah, 5Ch) registers and then program the Watchdog Timer Interrupt Control Register (42h) to enable the watchdog timer interrupt , The Timer 1 Count Register must be reloaded at intervals less than the Timer 1 Maxcount value to assure the watchdog interrupt is not occurred.

Register Offset: 42h
Register Name: Watchdog Timer Control Register
Reset Value : 000Fh

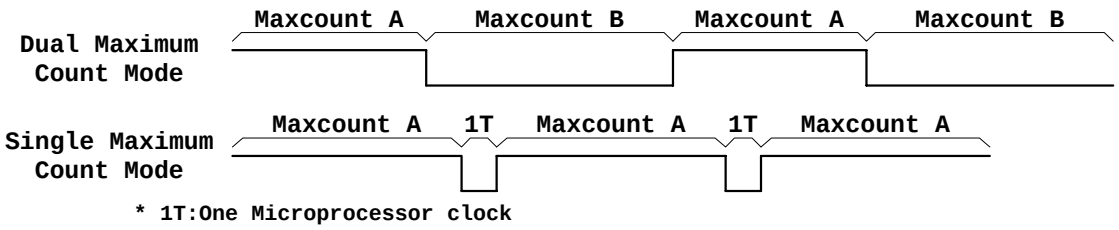
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd												MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the watchdog timer. Set 0: Enable the watchdog timer interrupt.
2-0	PR[2:0]		Priority. The priority selection: PR2, PR1, PR0 -- Priority 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

16.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and timer1 can be configured to single or dual Maximum Compare count mode, the TMROUT0 or TMROUT1 signals can be used to generate waveform of various duty cycles.

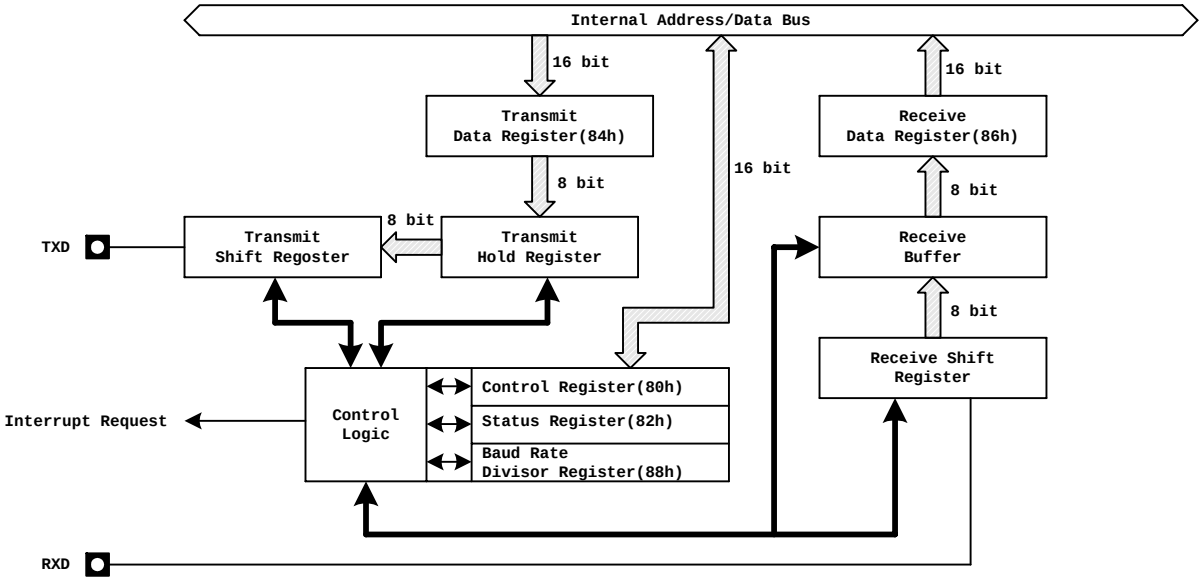


Timer/Counter Unit Output Modes

17. Asynchronous Serial Port

R1100 asynchronous serial port provides the TXD, RXD pins for the full duplex bi-directional data transfer and without handshaking signals. The UART port supports: 8-bit or 7-bit data transfer; odd parity, even parity, or no parity; 1 or 2 stop bits. DMA transfers through the serial port are not supported

The receive/transmit clock is based on the microprocessor clock. The serial port can be used in power-saved mode, but the transfer rate must be adjusted to correctly reflect the new internal operating frequency. Software is programmed through the 80h, 82h, 84h, 86h, and 88h registers to configure the asynchronous serial port.



Serial Port Block Diagram

Register Offset: 80h

Register Name: Serial Port Control Register

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd				TXIE	RXIE	LOOP	BRK	BRKVAL	PMODE		WLGN	STP	TMOD	RSIE	RMODE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TXIE	R/W	Transmitter Ready Interrupt Enable. When the Transmit Holding Register is empty (the THRE bit in the Status Register is set), an interrupt will occur.
10	RXIE	R/W	Receive Data Ready Interrupt Enable. When the receive buffer contains valid data (the RDR bit in Status Register is set), an interrupt will be generated.
9	LOOP	R/W	Loopback. Set 1: The serial port in the loopback mode. In this mode, the transmit shift register is connected to the transmit shift register internal and the TXD pin output high. It provides the serial port testing in this mode.
8	BRK	R/W	Send Break. It should to check the TEMT bit (82h.6) is a 1 before setting the BRK bit. Set 1: The serial port send a frame of continues level output on the TXD pin and the output level depends on the BRAVAL bit status, when any data is written to transmit data register.
7	BRKVAL	R/W	Break Value. Set 1: TXD pin continuous drive high level signal during the send break operation. Set 0: TXD pin continuous drive low level signal during the send break operation.
6-5	PMODE	R/W	Parity Mode. Parity generation and checking during transmission and reception. Parity mode selection by (Bit 6, Bit 5): (0, x) – No parity bit in frame. (1, 0) – Odd number of 1s in frame. (1, 1) – Even number of 1s in frame.
4	WLGN	R/W	Word Length. Set 1: The serial port sends and receives 8 bits of data per frame. Set 0: The serial port sends and receives 7 bits of data per frame.
3	STP	R/W	Stop Bits. Set 1: Two stop bits are used to signify the end of a frame. Set 0: One stop bit is used to signify the end of a frame.
2	TMODE	R/W	Transmit Mode. Set 1: Enable the transmit section of the serial port. Set 0: Disable the transmit section of the serial port.
1	RSIE	R/W	Receive Status interrupt Enable. Set 1: Enable the receive section of serial port to generate an interrupt Set 0: Disable the receive section of serial port to generate an interrupt
0	RMODE	R/W	Receive Mode. Set 1: Enable the receive section of the serial port. Set 0: Disable the receive section of the serial port.

Register Offset: 82h
Register Name: Serial Port Status Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd									TEMT	THRE	RDR	BRK1	FER	PER	OERd

Bit	Name	Attribute	Description
15-7	Rsvd	RO	Reserved.
6	TEMT	RO	Transmitter Empty. This bit is read only. When the Transmit Shift Register is empty, this bit will be set.
5	THRE	RO	Transmit Holding Register Empty. Read only. When the Transmit Hold Register is ready to accept data, this bit will be set. This bit will be reset when data is written to the Transmit Hold Register.
4	RDR	RO	Receive Data Ready. Read only. When the receive data register is ready to read, this bit is 1. When the bit is 0, the receive data register dose not contain valid data. This bit will be cleared by H/W when reading the receive data register.
3	BRKI	R/W	Break Interrupt. It indicates that a break has been receive when this bit is set 1 and it will generate a serial pot interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.
2	FER	R/W	Framing Error detected. This bit should be reset by software. This bit is set when a framing error is detected.
1	PER	R/W	Parity Error Detected. This bit should be reset by software. This bit is set when a parity error (for mode 1 and mode 3) is detected.
0	OER	R/W	Overrun Error Detected. This bit should be reset by software. This bit is set when an overrun error is detected.

Register Offset: 84h
Register Name: Serial Port 0 Transmit Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TDATA							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	TDATA	RO	Transmit Data. Transmit Data. Software writes this register with data to be transmitted on the serial port. The THRE bit (82h.5) should be read as a 1 before writing this register to avoid overwriting data to this register. When writing data to this register, the THRE bit will be cleared by H/W in the same time.

Register Offset: 86h
Register Name: Serial Port Receive Data Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDATA							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	RDATA	RO	Receive DATA. In order to avoid invalid data being read, the RDR bit (82h.4) should be read as 1 before this register is read.

Register Offset: 88h
Register Name: Serial Port Baud Rate Divisor Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUDDIV															

Bit	Name	Attribute	Description
15-0	BAUDDIV	R/W	Baud Rate Divisor. The general formula for baud rate divisor is **Baud Rate = Microprocessor Clock / (16 x BAUDDIV)**. For example, if the microprocessor clock is 22.1184MHz and the BAUDDIV=12 (decimal), the baud rate of the serial port will be 115.2k.

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18. Synchronous Serial Port

There are four pins for synchronous serial port interface, which is half duplex, bi-directional data transfer. The synchronous serial interface operates in a master/slave configuration, and the synchronous serial port of R1100 as a master mode. The SCLK frequency is affected by the reduced microprocessor clock frequency when it's in power-save mode. Software is programmed the 10h, 12h, 14h,16h, 18h to configured the synchronous serial port interface.

Register Offset: 10h
Register Name: Synchronous Serial Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd													RE/TE	DR/DT	PB

Read only register that indicates the state of the SSI port.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2	RE/TE		Receive/Transmit Error Detect. Set 1: Either a read of Synchronous Serial Receive register or a write to one transmit registers while the SSI is busy (PB=1). Set 0: SDEN output is inactive.
1	DR/TR		Data Receive/Transmit Complete. Set 1: End of the transfer of data bit 7 (SCLK rising edge) during a transmit or receive operation. Set 0: When the SSR register is read, when one of the SSD0 or SSD1 registers is written, when the SSS register is read, or when both SDEN0 and SDEN1 become inactive.
0	PB		SSI port Busy. Set 1: a transmit or receive operation is in progress. Set 0: the port is ready to transmit or receive data.

Register Offset: 12h
Register Name: Synchronous Serial Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd										SCLKDIV		Rsvd		DE1	DE0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.

5-4	SCLKDIV		SCLK Divide. SCLKDIV: 00b = Processor clock/2; 01b = Processor clock/4; 10b = Processor clock/8; 11b = Processor clock/16
3-2	Rsvd	RO	Reserved.
1	DE1		SDEN1 Enable. Set 1: SDEN1 pin is held High. Set 0: SDEN1 pint is Low.
0	DE0		SDEN0 Enable. Set 1: SDEN0 pin is held High. Set 0: SDEN0 pint is Low.

Register Offset: 14h
Register Name: Synchronous Serial Transmit 1 Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd								SD							

Synchronous Serial Transmit 1 Register contains data to be transferred from the processor to the peripheral on a write operation

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	SD		Send Data. Data to transmit over the SDATA pin.

Register Offset: 16h
Register Name: Synchronous Serial Transmit 0 Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd								SD							

Synchronous Serial Transmit 0 Register contains data to be transferred from the processor to the peripheral on a write operation.

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	SD		Send Data. Data to transmit over the SDATA pin.

Register Offset: 18h
Register Name: Synchronous Serial receive Register
Reset Value : ----

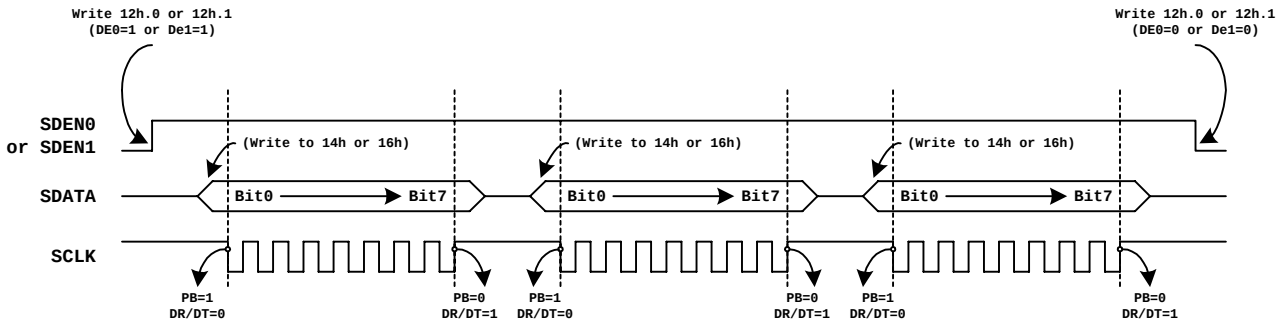
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd								SD							

Synchronous Serial receive Register contains the data transferred from the peripheral to the processor on a read operation.

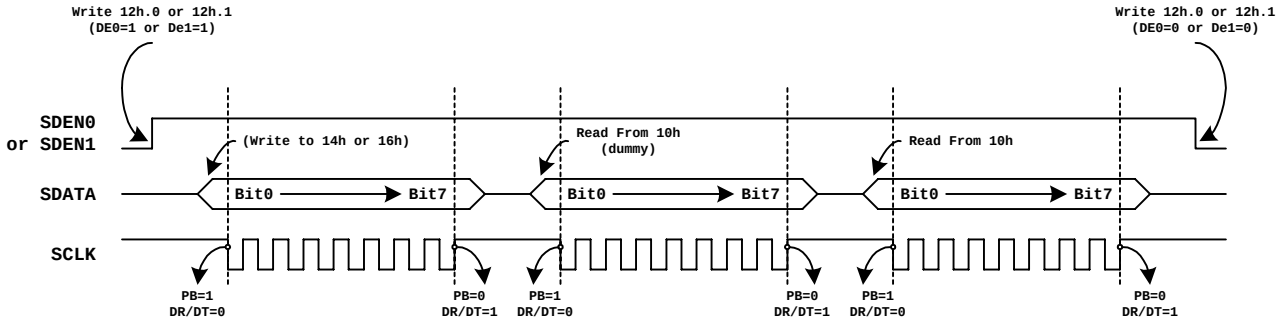
Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	SD		Receive Data. Data received over the SDATA pin.

18.1 Synchronous serial port operation

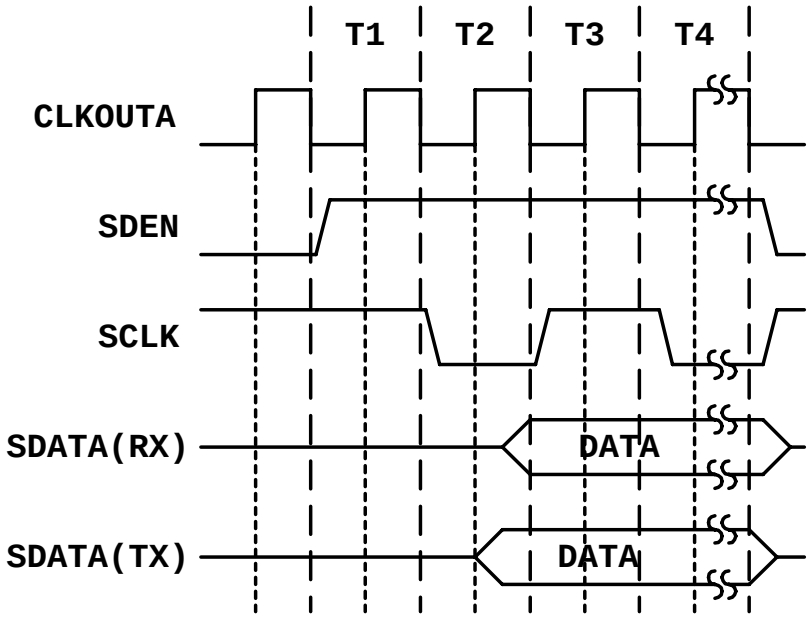
The following figures show the data transmit and data receive operation.



Synchronous Serial Port Multiple Write



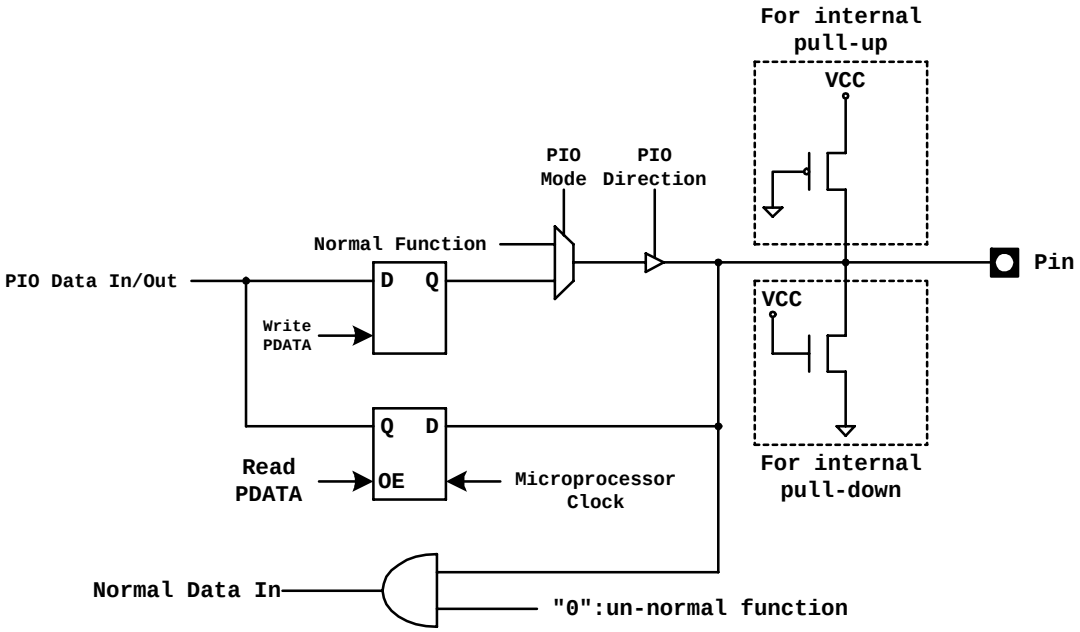
Synchronous Serial Port Multiple Read



Synchronous Serial Interface Waveforms

19. PIO Unit

The R1100 provides 32 programmable I/O signals, which are multi-function pins with other signals of normal functions. Through programming Registers 7Ah, 78h, 76h, 74h, 72h and 70h, software can configure these multi-function pins as PIOs or normal functions.



PIO pin Operation Diagram

19.1 PIO Multi-Function Pins

PIO No.	Pin No. (PQFP)	Multi Function	Reset status/PIO internal resistor
0	72	TMRIN1	Input with 10k pull-up
1	73	TMROUT1	Input with 10k pull-down
2	59	$\overline{\text{PCS6}}$ /A2	Input with 10k pull-up
3	60	$\overline{\text{PCS5}}$ /A1	Input with 10k pull-up
4	48	DT/$\overline{\text{R}}$	Normal operation/ Input with 10k pull-up
5	49	DEN	Normal operation/ Input with 10k pull-up
6	46	SRDY	Normal operation/ Input with 10k pull-down
7	22	A17	Normal operation/ Input with 10k pull-up
8	20	A18	Normal operation/ Input with 10k pull-up
9	19	A19	Normal operation/ Input with 10k pull-up
10	74	TMROUT0	Input with 10k pull-down
11	75	TMRIN0	Input with 10k pull-up

12	77	DRQ0	Input with 10k pull-up
13	76	DRQ1	Input with 10k pull-up
14	50	$\overline{\text{MCS0}}$	Input with 10k pull-up
15	51	$\overline{\text{MCS1}}$	Input with 10k pull-up
16	66	$\overline{\text{PCS0}}$	Input with 10k pull-up
17	65	$\overline{\text{PCS1}}$	Input with 10k pull-up
18	63	$\overline{\text{PCS2}}$	Input with 10k pull-up
19	62	$\overline{\text{PCS3}}$	Input with 10k pull-up
20	3	SCLK	Input with 10k pull-up
21	100	SDATA	Input with 10k pull-up
22	2	SDEN0	Input with 10k pull-down
23	1	SDEN1	Input with 10k pull-down
24	68	$\overline{\text{MCS2}}$	Input with 10k pull-up
25	69	$\overline{\text{MCS3}}$ / $\overline{\text{RFSH}}$	Input with 10k pull-up
26	97	$\overline{\text{UZI}}$	Input with 10k pull-up
27	98	TXD	Input with 10k pull-up
28	99	RXD	Input with 10k pull-up
29	96	S6/ $\overline{\text{CLKDIV2}}$	Input with 10k pull-up
30	52	INT4	Input with 10k pull-up
31	54	INT2	Input with 10k pull-up

Register Offset: 7Ah
Register Name: PIO Data 1 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [31:16]															

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data bits. These bits PDATA[31:16] are mapped to PIO[31:16], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 78h
Register Name: PIO Direction 1 Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [31:16]															

Bit	Name	Attribute	Description
15-0	PDIR[31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input. Set 0: Configure the PIO pin as an output or as normal pin function.

Register Offset: 76h
Register Name: PIO Mode 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE [31:16]															

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode bits. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the PIO pin function: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

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Register Offset: 74h
Register Name: PIO Data 0 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [15: 0]															

Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data bits. These bits PDATA[15:0] are mapped to PIO[15:0], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 72h
Register Name: PIO Direction 0 Register
Reset Value : FC0Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [15:0]															

Bit	Name	Attribute	Description
15-0	PDIR[15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input. Set 0: Configure the PIO pin as an output or as normal pin function.

Register Offset: 70h
Register Name: PIO Mode 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE [15:0]															

Bit	Name	Attribute	Description
15-0	PMODE[15:0]	R/W	PIO Mode bits.

20. INSTUCTION SET OPCODES AND CLOCK CYCLES

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	

Function	Format				Clocks	Notes
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	
JNO = not overflow	01110001	disp			1/9	
JNS = not sign	01111001	disp			1/9	

Function	Format			Clocks	Notes
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = Retum from procedure					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = Unconditional jump					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

21. R1100 Execution Timing

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.
2. No wait states or bus holds occur.
3. All word -data are located on even-address boundaries.
4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline stages for single micro operations (one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For memory function *u*OP)

4.1 *Memory read u*OP needs 6 cycles for bus.

Pipeline stages for *memory read u*OP (6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP needs 1 cycle if it has no previous *memory push u*OP, and 5 cycles if it has previous *memory push* or *memory write u*OP.

Pipeline stages for *memory push u*OP after *memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8-bit operations need both 8 cycles, for 16-bit operations need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*unconditional fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

These 9 cycles cause branch penalty

→ Fetch → Decode → following stages...(New *u*OP)

***Note**: op_r: operand read stage; EA: Calculate Effective Address stage; Idle: Bus Idle stage; T0..T3: Bus T0..T3 stage; Access: Access data from cache memory stage.*

22. I/O Characteristics of Each Pin

Pin NO.	Pin Name	Characteristics
71	$\overline{RST}$	Schmitt Trigger , 3.3V to 5V tolerant TTL input, with internal 75K pull-up resistor
8	ARDY	Schmitt Trigger , 3.3V to 5V tolerant TTL input, with internal 75K pull-down resistor
45 47	HOLD NMI	3.3V to 5V tolerant CMOS input, with internal 75K pull-down resistor
56 55	INT0 INT1/$\overline{SELECT}$	Schmitt Trigger , 3.3V to 5V tolerant TTL input, with internal 75K pull-down resistor
16	CLKOUTA	8 mA 3-State CMOS output, 3.3V
17	CLKOUTB/TDI	Bi-direction I/O , with 75 K internal pull-down resistor 8mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
9	$\overline{S2}$ /TDO	Bi-direction I/O , with 75 K internal pull-up resistor 16mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
10 11	$\overline{S1}$ /TCK $\overline{S0}$ /TMS	Bi-direction I/O , with 75 K internal pull-down resistor 4mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
43 6 5	$\overline{WLB}$ $\overline{RD}$ $\overline{WR}$	12 mA 3-State CMOS output, 3.3V
19 20 22	A19/PIO9 A18/PIO8 A17/PIO7	Bi-direction I/O , with enabled/disabled 10 K internal pull-up resistor when active as PIO, for normal function the 10k pull-up resistor is disabled. 16mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 39 40	A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	16 mA 3-State CMOS output, 3.3V

78 80 82 84 86 88 91 94 79 81 83 85 87 90 93 95	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	Bi-direction I/O , 16mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
7	ALE	Bi-direction I/O , with 75 K internal pull-down resistor 8mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
46 74 73 2 1	SRDY/PIO6 TMROUT0/PIO10 TMROUT1/PIO1 SDEN0/PIO22 SDEN1/PIO23	Bi-direction I/O , with enabled/disabled 10 K internal pull-down resistor when active as PIO, for normal function the 10k pull-down resistor is disabled. 8mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
4	$\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ / $\overline{TRST}$	Bi-direction I/O , with 75 K internal pull-up resistor 4mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
42	$\overline{\text{WHB}}$	Bi-direction I/O , with 75 K internal pull-up resistor 12mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
44	HLDA	4 mA CMOS output, 3.3 V
54 52	INT2/$\overline{\text{INTA0}}$/PIO31 INT4/PIO30	Bi-direction I/O , with enabled/disabled 10 K internal pull-up resistor when active as PIO, for normal function the 10k pull-up resistor is disabled. 8mA TTL output, 3.3 V 3.3 V to 5V tolerant Schmitt Trigger input
53	INT3/$\overline{\text{INTA1}}$/IRQ	Bi-direction I/O , with 75 K internal pull-down resistor 8mA TTL output, 3.3 V 3.3 V to 5V tolerant Schmitt Trigger input
57 58	$\overline{\text{UCS}}$/$\overline{\text{ONCE1}}$ $\overline{\text{LCS}}$/$\overline{\text{ONCE0}}$	Bi-direction I/O , with 10 K internal pull-up resistor 8mA TTL output, 3.3 V 3.3 V to 5V tolerant Schmitt Trigger input

49	$\overline{DEN}$/PIO5	Bi-direction I/O , with enabled/disabled 10 K internal pull-up resistor when active as PIO, for normal function the 10k pull-up resistor is disabled. 8mA TTL output, 3.3 V 3.3 V to 5V tolerant TTL input
48	DT$\overline{R}$/PIO4	
66	$\overline{PCS0}$/PIO16	
65	$\overline{PCS1}$/PIO17	
63	$\overline{PCS2}$/PIO18	
62	$\overline{PCS3}$/PIO19	
60	$\overline{PCS5}$/A1/PIO3	
59	$\overline{PCS6}$/A1/PIO3	
50	$\overline{MCS0}$/PIO14	
51	$\overline{MCS1}$/PIO15	
68	$\overline{MCS2}$/PIO24	
69	$\overline{MCS3}$/$\overline{RFSH}$/PIO25	
97	$\overline{UZI}$/PIO26	
96	S6/$\overline{CLKDIV2}$/PIO29	
75	TMRIN0/PIO11	
72	TMRIN1/PIO0	
77	DRQ0/PIO12	
76	DRQ1/PIO13	
98	TXD/PIO27	
99	RXD/PIO28	
100	SDATA/PIO21	
3	SCLK/PIO20	

23. DC Characteristics

Recommended DC Operating Conidtions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
Vih	Input High Voltage(1)	2		Vcc+0.5	V
Vih1	Input High Voltage(RES)	3		Vcc+0.5	V
Vih2	Input High Voltage(X1)	3		Vcc+0.5	V
Vil	Input Low Voltage	-0.5	0	0.8	V

Notes 1: RES, X1 pins not included

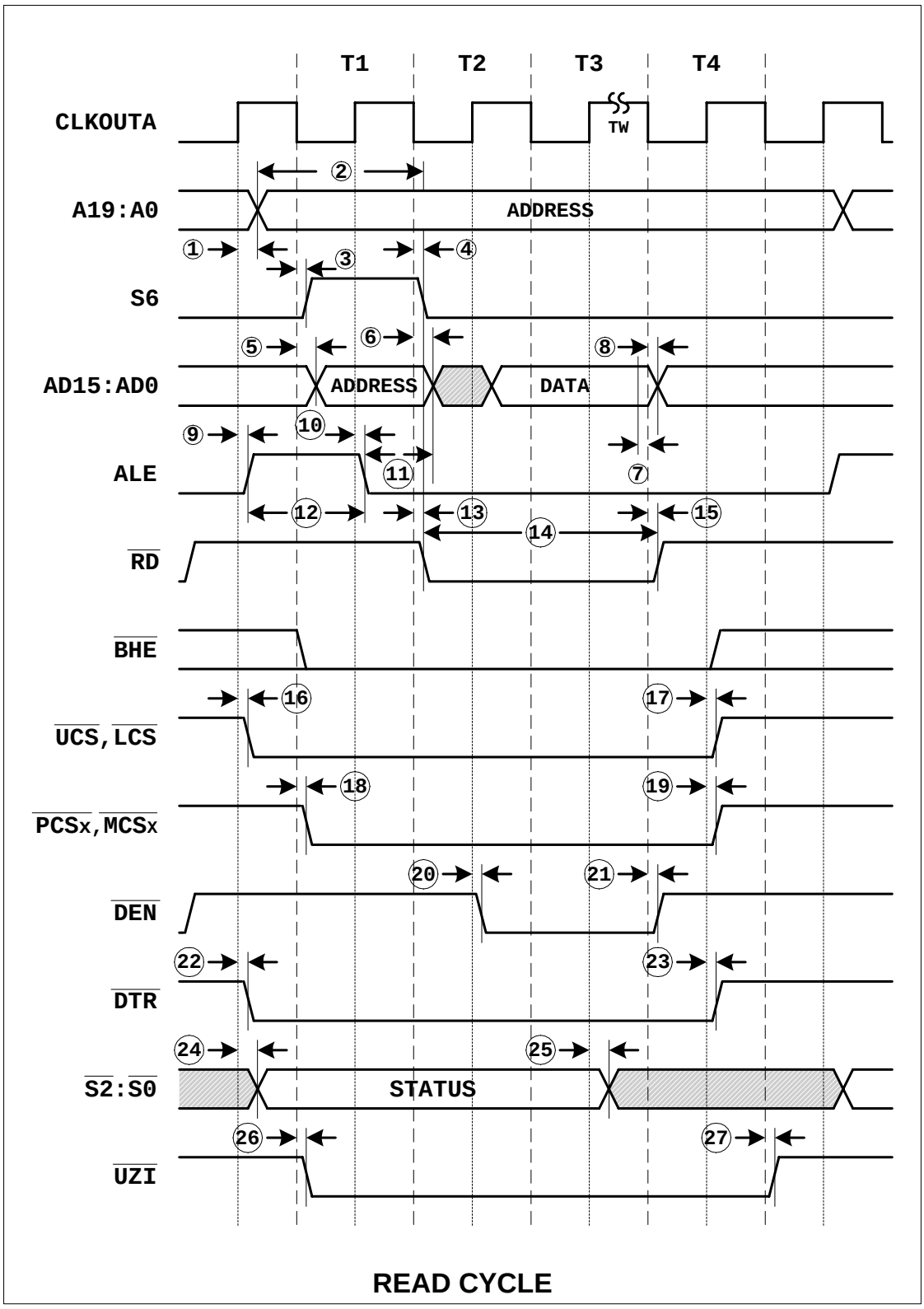
DC Elcetrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Ili	Input Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
Ili(with 10K pull R)	Input leakage Current with Pull_R 10K enable	Vcc=Vmax Vin=GND to Vmax	-300	300	uA
Ili(with 75K pull R)	Input leakage Current with Pull_R 75K enable	Vcc=Vmax Vin=GND to Vmax	-100	100	uA
Ilo	Output Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
VOL	Output Low Voltage	Iol=6mA, Vcc=Vmin		0.4	V
VOH	Output High Voltage	Ioh=-6mA Vcc=Vmin	2.4		V
Icc	Max Operating Current	Vcc = 3.6V 80MHz (*2)		180	mA

Note 1: Vmax=3.6V Vmin=3V

Note 2: While Reset Cycle, external Xin = 20 MHz, PLL 4 times.

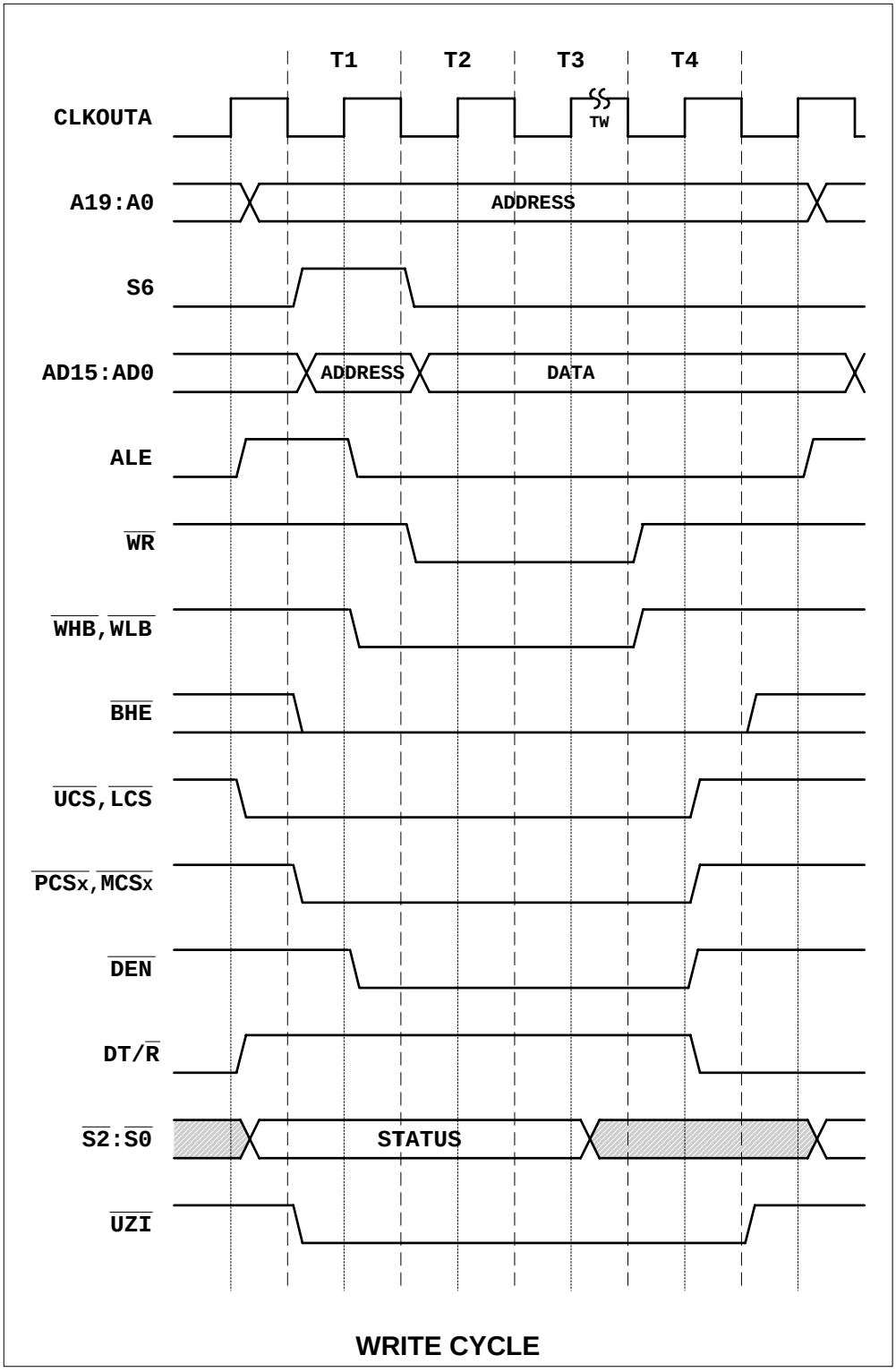
24. AC Characteristics



READ CYCLE

Read Cycle

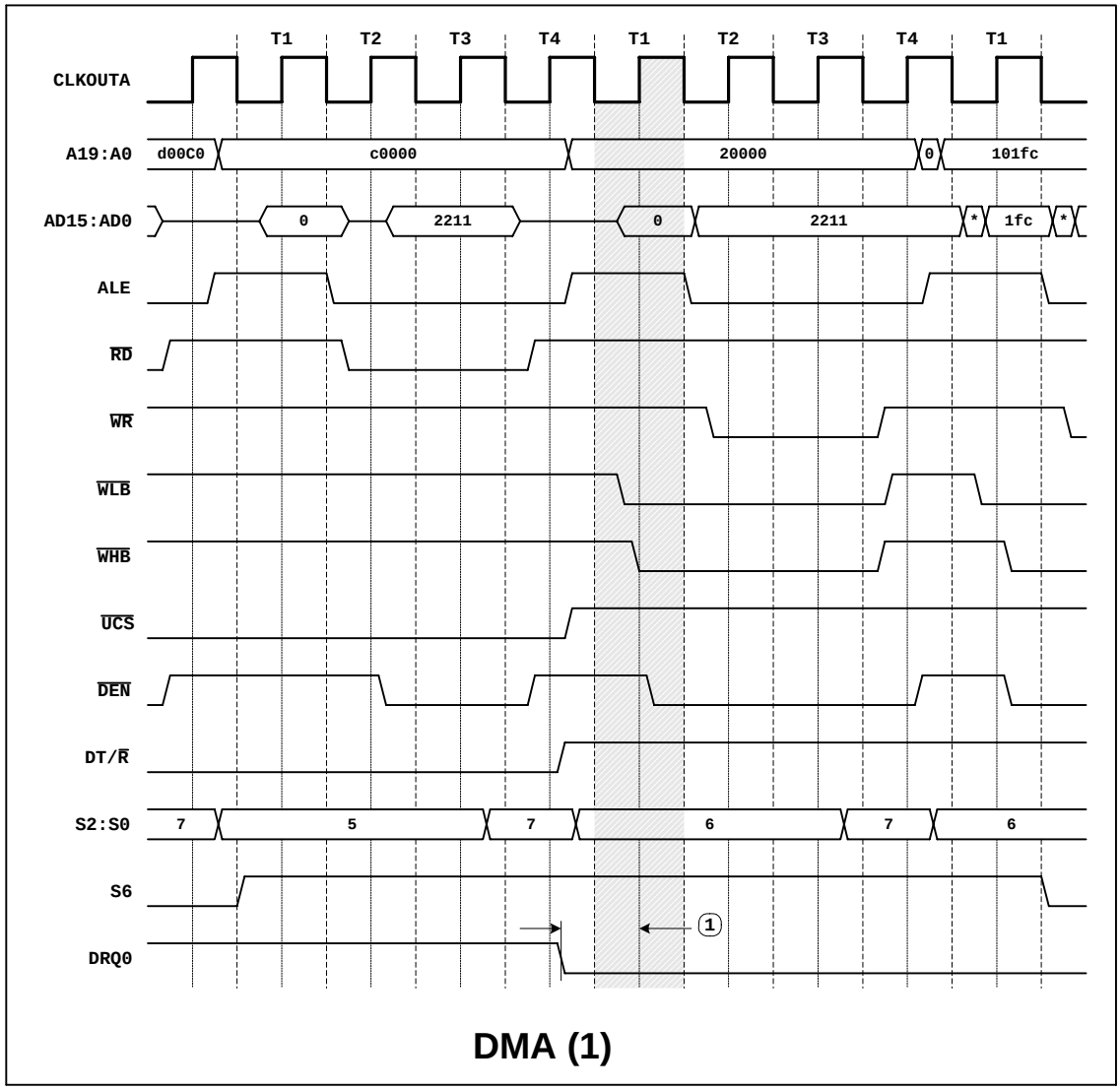
No.	Description	Min	Max	Unit
1	CLKOUTA high to A Address Valid	0	8	ns
2	A address valid to RD low	1.5T-8		ns
3	S6 active delay	0	8	ns
4	S6 inactive delay	0	8	ns
5	AD address Valid delay	0	8	ns
6	Adress Hold	0	8	ns
7	Data in setup	8		ns
8	Data in hold	0		ns
9	ALE active delay	0	8	ns
10	ALE inactive delay	0	8	ns
11	Address Valid after ALE inactive	T/2-5		ns
12	ALE width	T-5		ns
13	RD active delay	0	8	ns
14	RD Pulse width	2T-5		ns
15	RD inactive delay	0	8	ns
16	CLKOUTA HIGH to <CS UCS valid	0	8	ns
17	UCS, LCS inactive delay	0	8	ns
18	PCS, MCS active delay	0	8	ns
19	PCS, MCS inactive delay	0	8	ns
20	DEN active delay	0	8	ns
21	DEN inactive delay	0	8	ns
22	DTR active delay	0	8	ns
23	DTR inactive delay	0	8	ns
24	Status active delay	0	8	ns
25	Status inactive delay	0	8	ns
26	UZI active delay	0	8	ns
27	UZI inactive delay	0	8	ns


T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB, WLB
BHE
UCS, LCS
PCSx, MCSx
DEN
DT/R
S2:S0
STATUS
UZI

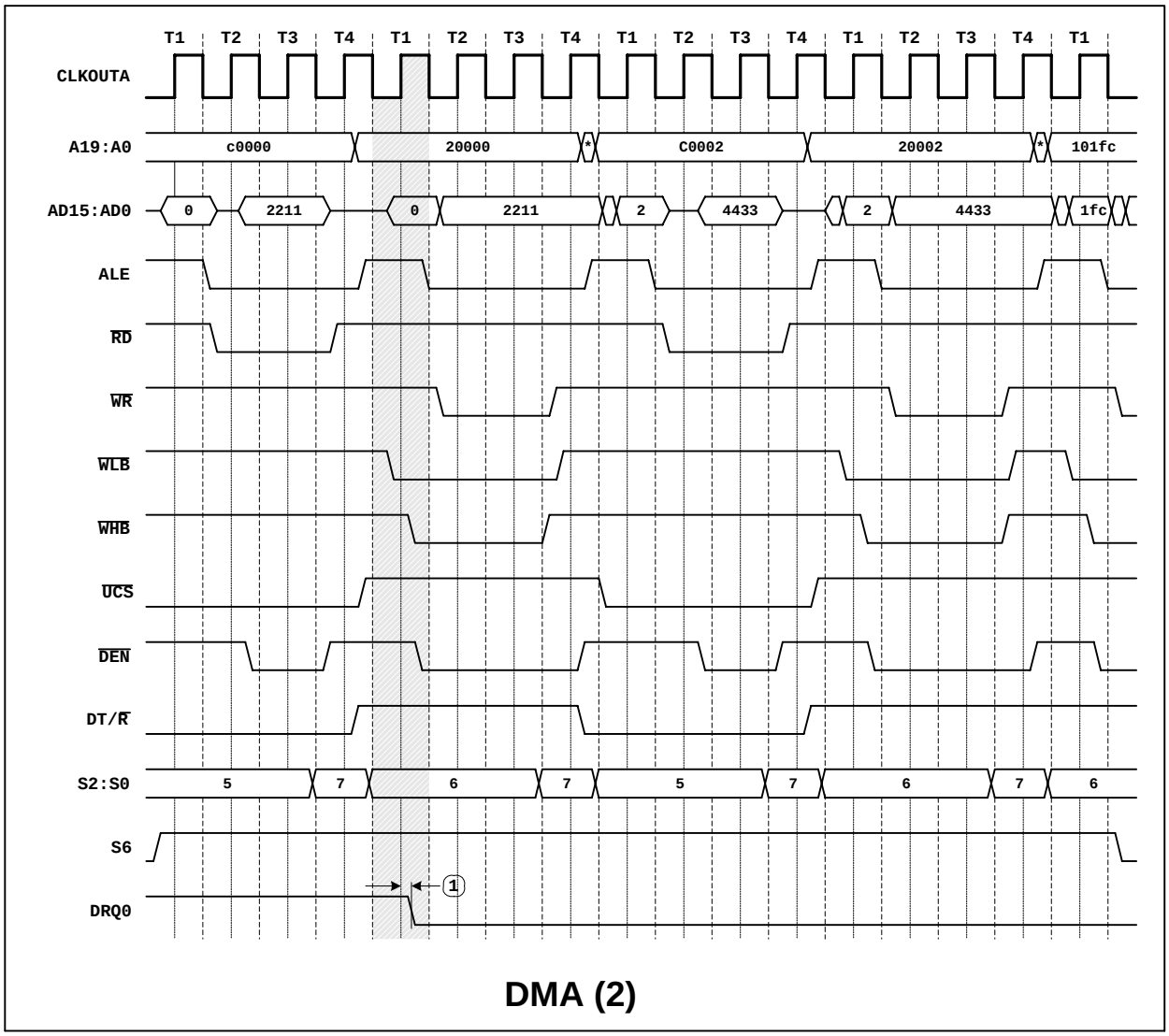
WRITE CYCLE

Write Cycle

No.	Description	Min	Max	Unit
1	CLKOUTA high to A Address Valid	0	8	ns
2	A address valid to WR low	1.5t-8		ns
3	S6 active delay	0	8	ns
4	S6 inactive delay	0	8	ns
5	AD address Valid delay	0	8	ns
6	Adress Hold	0	8	ns
7	ALE active delay	0	8	ns
8	ALE width	T-5		ns
9	ALE inactive delay	0	8	ns
10	Address Valid after ALE inactive	T/2-5		ns
11	WR active delay	0	8	ns
12	WR Pulse width	2T-5		ns
13	WR inactive delay	0	8	ns
14	WHB, WLB active delay	0	9	ns
15	WHB, WLB inactive delay	0	9	ns
16	BHE active delay	0	8	ns
17	BHE inactive delay	0	8	ns
18	CLKOUTA HIGH to LCS UCS valid	0	8	ns
19	UCS, LCS inactive delay	0	8	ns
20	PCS, MCS active delay	0	8	ns
21	PCS, MCS inactive delay	0	8	ns
22	DEN active delay	0	8	ns
23	DEN inactive delay	0	8	ns
24	DTR active delay	0	8	ns
25	DTR inactive delay	0	8	ns
26	Status active delay	0	8	ns
27	Status inactive delay	0	8	ns
28	UZI active delay	0	8	ns
29	UZI inactive delay	0	8	ns


T1
T2
T3
T4
T1
T2
T3
T4
T1
CLKOUTA
A19:A0
d00C0
c0000
20000
0
101fc
AD15:AD0
0
2211
0
2211
*
1fc
*
ALE
RD
WR
WLB
WHB
UCS
DEN
DT/R
S2:S0
7
5
7
6
7
6
S6
1
DRQ0

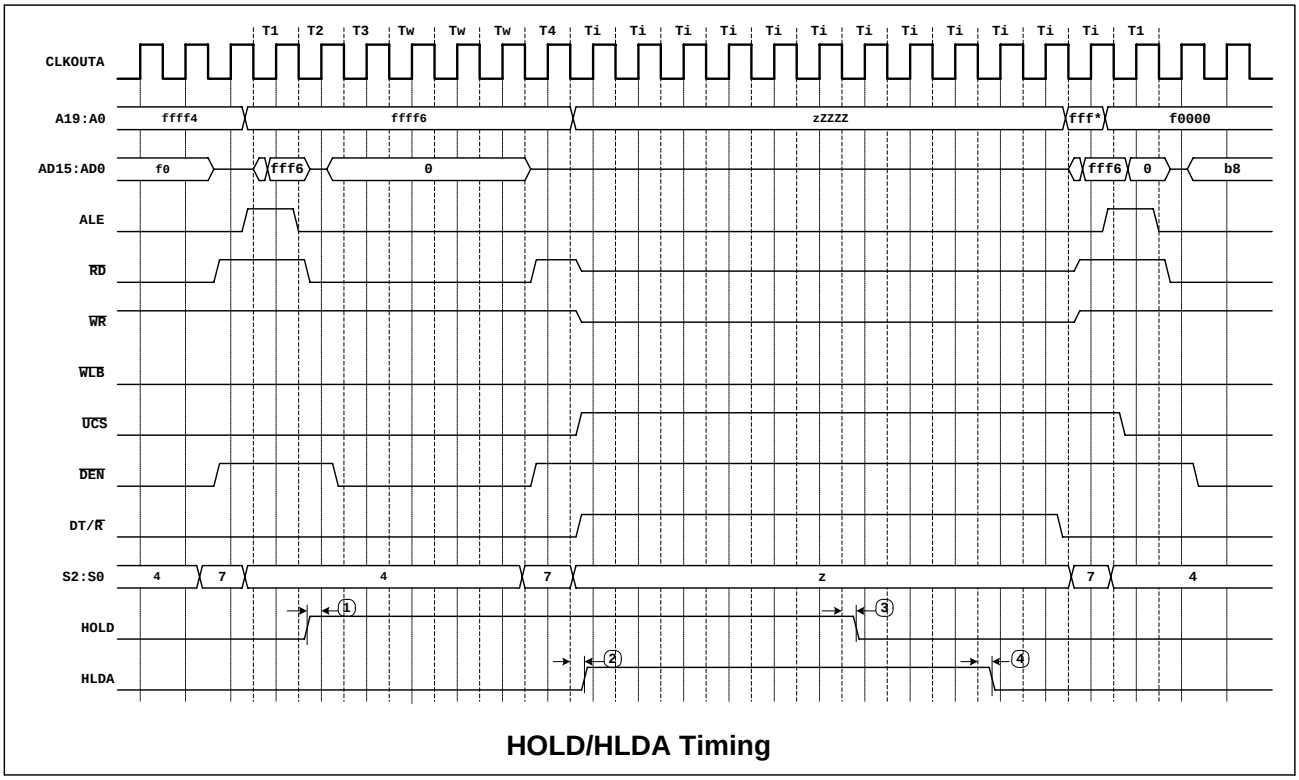
DMA (1)



DMA (2)

DMA(1)/(2) timing

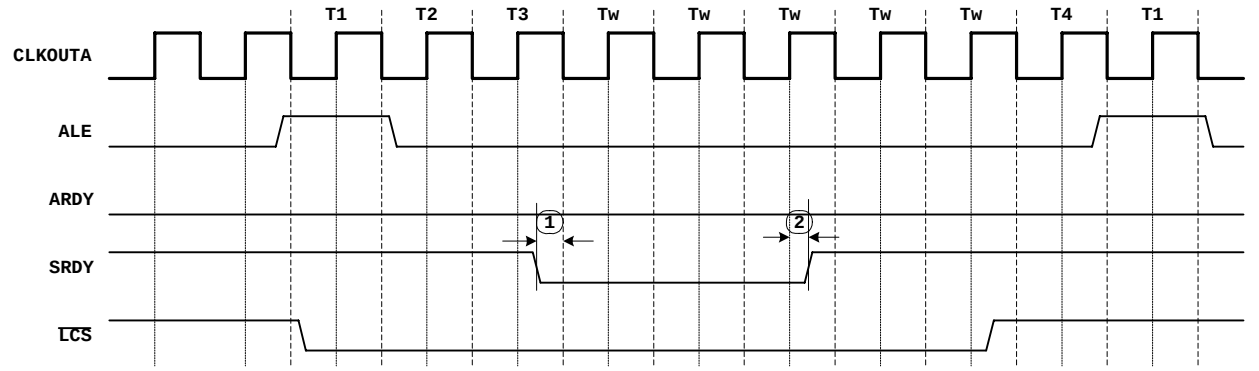
No.	Description	Min	Max	Unit
1	DRQ is confirmed time	5		ns



HOLD/HLDA Timing

Hold timing

No.	Description	Min	Max	Unit
1	HOLD setup time	8		ns
2	HLDA valid delay	0	8	ns
3	HOLD hold time	0		ns
4	HLDA valid delay	0	8	ns



SRDY Timing

SRDY timing

No.	Description	Min	Max	Unit
1	SRDY transition setup time	8		ns
2	SRDY transition hold time	0		ns

DRAM Read Cycle

No.	Description	Min	Max	Unit
1	CLKOUTA low to A Address Valid	0	8	ns
2	Data setup time	8		ns
3	Data hold time	0		ns
4	CLKOUTA high to Row address valid	0	8	ns
5	CLKOUTA low to Column address valid	0	8	ns
6	CLKOUTA low to RAS active	0	8	ns
7	CLKOUTA high to RAS inactive	0	8	ns
8	CLKOUTA high to CAS active	0	8	ns
9	CLKOUTA low to RAS inactive	0	8	ns
10	CLKOUTA low to RD active	0	8	ns
11	CLKOUTA low to RD inactive	0	8	ns

DRAM Write Cycle

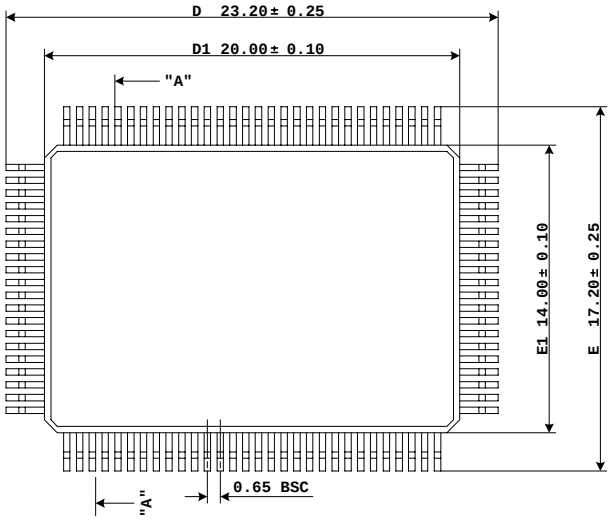
No.	Description	Min	Max	Unit
1	CLKOUTA low to A Address Valid	0	8	ns
2	CLKOUTA low to AD Data Valid	0	8	ns
3	CLKOUTA high to Row address valid	0	8	ns
4	CLKOUTA low to Column address valid	0	8	ns
5	CLKOUTA low to RAS active	0	8	ns
6	CLKOUTA high to RAS inactive	0	8	ns
7	CLKOUTA high to CAS active	0	8	ns
8	CLKOUTA low to RAS inactive	0	8	ns
9	CLKOUTA low to WR active	0	8	ns
10	CLKOUTA low to WR inactive	0	8	ns

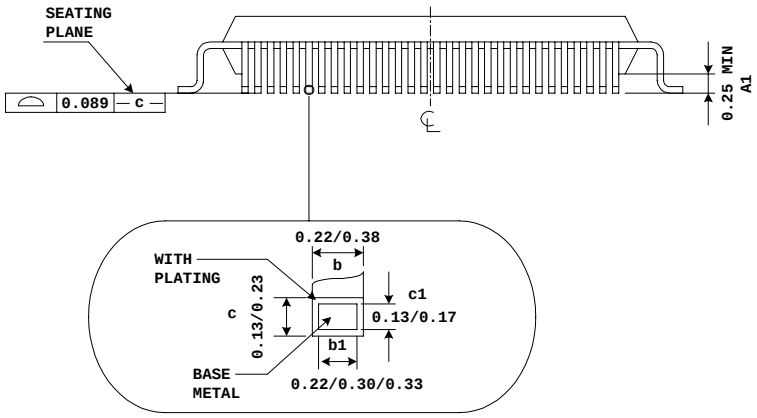
DRAM Refresh Cycle

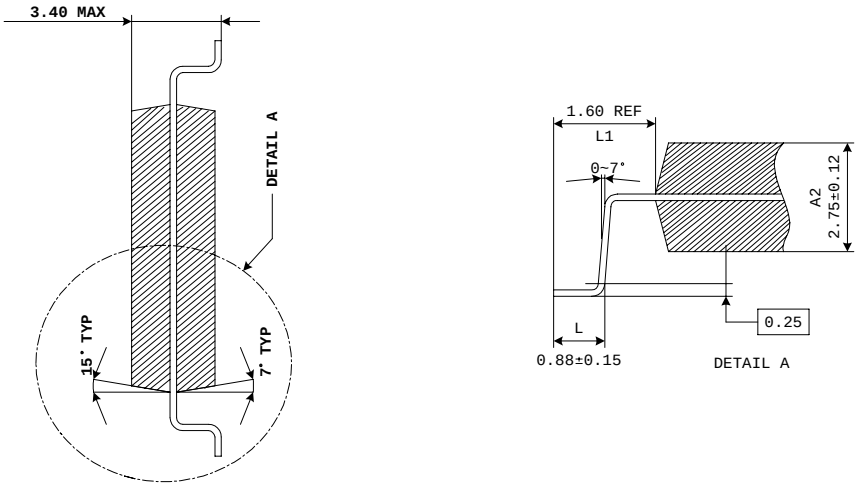
No.	Description	Min	Max	Unit
1	CLKOUTA high to Data drive FFFF	0	8	ns
2	CLKOUTA high to Row address valid	0	8	ns
4	CLKOUTA low to Column address valid	0	8	ns
5	CLKOUTA high to RAS active	0	8	ns
6	CLKOUTA low to RAS inactive	0	8	ns
7	CLKOUTA high to CAS active	0	8	ns
8	CLKOUTA low to RAS inactive	0	8	ns
9	CLKOUTA low to RD active	0	8	ns
10	CLKOUTA low to RD inactive	0	8	ns

25. Package Information

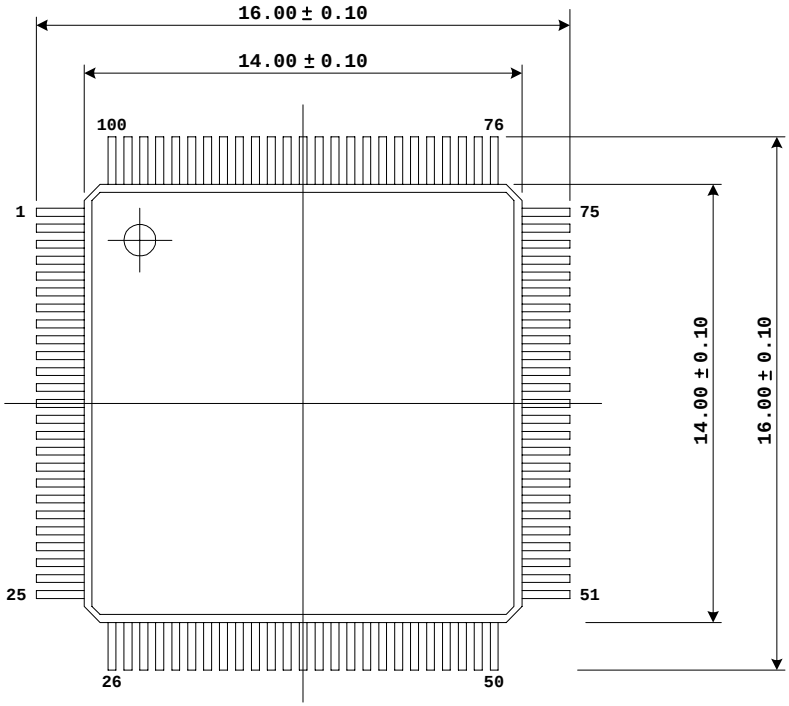
25.1 PQFP

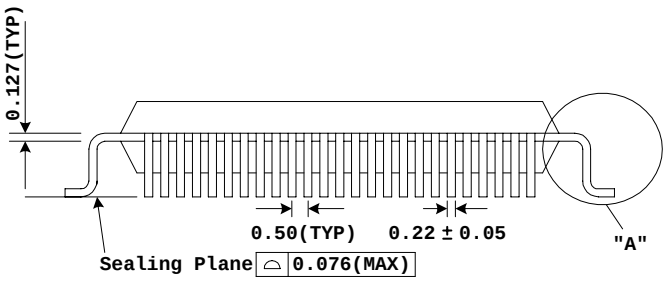


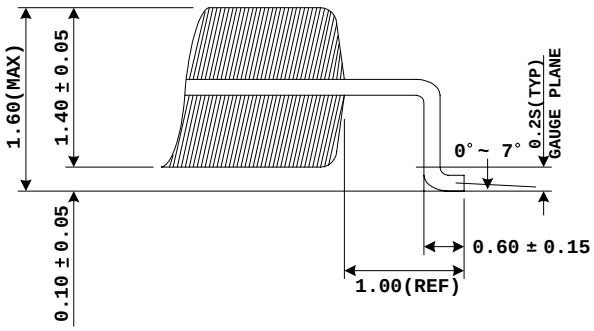




25.2 LQFP







UNIT:mm

Revision History

Rev.	Date	History
F10	2001/12/19	Formal Release
F11	2002/05/06	Modify JTAG and Wait State Description
F12	2002/07/11	Add DC/AC Characteristics
F12	2005/08/31	Format Modification