REV.	E.C.O. NO.	ZONE	DESCRIPTION	DATE	BY APPD
PR			PRE RELEASED	5-3-82	JBF JBF
A	1018		SHEET 1. ADD R46, 10 K. ADD D10, 1N914A; SHEET 2, ADD C29 1/50 ; U21 PIN 3 TIED TO U11 PINS 2 WAS TIED TO U21 PINS 2, 9 AND 10 "RELEASED"	4-26-82	JBF
B	1072	–	SHEET 1 REVISED CONNECTION OF C10 C11; PIN 3 OF U6 WAS CONNECTED TO I/O AND PIN 4 WAS CONN. TO 15. SHEET 2 ; ADDED C25, C26, C27.	8-16-82	DPG
C	1226		CHANGED: SCHEMATIC TO REFLECT THE CHANGE OF NEW IC FOR U5, ON SHEET 1 OF 2 & 2 OF 2. AND ADDITION OF R50 ON SHEET 2 OF 2. REV. ; R45, 4.7K WAS 10K; REV., J1, J2, J3 WERE P1, P2, P3; DELETED D5, 1N4004; R25, 270 Ω; R27, 1K; R28, 1K; Q1, 2N4401 AND Q2, 2N4403 ; LABELED TERM. BLOCK NO.'S 18-20; ADD POLARITY CB	3-8-83	MAR
D	1443		RE-DESIGNED CIRCUIT TO ACCEPT GENERIC 6116 CMOS RAM; CHANGED POWER FAIL CIRCUIT AND SPEED PICK-UP CIRCUIT	11-15-83	SAE
E	1561		ADDED NOTE 7	3-12-84	SAE
F	1683		U6, TIED PINS 17 AND 27 TO +5V	5-25-84	SAE
G	9488		ADDED C33, C34 AND R53	9-1995	LD

A.C. C.T. J3-1 ⟷ J2-15
J3-2 ⟷ J2-16
A.C. POWER J3-3 ⟷ J2-17

+ I OUT, 20 ⟷ J2-18
- I OUT, 19 ⟷ J2-20
I OUT SHIELD, 18 ⟷ J2-19

NOTE:
1. ALL RESISTORS ARE 1/4 W, 5 %, CF, UNLESS OTHERWISE SPECIFIED. RESISTORS MARKED 1% ARE 1/8 W, 1%, MF.
2. ALL CAPACITORS ARE MARKED IN MICROFARADS AND VOLTS.
3. ▽ DENOTES SIGNAL COMMON.
4. ⏚ DENOTES CHASSIS GROUND.
5. ○— DENOTES CONNECTION TO SECOND SHEET.
6. O— DENOTES TERMINAL BLOCK.
7. CHANGES TO THIS DRAWING MAY AFFECT DRAWING NO. D07048D-G014.

ITEM	PART NO.	E / U	DESCRIPTION	DWG NO / SPEC	QTY

DO NOT SCALE DWG
REMOVE ALL BURRS AND UNNECESSARY SHARP EDGES

TOLERANCE UNLESS SPECIFIED
.X ±
.XX ±
.XXX ±
FRACTIONS ±
ANGLES ±

SCALE NONE
JOB NO.
ENGINEER JEF — DATE 3-25-82
DRAWN SRE — DATE 3-25-82
APPROVED JBF — DATE 5-3-82

NEXT ASSY
CUST ORDER NO
CUSTOMER LOCATION
USER LOCATION

Thermo Ramsey
501 – 90th Avenue N W • Minneapolis MN 55433 • (763)783-2500

SCHEMATIC
CPU BOARD
μP MICRO-TECH INTEGRATOR
MODEL 10-201

PART NO	DRAWING NUMBER	REV
	D07033A-B014	G